

LC36256AL, AML-70W/85W/10W/12W

256 K (32768 words × 8 bits) SRAM

Preliminary

Overview

The LC36256AL, AML-70W/85W/10W/12W are fully asynchronous silicon gate CMOS static RAMs with an 32768 words × 8 bits.

This series has \overline{CE} chip enable pin for device select/nonselect control and an \overline{OE} output enable pin for output control, and features high speed, a wide temperature operating range, as well as low power dissipation.

For these reasons, the series is especially suited for use in systems requiring high speed, low power, and battery backup, and it is easy to expand memory capacity.

Features

· Access time

70 ns (max.): LC36256AL-70W, LC36256AML-70W 85 ns (max.): LC36256AL-85W, LC36256AML-85W 100 ns (max.): LC36256AL-10W, LC36256AML-10W 120 ns (max.): LC36256AL-12W, LC36256AML-12W

· Low current dissipation

During standby

2 $\mu A \text{ (max.)} / Ta = 25^{\circ} C$

5 μ A (max.) / Ta = -10 to +40°C

25 μ A (max.) / Ta = -10 to +70°C

During data retention

1 $\mu A \text{ (max.)} / Ta = 25^{\circ} C$

2 $\mu A \text{ (max.)} / Ta = -10 \text{ to } +40^{\circ}C$

10 μ A (max.) / Ta = -10 to +70°C

During operation (DC)

10 mA (max.)

• Single 5 V power supply: 5 V ±10%

Data retention power supply voltage: 2.0 to 5.5 V

No clock required (Fully static memory)

· All input/output levels are TTL compatible

· Common input/output pins, with three output states

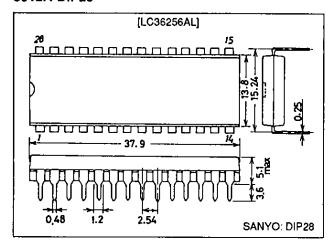
· Packages

DIP 28-pin plastic package: LC36256AL SOP 28-pin plastic package: LC36256AML

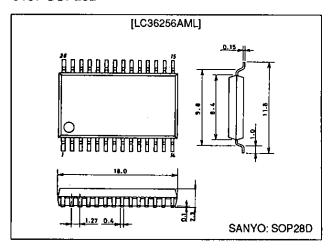
Package Dimensions

unit: mm

3012A-DIP28



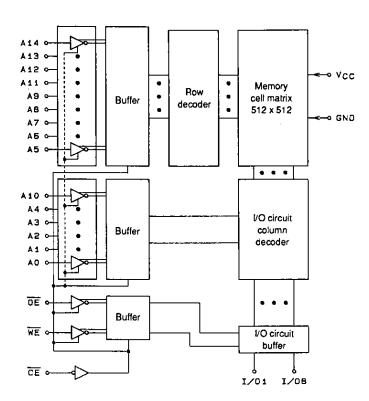
3187-SOP28D



Pin Assignment

DIP28, SOP28D A14 1 28 VCC A12 2 27 WE A7 3 26 A13 25 AB A6 4 A5 5 24 A9 23 A11 A4 6 A3 7 22 DE 42 B 21 A10 A1 9 20 <u>CE</u> A0 10 19 I/OB 1/01 11 18 I/07 1/02 12 17 I/06 I/03 13 16 1/05 GND 14 15 I/04 **Top View** A01783

Block Dlagram



Pin Functions

A ₀ to A ₁₄	Address input
WE	Read/write control input
Œ	Output enable input
CE	Chip enable input
I/O ₁ to I/O ₈	Data input/output
V _{CC} , GND	Power supply pins

Functions

Mode	CE	ŌĒ	WE	VO	Supply current
Read cycle	Ł	L	Н	Data output	ICCA
Write cycle	Ł	Х	L	Data input	ICCA
Output disable	L	Н	Н	High impedance	ICCA
Nonselect	Н	Х	X	High impedance	lccs

X: H or L

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{CC} max		7.0	٧
Input pin voltage	V _{IN}		-0.5* to V _{CC} + 0.5	v
I/O pin voltage	V _{I/O}		-0.5* to V _{CC} + 0.5	V
Allowable power dissipation	Pd max	LC36256AL	1.0	W
Allowable power dissipation	Fu max	LC36256AML	0.7	W
Operating temperature range	Topr		-10 to +70	°C
Storage temperature range	Tstg		-55 to +150	°C

^{* -3.0} V when pulse width is less than 50 ns

DC Recommended Operating Ranges at $Ta = -10 \text{ to } +70^{\circ}\text{C}$

Parameter	Symbol	min	typ	max	Unit
Power supply voltage	V _{CC}	4.5	5.0	5.5	٧
Input high level voltage	V _{IH}	2.2		V _{CC} + 0.3	٧
Input low level voltage	V _{tL}	-0.3*	-	+0.8	٧

^{* -3.0} V when pulse width is less than 50 ns

DC Electrical Characteristics at Ta = -10 to +70°C, V_{CC} = 5 V ±10%

Parameter	Symbol	Conditions			min	typ*	max	Unit
Input leakage current	ILI	V _{IN} = 0 to V _{CC}			-0.5		+0.5	μА
I/O leakage current	lLO	VCE = VIH or VOE = VI	Voe VIH or Voe VIH, VI/O = 0 to Voc				+0.5	μА
Output high level voltage	V _{OH}	I _{OH} = -1.0 mA			2.4			v
Output low level voltage	V _{OL}	I _{OL} = 2.1 mA					0.4	V
Operating supply current (DC)	ICCA1 VCI		V _{CE} ≤ 0.2 V, V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} - 0.2 V			1	5	mA
——————————————————————————————————————	I _{CCA2}	V _{CE} = V _{IL} , I _{I/O} = 0 mA			3	10	mA	
		min cycle Duty = 100% i _{I/O} = 0 mA		70 ns		30	50	
Average operating supply current			Access	85 ns		25	50	1.
Avoide operating supply current	CCA3		time	100 ns		23	50	mA
				120 ns		20	50	1
			-10 to				25	T
Standby supply current	I _{CCS1}	Vce ≥ Vcc - 0.2 V		-10 to +40°C			5	μΑ
			25			0.5	2	1
	I _{CCS2}	V _{CE} = V _{IH}				0.4	2	mA

^{*} Reference values at V_{CC} = 5 V, Ta = 25°C

Input/Output Capacitance at Ta = 25°C, f = 1 MHz

Parameter	Symbol	Conditions	min	typ	max	Unit
Input/output capacitance	C _{I/O}	V _{I/O} = 0 V			8	pF
Input capacitance	C _{IN}	V _{IN} = 0 V			6	рF

Note: These parameters were obtained through sampling, and not full-lot measurement.

- No products described or contained herein are intended for use in surgical implants, life-support systems, aerospace equipment, nuclear power control systems, vehicles, disaster/crime-prevention equipment and the like, the failure of which may directly or indirectly cause injury, death or property loss.
- Anyone purchasing any products described or contained herein for an above-mentioned use shall:
 - ① Accept full responsibility and indemnify and defend SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors and all their officers and employees, jointly and severally, against any and all claims and litigation and all damages, cost and expenses associated with such use:
 - ② Not impose any responsibility for any fault or negligence which may be cited in any such claim or litigation on SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors or any of their officers and employees jointly or severally.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

LC36256AL, AML-70W/85W/10W/12W

AC Electrical Characteristics at Ta = –10 to +70°C, V_{CC} = 5 V $\pm 10\,\%$

AC testing conditions

Input pulse voltage level

0.8 V, 2.2 V

Input rise and fall time

5 ns

Input - output timing level

1.5 V

Output load

1 TTL gate + C_L = 100 pF (85 ns/100 ns/120 ns)

1 TTL gate + $C_L = 30 \text{ pF} (70 \text{ ns})$

(including scope and jig capacitance)

Read Cycle

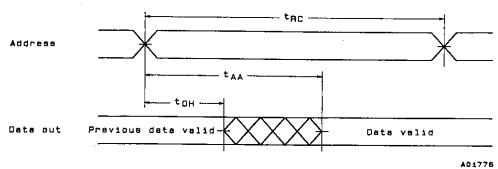
Parameter S	Symbol	LC36256AL-70W LC36256AML-70W		LC36256AL-85W LC36256AML-85W		LC36256AL-10W LC36256AML-10W		LC36256AL-12W LC36256AML-12W		Unit
	İΓ	min	max	min	max	min	max	min	max	1
Read cycle time	t _{RC}	70		85		100		120		ns
Address access time	taa		70		85		100		120	ns
CE access time	t _{CA}		70		85		100		120	ns
OE access time	t _{OA}		35		45		50		60	ns
Output hold time	фн	20		20		20		20		ns
CE output enable time	tCOE	10		10		10		10		ns
OE output enable time	†OOE	5		5		5	1	5		ns
CE output disable time	tcop	0	30	0	30	0	30	0	30	ns
OE output disable time	t _{OOD}	0	30	0	30	0	30	0	30	ns

Write Cycle

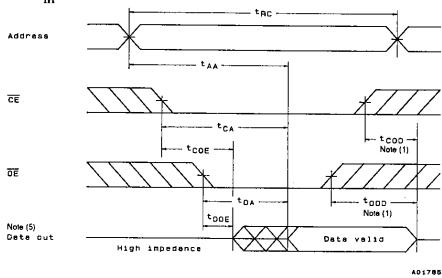
Parameter S	Symbol	LC36256AL-70W LC36256AML-70W		LC36256AL-85W LC36256AML-85W		LC36256AL-10W LC36256AML-10W		LC36256AL-12W LC36256AML-12W		Unit
		min	max	min	max	min	max	min	max	1
Write cycle time	twc	70		85		100		120		ns
Address valid to end of write	taw	65		75		80		100		ns
Address setup time	tas	0		0		0		0		ns
Write pulse width	t _{WP}	50		50	<u> </u>	60		70		ns
CE setup time	t _{CW}	65		75		80		100		ns
Write recovery time (WE)	twR	0		0		0		0		ns
Write recovery time (CE)	t _{WR1}	0		0		0		0		ns
Data setup time	t _{DS}	30		30		35	ĺ	40		ns
Data hold time	t _{DH}	0		0		0		0		ns
WE output enable time	twoE	10		10		10		10		ns
WE output disable time	twop	0	25	0	25	0	25	0	25	nş

Timing Chart

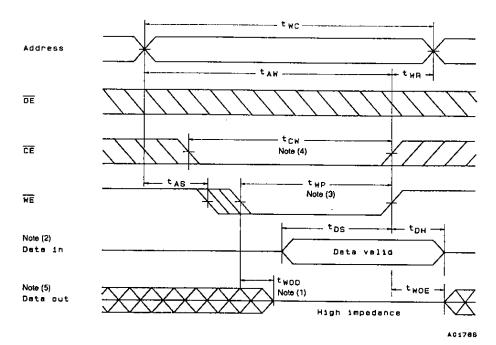
• Read Cycle (1): $\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$



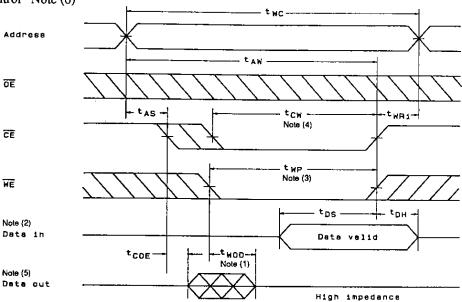
• Read Cycle (2): $\overline{WE} = V_{IH}$



• Write Cycle (1): WE Control Note (6)



• Write Cycle (2): $\overline{\text{CE}}$ Control Note (6)



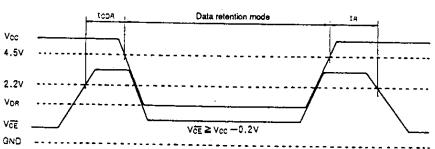
- Notes: (1) t_{COD}, t_{OOD}, and t_{WOD} are defined as the time at which the outputs becomes the high impedance state and are not referred to output voltage levels.
 - (2) An external antiphase signal must not be applied when D_{OUT} is in the output state.
 - (3) t_{WP} is the time interval that \overline{CE} and \overline{WE} are low-level and is defined as the interval from the falling of \overline{WE} to the rising of \overline{CE} or \overline{WE} whichever is earlier.
 - (4) t_{CW} is the time interval that \overline{CE} and \overline{WE} are low-level and is defined as the time from the falling of \overline{CE} to the rising of \overline{CE} or \overline{WE} whichever is earlier.
 - (5) D_{OUT} goes to the high-impedance state when either \overline{OE} is high-level, \overline{CE} is high-level, or \overline{WE} is low-level.
 - (6) When \overline{OE} is high-level during the write cycle, D_{OUT} goes to the high-impedance state.

Data Retention Characteristics at $Ta = -10 \text{ to } +70^{\circ}\text{C}$

Parameter	Symbol	Conditions	min	typ*	max	Unit	
Data retention supply voltage	V_{DR}	V _{CE} ≥ V _{CC} - 0.2 V		2.0		5.5	V
Data retention supply current			-10 to +70°C			10	
	I _{CCDR1}	V _{CC} = 3.0 V, V _{CE} ≥ 2.8 V	-10 to +40°C			2	μ×
Data retention supply current		<u>L</u>	25°C		0.25	1	1
	ICCDR2	V _{CC} = 2.0 to 5.5 V, V _{CE} ≥ V _{CC} - 0.2 V			0.5	25	μA
CE setup time	tCDR			0		· · · · · · · · · · · · · · · · · · ·	ns
CE hold time	t _B			t _{RC} **		-	ns

^{*} Reference values at Ta = 25°C

Data Retention Waveform



^{**} t_{RC} = read cycle time