Ordering number : EN4969

CMOS LSI

SANYO

No. 4969

LC78681KE, 78681KE-L

Digital Signal Processor for Compact Disc Players

Overview

The LC78681KE and LC78681KE-L are signal processing and servo control CMOS LSIs for compact disk players, laser disk players, CD-V, CD-I and similar applications. These products provide a rich set of signal processing functions, including demodulation of the EFM signal from the optical pickup, de-interleaving, error detection and correction, and digital filter functions that can contribute to end product cost reduction. These LSIs also process servo system commands sent from a control microprocessor. They can be directly interfaced to a serial input DAC (such as the Sanyo LC78835K or LC78855K) that provides built-in dedicated digital filters.

Functions

- Input signal processing: The LC78681KE takes an HF signal as input, digitizes (slices) that signal at a precise level, converts that signal to an EFM signal, and generates a PLL clock with an average frequency of 4.3218 MHz by comparing the phases of that signal and a VCO output.
- Precise reference clock and necessary internal timing generation using an external 16.9344 MHz crystal oscillator
- Disk motor speed control using a frame phase difference signal generated from the playback clock and the reference clock
- Frame synchronization signal detection, protection and interpolation to assure stable data readout
- EFM signal demodulation and conversion to 8-bit symbol data
- Subcode data separation from the EFM demodulated signal and output of that data to an external microprocessor
- Subcode Q signal output to a microprocessor over the serial interface after performing a CRC error check (An LSB first output format can be selected.)
- Demodulated EFM signal buffering in internal RAM to handle up to ±4 frames of disk rotational jitter
- Demodulated EFM signal reordering in the prescribed order for data unscrambling and de-interleaving
- Error detection, correction, and flag processing (error correction scheme: dual C1 plus dual C2 correction)
- The LC78681KE sets the C2 flags based on the C1 flags and a C2 check, and then performs signal interpolation or previous value hold depending on the C2 flags. The interpolation circuit uses a quadruple interpolation scheme. The output value is locked at zero when four or more consecutive C2 flags occur.
- Support for command input from a control microprocessor: commands include track jump, focus start, disk motor start/stop, muting on/off and track count (8 bit serial input)
- Built-in digital output circuits.
- Arbitrary track counting to support high-speed data access
- Zero cross muting
- Double speed dubbing support
- Supports most D/A converters
- Built-in digital level and peak meter functions
- Support for bilingual applications

Features

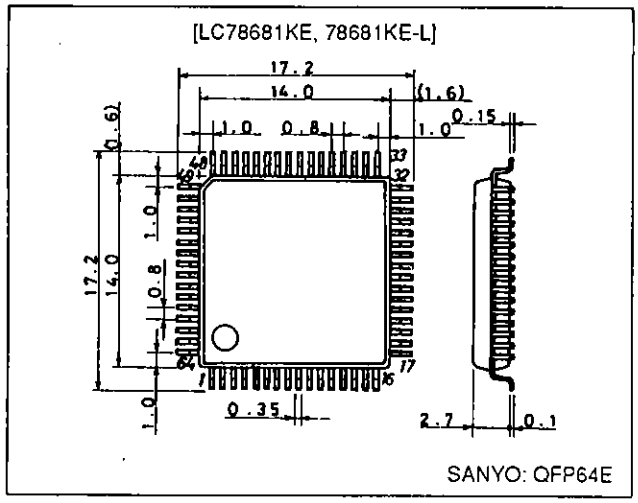
- 64-pin QFP (miniature, reduced space package)
- Silicon gate CMOS process (low power)
- Provision of a DEMO pin eases the manufacturing processes associated with adjustment steps.
- Low voltage operation (LC78681KE-L)

SANYO Electric Co., Ltd. Semiconductor Business Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

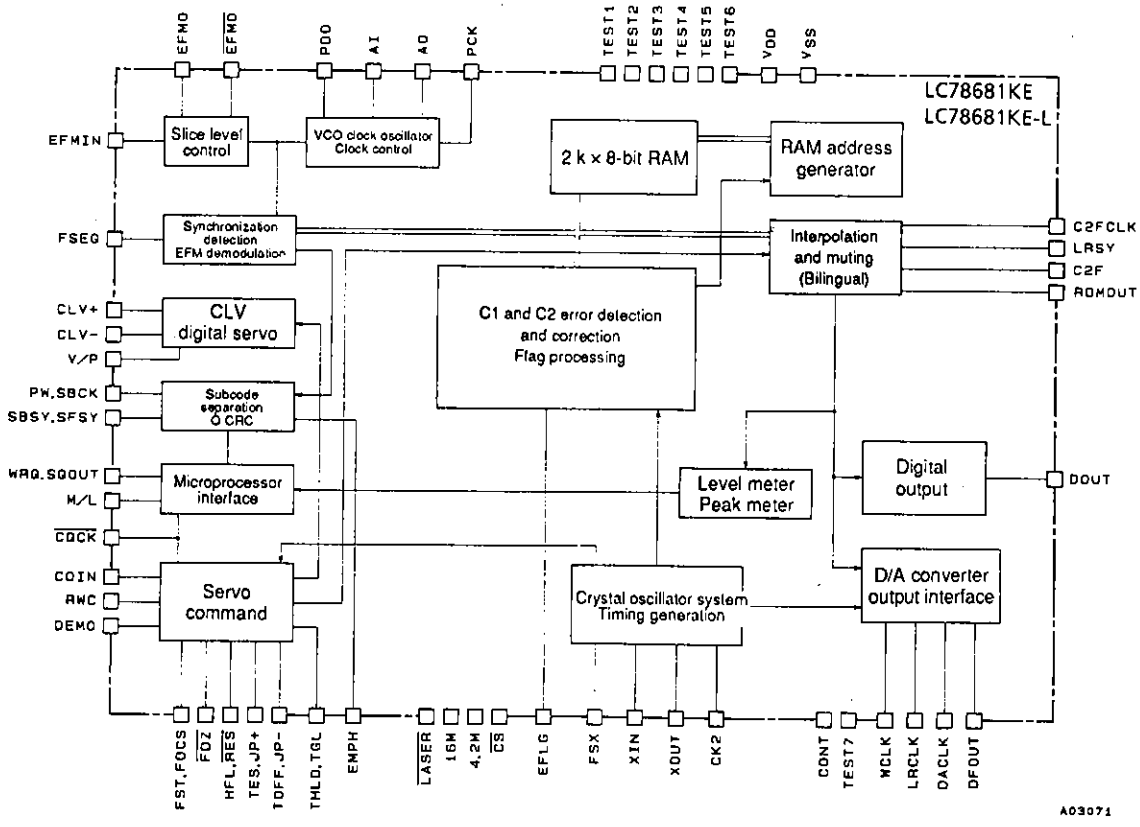
Package Dimensions

unit: mm

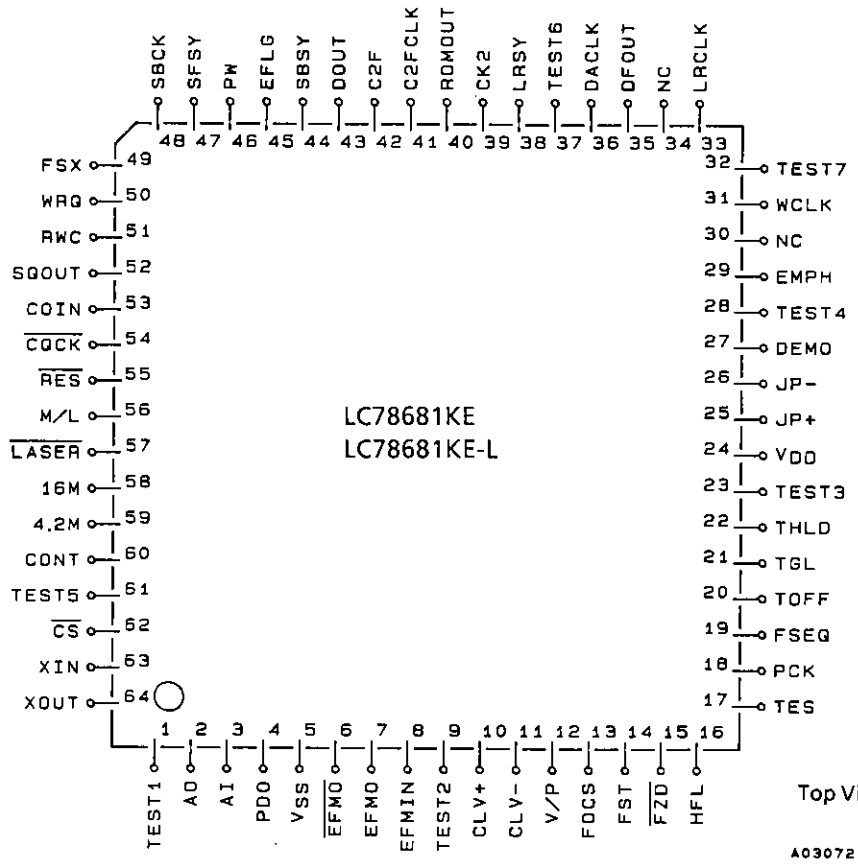
3159-QFP64E



Equivalent Circuit Block Diagram



Pin Assignment



Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		V_{SS} – 0.3 to +7	V
Maximum input voltage	V_{IN} max		V_{SS} – 0.3 to V_{DD} + 0.3	V
Maximum output voltage	V_{OUT} max		V_{SS} – 0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max		300	mW
Operating temperature	**Topr**		–30 to +75	°C
Storage temperature	Tstg		–40 to +125	°C

Allowable Operating Ranges at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}	V_{DD}	*		5.5	V
Input high level voltage	V_{IH} (1)	TEST1 to 5, AI, $\overline{FZD}$, HFL, DEMO, M/L, $\overline{RES}$	0.7 V_{DD}		V_{DD}	V
	V_{IH} (2)	SBCK, RWC, COIN, $\overline{CQCK}$, $\overline{CS}$	2.2		V_{DD}	V
	V_{IH} (3)	EFMIN	0.6 V_{DD}		V_{DD}	V
	V_{IH} (4)	TES	0.8 V_{DD}		V_{DD}	V
Input low level voltage	V_{IL} (1)	TEST1 to 5, AI, $\overline{FZD}$, HFL, DEMO, M/L, $\overline{RES}$	V_{SS}		0.3 V_{DD}	V
	V_{IL} (2)	SBCK, RWC, COIN, $\overline{CQCK}$, $\overline{CS}$	V_{SS}		0.8	V
	V_{IL} (3)	EFMIN	V_{SS}		0.4 V_{DD}	V
	V_{IL} (4)	TES	V_{SS}		0.2 V_{DD}	V
Data setup time	t_{setup}	COIN, RWC: Figure 1	400			ns
Data hold time	t_{hold}	RWC: Figure 1	400			ns
High level clock pulse width	$t_{WøH}$	SBCK, $\overline{CQCK}$: Figures 1, 2 and 3	400			ns
Low level clock pulse width	$t_{WøL}$	SBCK, $\overline{CQCK}$: Figures 1, 2 and 3	400			ns
Data read access time	t_{RAC}	Figures 2 and 3	0		400	ns
Command transfer time	t_{RWC}	RWC: Figure 1	1000			ns
Subcode Q read enable time	t_{SQE}	Figure 2, with no RWC signal		11.2		ms
Subcode read cycle	t_{sc}	Figure 3		136		µs
Subcode read enable time	t_{se}	Figure 3	400			ns
Crystal oscillator frequency	fX'tal	XIN, XOUT		16.9344		MHz
Operating frequency range	fop (1)	AI	2.0		20	MHz
	fop (2)	EFMIN: V_{IN} ≥ 1 Vp-p			10	MHz

Note: * This value differs between the LC78681KE and the LC78681KE-L.
The only difference between these products is the minimum value of the supply voltage V_{DD}, as listed in the table below.

	Normal speed playback	Double speed playback
LC78681KE	4.5 V	4.5 V
LC78681KE-L	3.0 V	3.3 V

Electrical Characteristics at Ta = 25°C, V_{SS} = 0 V, V_{DD} = 5 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply current	I_{DD}			17	30	mA
Input high level current	I_{IH} (1)	AI, EFMIN, $\overline{FZD}$, TES, SBCK, COIN, $\overline{CQCK}$, $\overline{RES}$, HFL, RWC, M/L: V_{IN} = V_{DD}			5	µA
	I_{IH} (2)	TEST1 to 5, DEMO, $\overline{CS}$: V_{IN} = V_{DD} = 5.5 V	25		75	µA
Input low level current	I_{IL} (1)	AI, EFMIN, $\overline{FZD}$, TES, SBCK, COIN, $\overline{CQCK}$, $\overline{RES}$, HFL, RWC, M/L: V_{IN} = V_{SS}	−5			µA
Output high level voltage	V_{OH} (1)	AO, PDO,EFMO, $\overline{EFMO}$, CLV+, CLV−, FOCS, FSEQ, PCK, TOFF, TGL, THLD, JP+, JP−, EMPH, EFLG, FSX, V/P: I_{OH} = −1 mA	V_{DD} − 1			V
	V_{OH} (2)	DOUT: I_{OH} = −12 mA	V_{DD} − 0.5			V
	V_{OH} (3)	$\overline{LASER}$, SQOUT, 16M, 4.2M, CONT, LRCLK, WRQ, C2F, DACLK, SFSY, LRSY, SBSY, CK2, PW, ROMOUT, C2FCLK, DFOUT, TEST7, WCLK: I_{OH} = −0.5 mA	V_{DD} − 1			V
Output low level voltage	V_{OL} (1)	AO, PDO, EFMO, $\overline{EFMO}$, CLV+, CLV−, FOCS, FSEQ, PCK, TOFF, TGL, THLD, JP+, JP−, EMPH, EFLG, FSX, V/P: I_{OL} = 1 mA			1	V
	V_{OL} (2)	DOUT: I_{OL} = 12 mA			0.5	V
	V_{OL} (3)	$\overline{LASER}$, SQOUT, 16M, 4.2M, CONT, LRCLK, WRQ, C2F, DACLK, SFSY, LRSY, SBSY, CK2, PW, ROMOUT, C2FCLK, DFOUT, TEST7, WCLK: I_{OL} = 2 mA			0.4	V
	V_{OL} (4)	FST: I_{OL} = 5 mA			0.75	V
Output off leakage current	I_{OFF} (1)	PDO, FST: V_{OH} = V_{DD}			5	µA
	I_{OFF} (2)	PDO, FST: V_{OL} = V_{SS}	−5			µA

Waveform

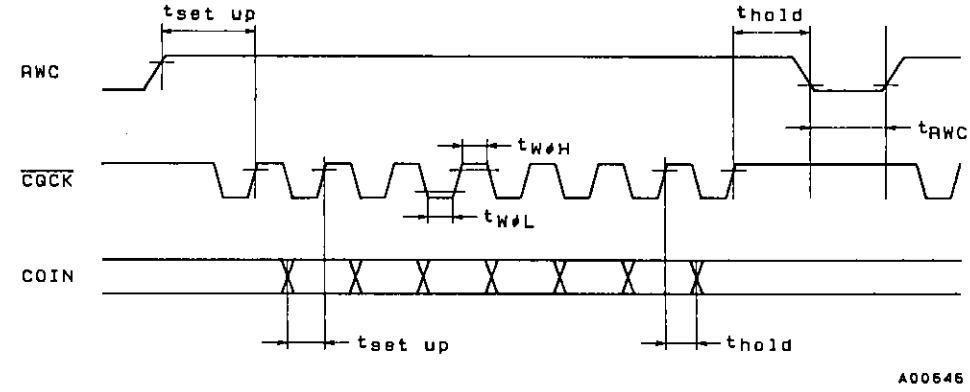


Figure 1 Command Input

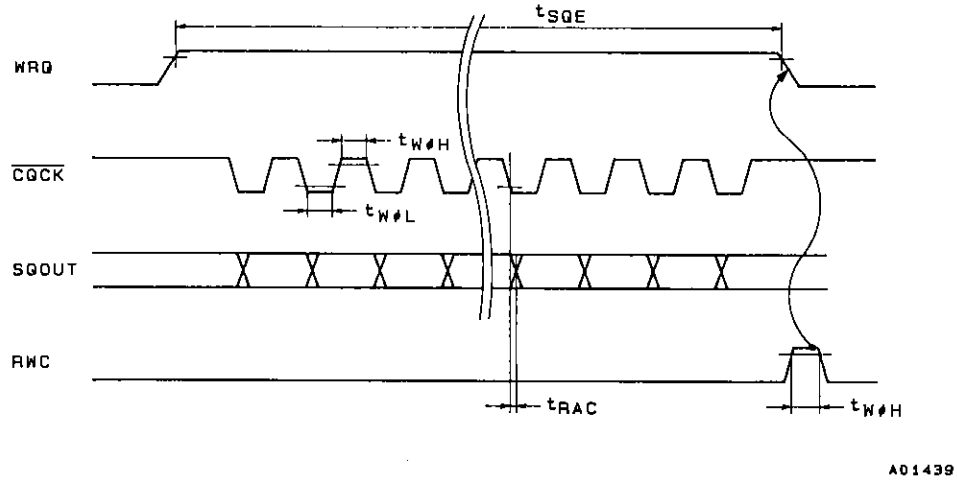


Figure 2 Subcode Q Output

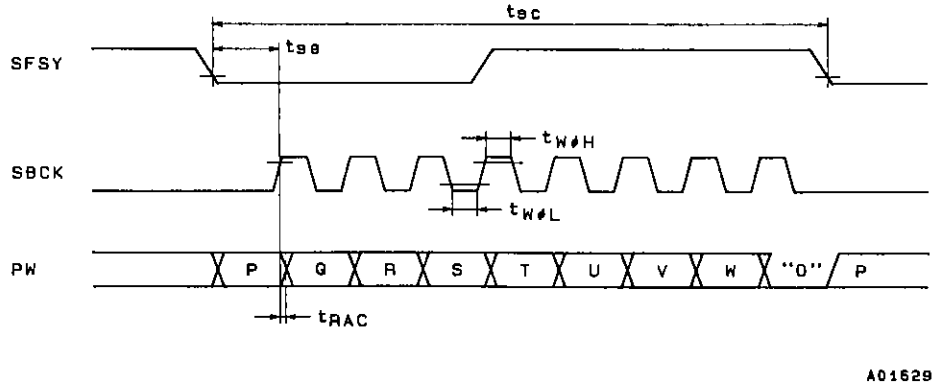


Figure 3 Subcode Output

Pin Functions

No.	Name	I/O	Description
1	TEST1	I	LSI test pin. Normally left open.
2	AO	O	Inputs for the LA9210 internal VCO output. (8.6436 MHz) Set up PDO so that the frequency increases when the EFM signal and the phase output are positive.
3	AI	I	
4	PDO	O	
5	V_{SS}	—	GND
6	$\overline{EFMO}$	O	Supply an HF signal with a 1 to 2 Vp-p level to EFMIN. EFMO and $\overline{EFMO}$ output EFM signals with opposite phases that passed through an amplitude limiter circuit. These are used for slice level control.
7	EFMO	O	
8	EFMIN	I	
9	TEST2	I	LSI test pin. Normally left open.
10	CLV+	O	Disk motor control output.
11	CLV−	O	
12	V/P	O	Outputs a high level during CLV rough servo and a low level during phase control.
13	FOCS	O	FOCS outputs a high level when the focus servo is off. The lens is lowered by FST, and when FOCS is high the lens is raised gradually. FOCS is reset when an $\overline{FZD}$ input occurs. These are used for focus pull-in.
14	FST	O	
15	$\overline{FZD}$	I	
16	HFL	I	The LC78681KE outputs a kick pulse from JP+ and JP− in response to a track jump command. A track jump of the specified number of tracks (1, 2, 4, 16, 32, 64, and 128) is performed.
17	TES	I	
18	PCK	O	PCK is the 4.3218 MHz monitor pin.
19	FSEQ	O	FSEQ outputs a high level when the synchronization (positive FS) detected from the EFM signal matches the counter synchronization (interpolation FS). (The output is latched for a single frame.)
20	TOFF	O	The LC78681KE outputs a kick pulse from JP+ and JP− in response to a track jump command. A track jump of the specified number of tracks (1, 2, 4, 16, 32, 64, and 128) is performed.
21	TGL	O	
22	THLD	O	
23	TEST3	I	LSI test pin. Normally left open.
24	V_{DD}	—	+5 V
25	JP+	O	The LC78681KE outputs a kick pulse from JP+ and JP− in response to a track jump command. A track jump of the specified number of tracks (1, 2, 4, 16, 32, 64, and 128) is performed.
26	JP−	O	
27	DEMO	I	Sound output function for end product adjustment manufacturing steps.
28	TEST4	I	LSI test pin. Normally left open.
29	EMPH	O	De-emphasis is required when high.
30	NC		No connection
31	WCLK	O	Signal used for signal output to the D/A converter, latch signal and L/R switching, and sample and hold.
32	TEST7	O	LSI test pin. Normally left open.
33	LRCLK	O	Signal used for signal output to the D/A converter, latch signal and L/R switching, and sample and hold.
34	NC		No connection
35	DFOUT	O	Signals used for signal output to the D/A converter, latch signal and L/R switching, and sample and hold.
36	DACLK	O	
37	TEST6	O	LSI test pin. Normally left open.
38	LRSY	O	CD-ROM application output signals
39	CK2	O	
40	ROMOUT	O	
41	C2FCLK	O	
42	C2F	O	
43	DOUT	O	Digital output
44	SBSY	O	Subcode block synchronization signal
45	EFLG	O	C1, C2, single and double error correction monitor pin
46	PW	O	SFSY is the subcode frame synchronization signal. The P, Q, R, S, T, U, V and W subcodes can be read out by applying 8 clock cycles to SBCK.
47	SFSY	O	
48	SBCK	I	
49	FSX	O	7.35 kHz synchronization signal output

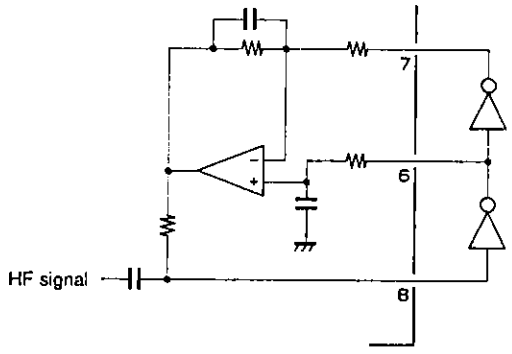
Continued on next page.

Continued from preceding page.

No.	Name	I/O	Description
50	WRQ	O	WRQ goes high when the subcode Q data passes the CRC check. An external controller can read out data from SQOUT by monitoring this pin and applying a $\overline{CQCK}$ signal. Set M/L to low when data is required LSB first. The control microprocessor can send commands to the LC78681KE by setting RWC high and then sending command data synchronized with $\overline{CQCK}$.
51	RWC	I	
52	SQOUT	O	
53	COIN	I	
54	$\overline{CQCK}$	I	
55	$\overline{RES}$	I	This pin must be set low briefly after power is first applied.
56	M/L	I	Similar to pins number 50, 51, 52, 53 and 54 described above.
57	$\overline{LASER}$	O	Output pin controllable by serial data sent from the microprocessor.
58	16M	O	16.9344 MHz output pin
59	4.2M	O	4.2336 MHz output pin
60	CONT	O	Output pin controllable by serial data sent from the microprocessor.
61	TEST5	I	LSI test pin. Normally left open.
62	$\overline{CS}$	I	Chip select pin. The LC78681KE becomes active when this pin is low. (A pull-down resistor is built-in.)
63	X_{IN}	I	Connections for a 16.9344 MHz crystal oscillator
64	X_{OUT}	O	

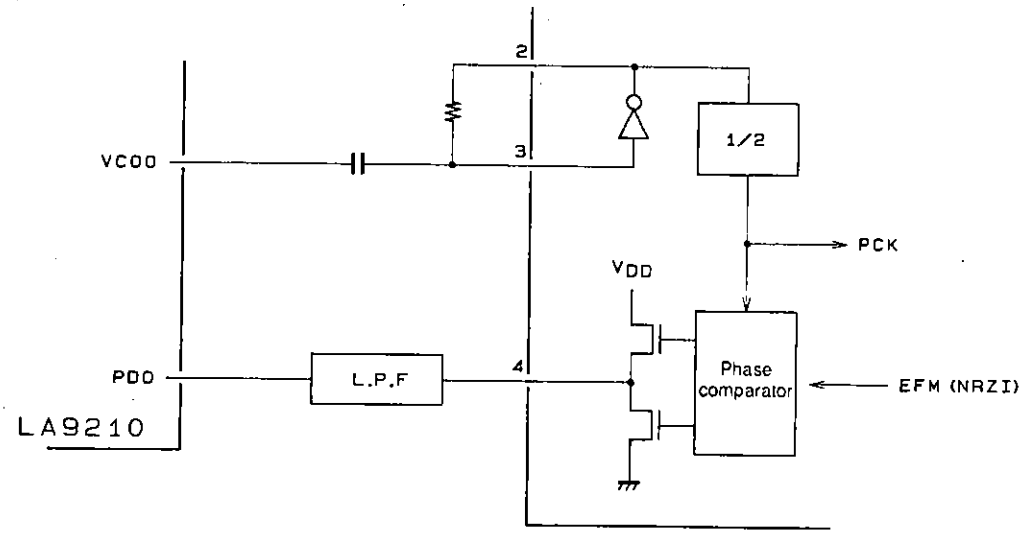
Pin Applications

1. HF signal input circuit; Pin 8: EFMIN, pin 7: EFMO, pin 6: $\overline{EFMO}$
   An EFM signal (NRZ) with an optimal slice level can be acquired by inputting the HF signal to EFMIN.



A01440

2. PLL clock generation circuit; Pin 4: PDO, Pin 3: AI, Pin 2: AO



A01441

A VCO can be constructed by combining the LC78681KE with the Sanyo LA9210. The PDO pin swings in the positive direction when the VCO phase lags.

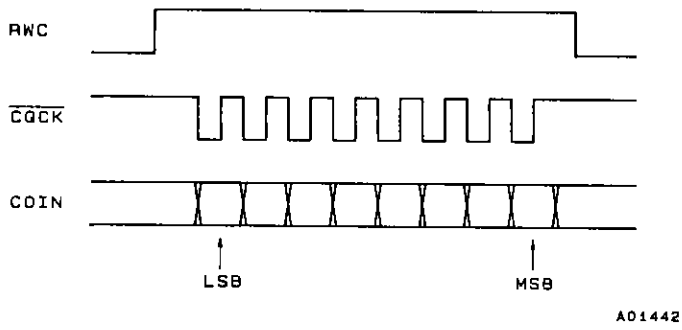
3. 1/2 VCO; Pin 18: PCK
   PCK is a monitor pin that outputs an average frequency of 4.3218 MHz, which is the VCO frequency divided by two.

4. Synchronization detection monitor; Pin 19: FSEQ
   Pin 19 goes high when the frame synchronization (a positive polarity synchronization signal) from the EFM signal read in by PCK and the timing generated by the counter (the interpolation synchronization signal) agree. This pin is a synchronization detection monitor. (It is held high for a single frame.)

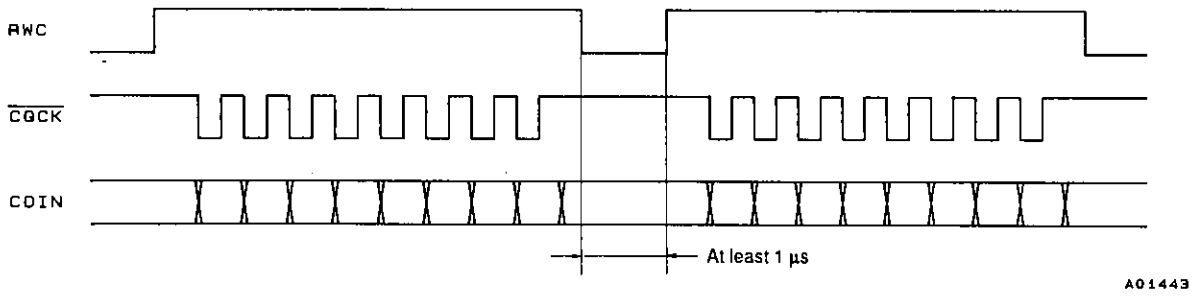
5. Servo command function; Pin 51: RWC, pin 53: COIN, pin 54: CQCK, pin 62: CS
   Commands are input to the LC78681KE by setting RWC high and sending commands to the COIN pin in synchronization with the $\overline{\text{CQCK}}$ clock.

Focus start Track jump Mute control Disc motor control Other control commands	1-byte commands
Track count	2-byte command

- 1-byte commands



- 2-byte commands



Command execution starts on the falling edge of the RWC signal.

- Command noise exclusion

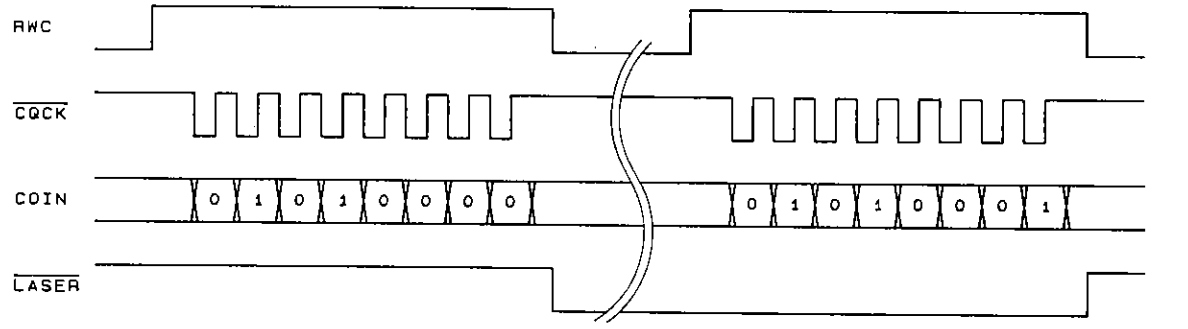
MSB LSB	Command	$\overline{\text{RES}}$ = low
1 1 1 0 1 1 1 1	COMMAND INPUT NOISE EXCLUSION MODE	
1 1 1 0 1 1 1 0	RESET NOISE EXCLUSION MODE	○

This command allows the noise on the $\overline{\text{CQCK}}$ clock signal to be excluded.

6. Focus servo circuit; Pin 13: FOCS, pin 14: FST, pin 15: $\overline{\text{FZD}}$, pin 57: $\overline{\text{LASER}}$

MSB LSB	Command	$\overline{\text{RES}}$ = low
0 0 0 0 1 0 0 0	FOCUS START #1	
1 0 1 0 0 0 1 0	FOCUS START #2	
0 0 0 0 1 0 1 0	LASER ON	
1 0 0 0 1 0 1 0	LASER OFF	○
0 0 0 0 0 0 0 0	NOTHING	

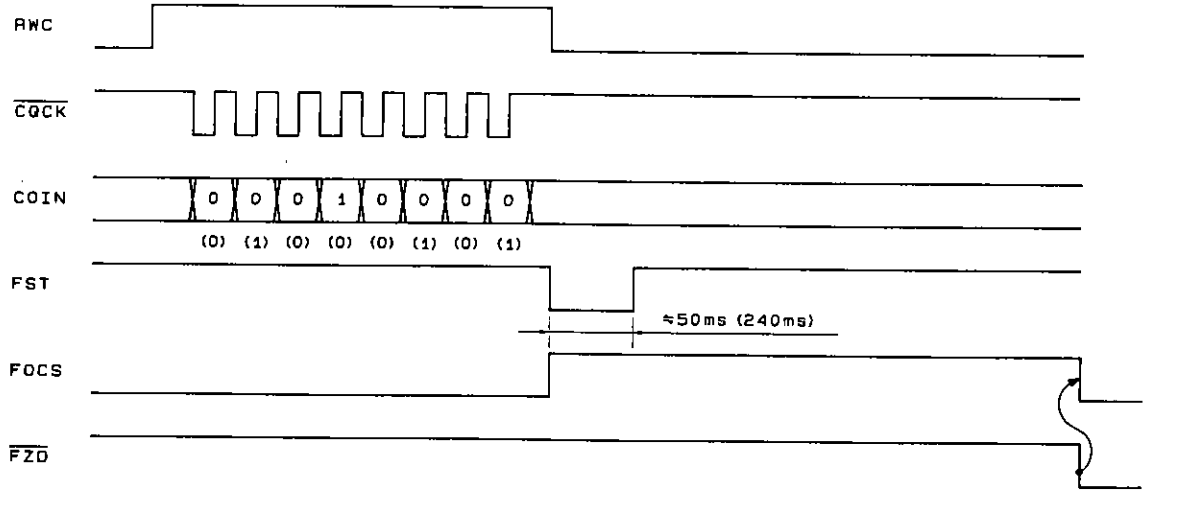
- Laser control



A01444

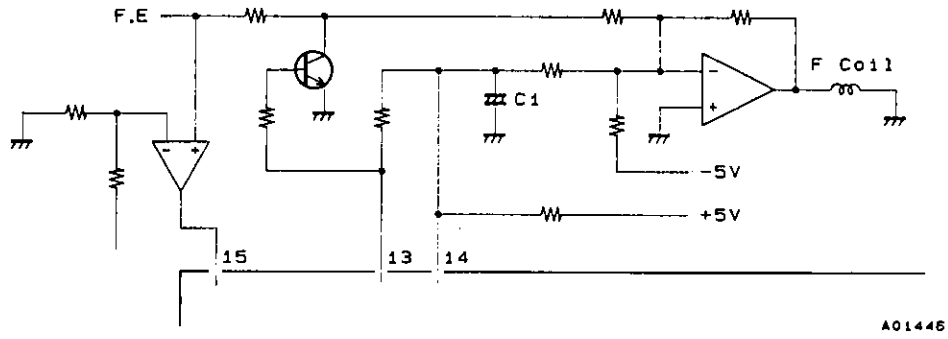
- Focus start

When a focus start instruction (either FOCUS START #1 or FOCUS START #2) is input as a servo command, first the charge on capacitor C1 is discharged by FST and the objective lens is lowered. Next, the capacitor is charged by FOCS, and the lens is slowly raised. $\overline{\text{FZD}}$ falls when the lens reaches the focus point. When this signal is received, FOCS is reset and the focus servo turns on. After sending the command, the microprocessor should check the in-focus detection signal (the LA9210 DRF signal) to confirm focus before proceeding to the next part of the program. If focus is not achieved by the time C1 is fully charged, the microprocessor should issue another focus command and iterate the focus servo operation.



A01445

Note: 1. Values in parentheses are for the FOCUS START #2 command. The only difference is in the FST low period.
2. An $\overline{\text{FZD}}$ falling edge will not be accepted during the period that FST is low.
3. After issuing a focus start command, initialization will be performed if RWC is set high. Therefore, do not issue the next command during focus start until the focus coil drive S curve has completed.
4. When focus cannot be achieved (i.e., when $\overline{\text{FZD}}$ does not go low) the FOCS signal will remain in the high state, so the microprocessor should initialize the system by issuing a NOTHING command.
5. When the RESET pin is set low, the $\overline{\text{LASER}}$ pin is set high directly.
6. Focus start using the DEMO coil executes a mode #1 focus start.

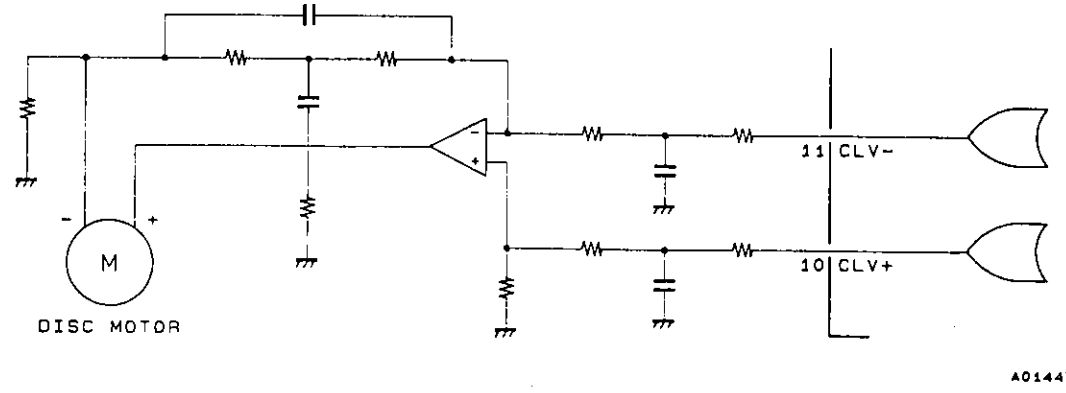


7. CLV servo circuit; Pin 10: CLV+, pin 11: CLV−, pin 12: V/P

MSB LSB	Command	$\overline{RES}$ = low
0 0 0 0 0 1 0 0	DISC MOTOR START (accelerate)	
0 0 0 0 0 1 0 1	DISC MOTOR CLV (CLV)	
0 0 0 0 0 1 1 0	DISC MOTOR BRAKE (decelerate)	
0 0 0 0 0 1 1 1	DISC MOTOR STOP (stop)	O

The CLV+ pin provides the signal that accelerates the disk in the forward direction and the CLV− pin provides the signal that decelerates the disk. Commands from the control microprocessor select one of four modes; accelerate, decelerate, CLV and stop. The table below lists the CLV+ and CLV− outputs in each of these modes.

Mode	CLV+	CLV-
Accelerate	High	Low
Decelerate	Low	High
CLV	*	*
Stop	Low	Low



Note: CLV servo control commands can set the TOFF pin low only in CLV mode. That pin will be at the high level at all other times.

- CLV mode

  In CLV mode the LC78681KE detects the disk speed from the HF signal and provides proper linear speed using several different control schemes by switching the DSP internal modes. The PWM period is 7.35 kHz. V/P outputs a high level during rough servo and a low level during phase control.

Internal mode	CLV+	CLV-	V/P
Rough servo (velocity too low)	High	Low	High
Rough servo (velocity too high)	Low	High	High
Phase control (PCK locked)	PWM	PWM	Low

• Rough servo gain switching

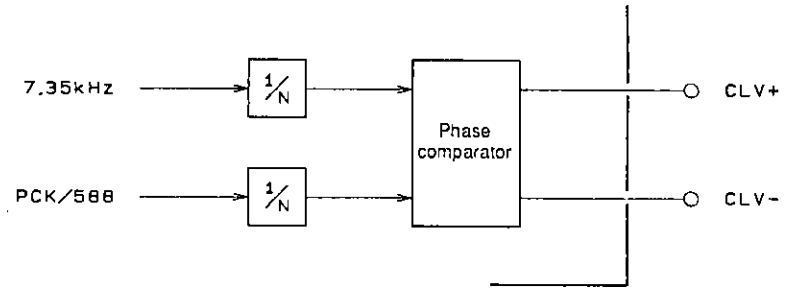
MSB LSB	Command	$\overline{RES}$ = low
1 0 1 0 1 0 0 0	DISC 8 SET	
1 0 1 0 1 0 0 1	DISC 12 SET	○

For 8 cm disks, the rough servo mode CLV control gain can be set about 8.5 dB lower than the gain used for 12 cm disks.

• Phase control gain switching

MSB LSB	Command	$\overline{RES}$ = low
1 0 1 1 0 0 0 1	CLV PHASE COMPARATOR DIVISOR: 1/2	
1 0 1 1 0 0 1 0	CLV PHASE COMPARATOR DIVISOR: 1/4	
1 0 1 1 0 0 1 1	CLV PHASE COMPARATOR DIVISOR: 1/8	
1 0 1 1 0 0 0 0	NO CLV PHASE COMPARATOR DIVISOR USED	○

The phase control gain can be changed by changing the divisor used by the dividers in the stage immediately preceding the phase comparator.

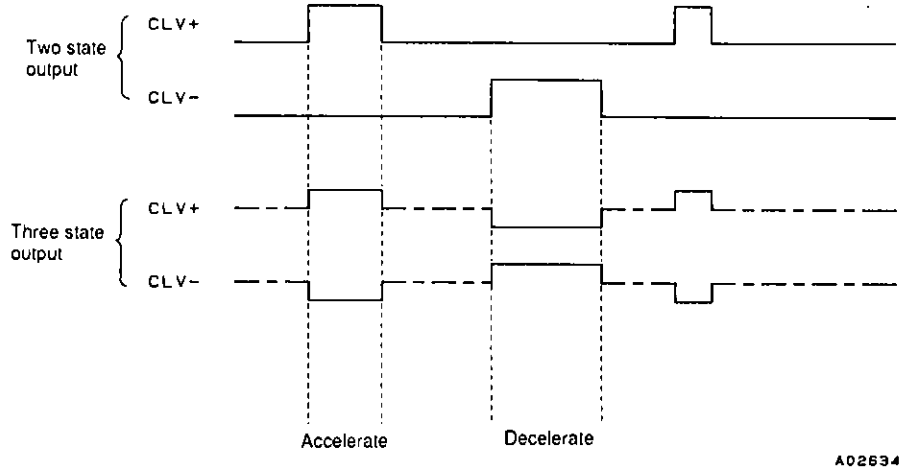


A02633

• CLV three state output

MSB LSB	Command	$\overline{RES}$ = low
1 0 1 1 0 1 0 0	CLV THREE STATE OUTPUT	
1 0 1 1 0 1 0 1	CLV TWO STATE OUTPUT (the scheme used by former products)	○

The CLV three state output command allows the CLV to be controlled by a single pin.



A02634

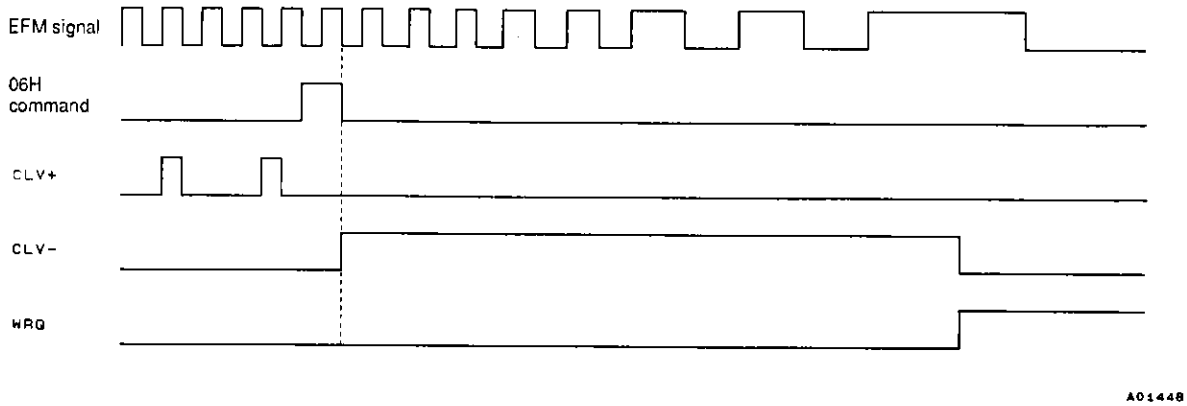
• Internal brake mode

MSB	LSB	Command	$\overline{RES}$ = low
1 1 0 0 0 1 0 1		INTERNAL BRAKE ON	
1 1 0 0 0 1 0 0		INTERNAL BRAKE OFF	O
1 0 1 0 0 0 1 1		INTERNAL BRAKE CONT	
1 1 0 0 1 0 1 1		INTERNAL BRAKE CONTINUOUS MODE	
1 1 0 0 1 0 1 0		RESET CONTINUOUS MODE	O
1 1 0 0 1 1 0 1		TOFF OUTPUT DISABLED MODE	
1 1 0 0 1 1 0 0		RESET TOFF OUTPUT DISABLED MODE	O

— Issuing the internal brake on (C5H) command sets the LC78681KE to internal brake mode. In this mode, the disk deceleration state can be monitored from the WRQ pin when a brake command (06H) is executed.

— In this mode the disk deceleration state is determined by counting the EFM signal in a single frame to determine the density, and when the EFM signal count falls under four, the CLV⁻ pin is dropped to low. At the same time the WRQ signal, which functions as a brake completion monitor, goes high when the microprocessor detects a high level on the WRQ signal, it issues a STOP command to complete the disk stop operation. In internal brake continuous mode, the CLV⁻ pin high level output braking operation continues even after the WRQ brake completion monitor goes high.
Note that if errors occur in deceleration state determination due to noise in the EFM signal, the problem can be rectified by changing the EFM signal count from four to eight with the internal brake control command (A3H).

— In TOFF output disabled mode the TOFF pin is held low during internal brake operations.



Note: 1. If focus is lost during the execution of an internal brake command, the pickup must be refocussed and then the internal brake command can be reissued.
2. Since incorrect deceleration state determination is possible depending on the EFM signal playback state (e.g., disk defects, access in progress), we recommend using these functions in combination with a microprocessor.

8. Track jump circuit; Pin 16: HFL, pin 17: TES, pin 20: TOFF, pin 21: TGL, pin 22: THLD, pin 25: JP⁺, pin 26: JP⁻

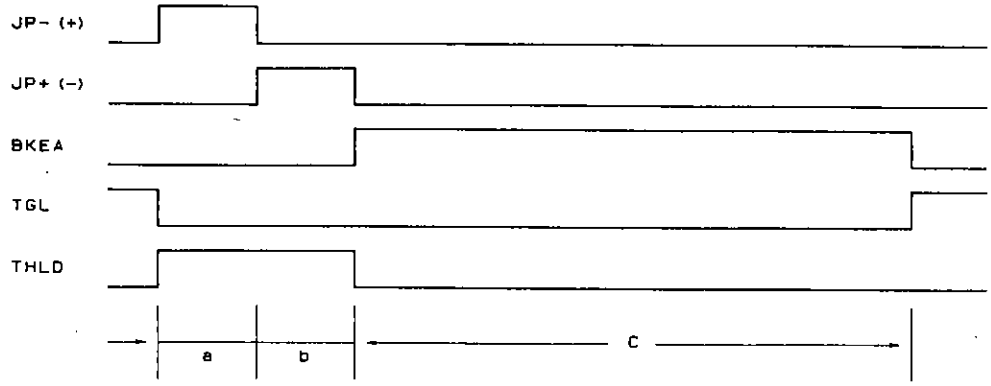
MSB	LSB	Command	$\overline{RES}$ = low
0 0 1 0 0 0 1 0		NEW TRACK COUNT (using the TES/HFL combination)	O
0 0 1 0 0 0 1 1		FORMER TRACK COUNT (directly counts the TES signal)	

• The LC78681KE supports the two track jump commands listed below.

The former track count function uses the TES signal directly as the internal track counter clock. To reduce counting errors resulting from noise on the rising and falling edges of the TES signal, the new track count function prevents noise induced errors by using the combination of the TES and HFL signals, and implements a more reliable track count function. However, dirt and scratches on the disk can result in HFL signal

• Track jump commands

MSB							LSB	Command	$\overline{RES}$ = low
1	0	1	0	0	0	0	0	FORMER TRACK JUMP	O
1	0	1	0	0	0	0	1	NEW TRACK JUMP	
0	0	0	1	0	0	0	1	1 TRACK JUMP IN #1	
0	0	0	1	0	0	1	0	1 TRACK JUMP IN #2	
0	0	1	1	0	0	0	1	1 TRACK JUMP IN #3	
0	1	0	1	0	0	1	0	1 TRACK JUMP IN #4	
0	0	0	1	0	0	0	0	2 TRACK JUMP IN	
0	0	0	1	0	0	1	1	4 TRACK JUMP IN	
0	0	0	1	0	1	0	0	16 TRACK JUMP IN	
0	0	1	1	0	0	0	0	32 TRACK JUMP IN	
0	0	0	1	0	1	0	1	64 TRACK JUMP IN	
0	0	0	1	0	1	1	1	128 TRACK JUMP IN	
0	0	0	1	1	0	0	1	1 TRACK JUMP OUT #1	
0	0	0	1	1	0	1	0	1 TRACK JUMP OUT #2	
0	0	1	1	1	0	0	1	1 TRACK JUMP OUT #3	
0	1	0	1	1	0	1	0	1 TRACK JUMP OUT #4	
0	0	0	1	1	0	0	0	2 TRACK JUMP OUT	
0	0	0	1	1	0	1	1	4 TRACK JUMP OUT	
0	0	0	1	1	1	0	0	16 TRACK JUMP OUT	
0	0	1	1	1	0	0	0	32 TRACK JUMP OUT	
0	0	0	1	1	1	0	1	64 TRACK JUMP OUT	
0	0	0	1	1	1	1	1	128 TRACK JUMP OUT	
0	0	0	1	0	1	1	0	256 TRACK CHECK	
0	0	0	0	1	1	1	1	TOFF	
1	0	0	0	1	1	1	1	TON	O
1	0	0	0	1	1	0	0	TRACK JUMP BRAKE	
0	0	1	0	0	0	0	1	THLD PERIOD TOFF OUTPUT MODE	
0	0	1	0	0	0	0	0	RESET THLD PERIOD TOFF OUTPUT MODE	O



A01449

When the LC78681KE receives a track jump instruction as a servo command, it first generates accelerating pulses (period a) and next generates deceleration pulses (period b).
The passage of the braking period (period c) completes the specified jump. During the braking period, the LC78681KE detects the beam slip direction from the TES and HFL inputs. TOFF is used to cut the components in the TE signal that aggravate slip. The jump destination track is captured by increasing the servo gain with TGL. In THLD period TOFF output mode the TOFF signal is held high during the period when THLD is high.

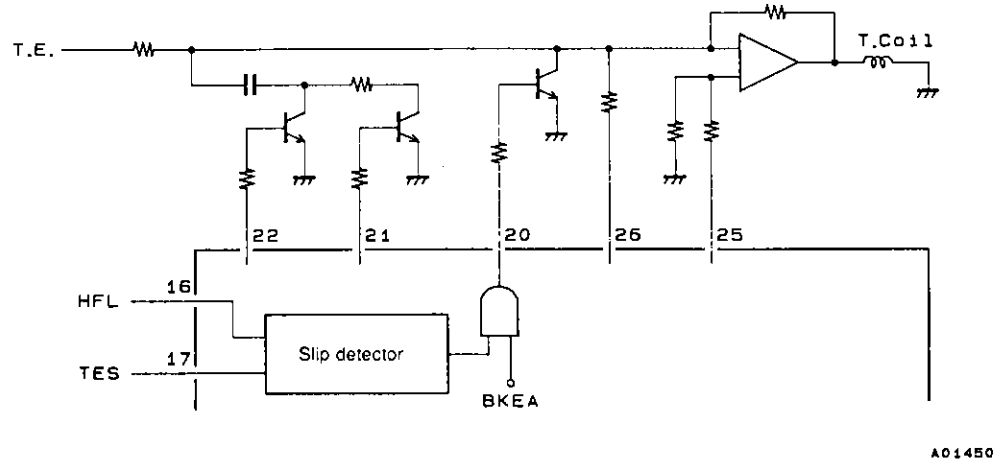
Note: Of the modes related to disk motor control, the TOFF pin only goes low in CLV mode, and will be high during start, stop, and brake operations. Note that the TOFF pin can be turned on and off independently by microprocessor issued commands. However, this function is only valid when disk motor control is in CLV mode.

- Track jump modes

  The table lists the relationships between acceleration pulse output, deceleration pulse output, and the braking period.

Command	Former track jump mode			New track jump mode		
	a	b	c	a	b	c
1 TRACK JUMP IN (OUT) #1	233 µs	233 µs	60 ms	233 µs	233 µs	60 ms
1 TRACK JUMP IN (OUT) #2	0.5-track jump	233 µs	60 ms	0.5-track jump	a period	60 ms
1 TRACK JUMP IN (OUT) #3	0.5-track jump	233 µs	Does not occur	0.5-track jump	a period	Does not occur
1 TRACK JUMP IN (OUT) #4	0.5-track jump	233 µs	60 ms,TOFF = low during the c period	0.5-track jump	a period	60 ms,TOFF = low during the c period
2 TRACK JUMP IN (OUT)	None	None	None	1-track jump	a period	Does not occur
4 TRACK JUMP IN (OUT)	2-track jump	466 µs	60 ms	2-track jump	a period	60 ms
16 TRACK JUMP IN (OUT)	9-track jump	7-track jump	60 ms	9-track jump	a period	60 ms
32 TRACK JUMP IN (OUT)	18-track jump	14-track jump	60 ms	18-track jump	14-track jump	60 ms
64 TRACK JUMP IN (OUT)	36-track jump	28-track jump	60 ms	36-track jump	28-track jump	60 ms
128 TRACK JUMP IN (OUT)	72-track jump	56-track jump	60 ms	72-track jump	56-track jump	60 ms
256 TRACK CHECK	TOFF goes high after 256 tracks are jumped. The a and b pulses are not output.		60 ms	TOFF goes high after 256 tracks are jumped. The a and b pulses are not output.		60 ms
TRACK JUMP BRAKE	There are no a and b periods.		60ms	There are no a and b periods.		60 ms

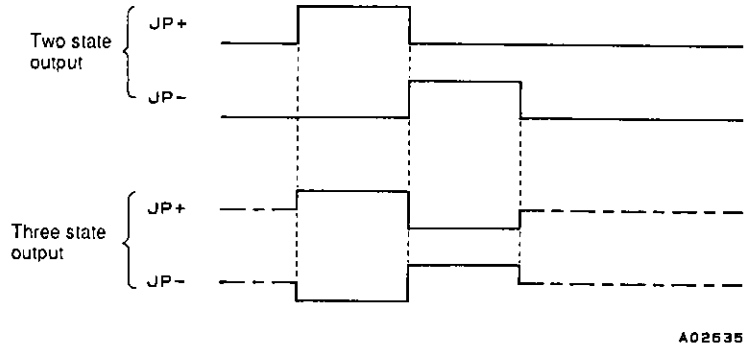
Note: 1. As indicated in the table, actuator signals are not output during the 256 TRACK CHECK function. This is a mode in which the TES signal is counted in the tracking loop off state. Therefore, feed motor forwarding is required.
2. The servo command register is automatically reset after the track jump sequence (a, b, c) completes.
3. If another track jump command is issued during a track jump operation, the content of that new command will be executed starting immediately.



• JP three state output

MSB	LSB	Command	$\overline{RES}$ = low
1 0 1 1 0 1 1 0		JP THREE STATE OUTPUT	
1 0 1 1 0 1 1 1		JP TWO STATE OUTPUT (former scheme)	○

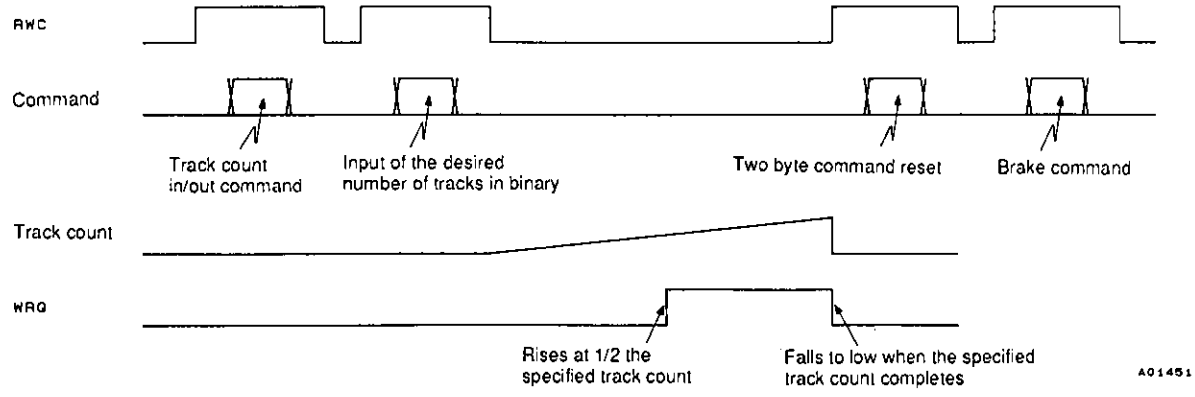
The JP three state output allows the track jump operation to be controlled from a single pin.



• Track check mode

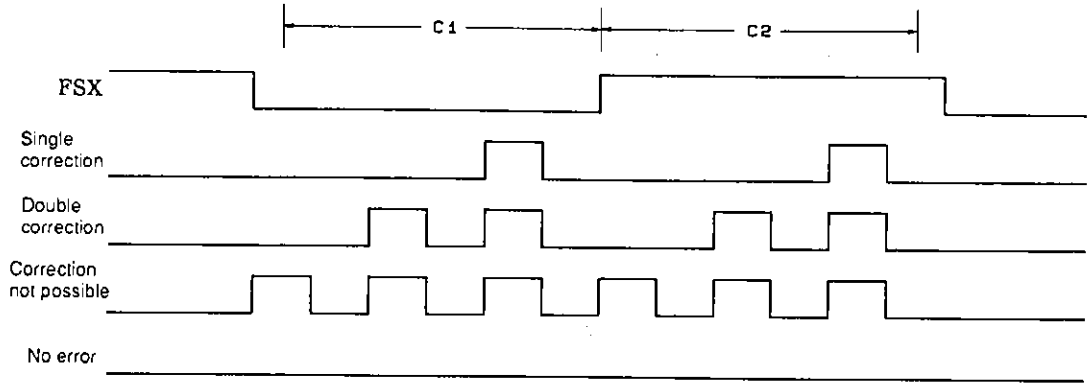
MSB	LSB	Command	$\overline{RES}$ = low
1 1 1 1 0 0 0 0		TRACK COUNT IN	
1 1 1 1 1 0 0 0		TRACK COUNT OUT	
1 1 1 1 1 1 1 1		TWO BYTE COMMAND RESET	○

The LC78681KE will count the specified number of tracks when the microprocessor sends an arbitrary binary value in the range 16 to 254 after issuing either a track count in or a track count out command.



Note: 1. Once the desired track count has been input in binary, the track count operation is started by the fall of RWC.
2. During a track count operation the TOFF pin goes high and the tracking loop is turned off. Therefore, feed motor forwarding is required.
3. When a track count in/out command is issued the function of the WRQ signal switches from the normal mode subcode Q standby monitor function to a track count monitor function. This signal goes high when the track count is half completed, and goes low when the count finishes. The control microprocessor should monitor this signal for a low level to determine when the track count completes.
4. If a two-byte reset command is not issued, the track count operation will be repeated. That is, to skip over 20,000 tracks, issue a track count 200 command once, and then count the WRQ signal 100 times.
5. After performing a track count operation, use the brake command to have the pickup lock onto the track.

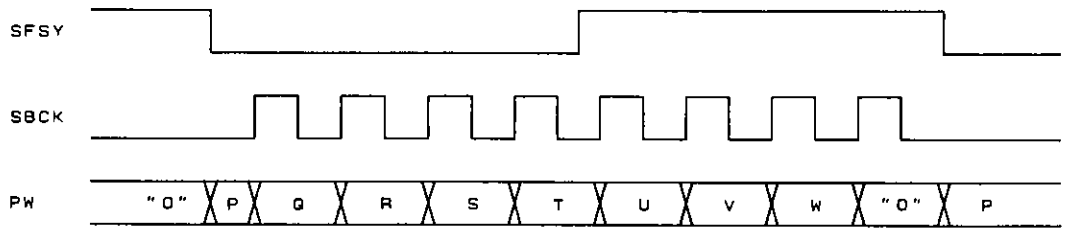
9. Error flag output; Pin 45: EFLG, pin 49: FSX



A01452

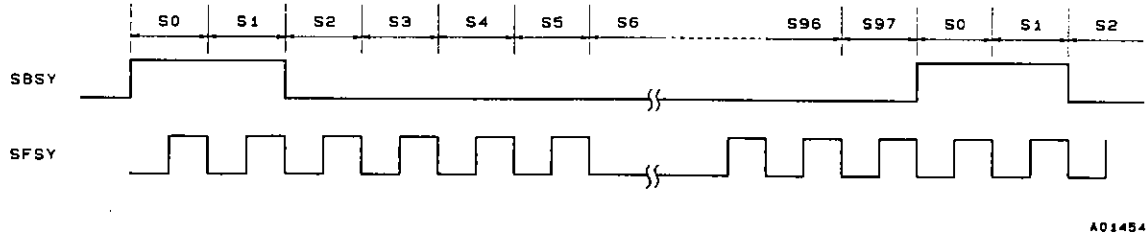
The FSX signal is generated by dividing the crystal oscillator clock, and is a 7.35 kHz frame synchronization signal. The error correction state for each frame is output from EFLG. The playback OK/NG state can be easily determined from the extent of the high level that appears here.

10. Subcode P, Q, and R to W output circuit; Pin 46: PW, pin 44: SBSY, pin 47: SFSY, pin 48: SBCK
PW is the subcode signal output pin, and all the codes P, Q, and R to W can be read out by sending eight clocks to the SBCK pin within 136 µs after the fall of SFSY. The signal that appears on the PW pin changes on the falling edge of SBCK. If a clock is not applied to SBCK, the P code will be output from PW. SFSY is a signal that is output for each subcode frame cycle, and the falling edge of this signal indicates standby for the output of the subcode symbol (P to W). Subcode data P is output on the fall of this signal.



A01453

SBSY is a signal output for each subcode block. This signal goes high for the S0 and S1 synchronization signals. The fall of this signal indicates the end of the subcode synchronization signals and the start of the data in the subcode block. (EIAJ format)



A01454

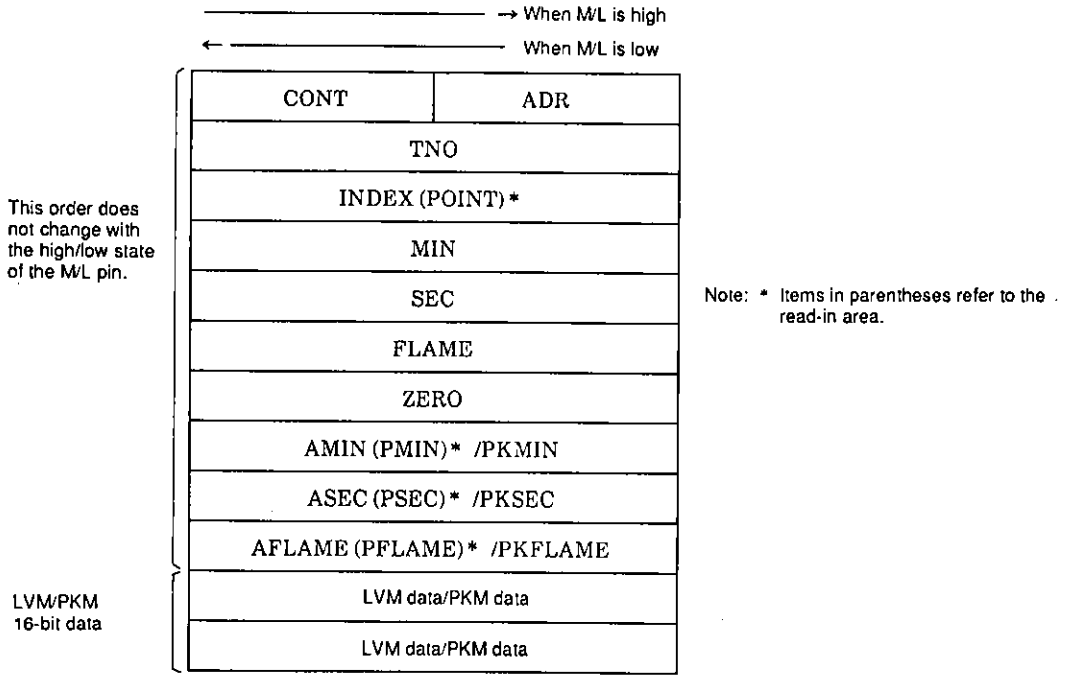
11. Subcode Q output circuit; Pin 50: WRQ, pin 51: RWC, pin 52: SQOUT, pin 54: $\overline{CQCK}$, pin 56: M/L, pin 62: CS

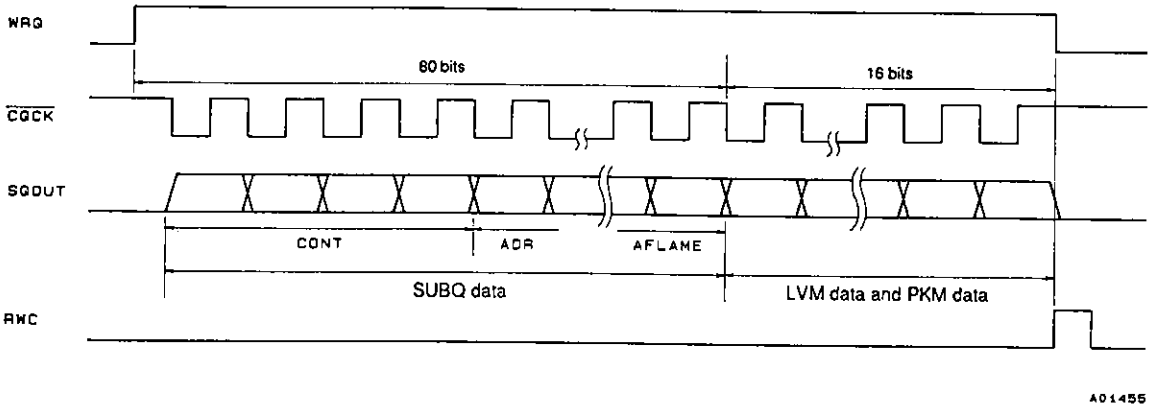
MSB LSB	Command	$\overline{RES}$ = low
0 0 0 0 1 0 0 1	ADDRESS FREE	
1 0 0 0 1 0 0 1	ADDRESS 1	O

Subcode Q can be read from the SQOUT pin by applying a clock to the $\overline{CQCK}$ pin.

Of the eight bits in the subcode, the Q signal is used for song (track) access and display. The WRQ will be high only if the data passed the CRC error check and the subcode Q format internal address is 1*. The control microprocessor can read out data from SQOUT in the order shown below by detecting this high level and applying $\overline{CQCK}$. When $\overline{CQCK}$ is applied the DSP disables register update internally. The microprocessor should give update permission by setting RWC high briefly after reading has completed. WRQ will fall to low at this time. Since WRQ falls to low 11.2 ms after going high, $\overline{CQCK}$ must be applied during the high period. Data can be read out in an LSB first format if the M/L pin is set low, and in an MSB first format if that pin is set high.

Note: * That state will be ignored if an address free command is sent. This is provided to handle CDV applications.





Note: 1. Normally, the WRQ pin indicates the subcode Q standby state. However, it is used for a different monitoring purpose in track count mode and internal brake mode. (See the item on track counting and internal braking for details.)
2. The LC78681KE becomes active when the $\overline{CS}$ pin is low, and data is output from the SQOUT pin. When the $\overline{CS}$ pin is high, the SQOUT pin goes to the high impedance state.

12. Level meter (LVM) data and peak meter (PKM) data readout

MSB LSB	Command	$\overline{RES}$ = low
0 0 1 0 1 0 1 1	PKM SET (LVM Reset)	
0 0 1 0 1 1 0 0	LVM SET (PKM Reset)	○
0 0 1 0 1 1 0 1	PKM MASK SET	
0 0 1 0 1 1 1 0	PKM MASK RESET	○

- Level meter (LVM)
  - — The LVM set (2CH) command sets the LC78681KE to LVM mode.
  - — LVM data is a 16-bit word in which the MSB indicates the L/R polarity and the low order 15 bits are absolute value data. A one in the MSB indicates left channel data and a zero indicates right channel data.
  - — LVM data is appended after the 80 bits of SubQ data, and can be read out from the SQOUT pin by applying 96 clock cycles to the CQCK pin. Each time LVM data is read out the left/right channel state is inverted. Data is held independently for both the left and right channels. In particular, the largest value that occurs between readouts for each channel is held.

- Peak meter (PKM)
  - — The PKM set (2BH) command sets the LC78681KE to PKM mode.
  - — PKM data is a 16-bit word in which the MSB is always zero and the low order 15 bits are absolute value data. This functions detects the maximum value that occurs in the data, whichever channel that value occurs in.
  - — PKM data is read out in the same manner as LVM data. However, data is not updated as a result of the readout operation.
  - — PKM mode SubQ data absolute time is computed by holding the absolute time (ATIME) detected after the maximum value occurred and sending that value. (Normal operation uses relative time.)
  - — It is possible to set the LC78681KE to ignore values larger than the already recorded value by issuing the PKM mask set command, even in PKM mode. This function is cleared by issuing a PKM mask reset command. (This is used in PK search in a memory track.)

13. Mute control circuit

MSB LSB	Command	$\overline{RES}$ = low
0 0 0 0 0 0 0 1	MUTE: 0 dB	
0 0 0 0 0 0 1 0	MUTE: −12 dB	
0 0 0 0 0 0 1 1	MUTE: ∞ dB	O

An attenuation of 12 dB (MUTE −12 dB) or full muting (MUTE ∞ dB) can be applied by issuing the appropriate command from the table. Since zero cross muting is used, there is no noise associated with this function. Zero cross is defined for this function as the top seven bits being all ones or all zeros.

14. Bilingual function

MSB LSB	Command	$\overline{RES}$ = low
0 0 1 0 1 0 0 0	STO CONT	O
0 0 1 0 1 0 0 1	Lch CONT	
0 0 1 0 1 0 1 0	Rch CONT	

- Following a reset or when a stereo (28H) command has been issued, the left and right channel data is output to the left and right channels respectively.
- When an Lch set (29H) command is issued, the left and right channels both output the left channel data.
- When an Rch set (2AH) command is issued, the left and right channels both output the right channel data.

15. De-emphasis on/off; Pin 29: EMPH

The preemphasis on/off bit in subcode Q control information is output from the EMPH pin. De-emphasis should be performed when this signal is high.

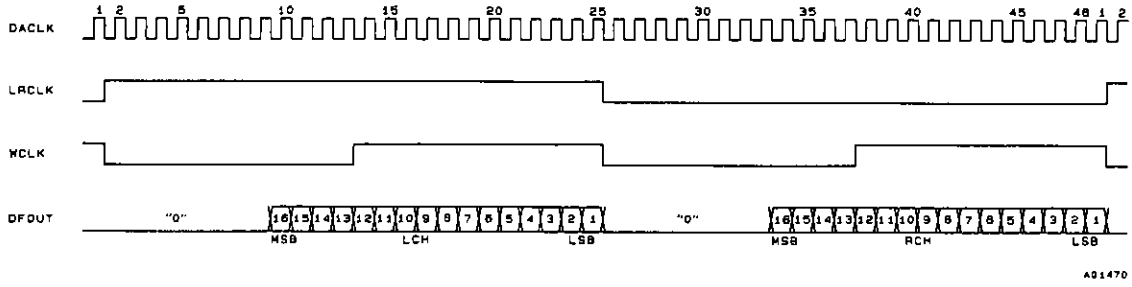
16. D/A converter interface; pin 31: WCLK, pin 33: LRCLK, pin 35: DFOUT, pin 36: DACLK
Data for the D/A converter is output MSB first from DFOUT synchronized with the falling edge of DACLK.

MSB LSB	Command	$\overline{RES}$ = low
1 0 0 0 1 0 0 0	CD-ROM XA	
1 0 0 0 1 0 1 1	CONT AND CD-ROM XA RESET	O

When the CD-ROM XA command described above is issued, data that is neither interpolated nor muted will be output from the DFOUT and DOUT pins. (This command is used for CD-ROM XA applications.) The CD-ROM XA reset command also functions as a pin 60 CONT reset, so caution is required.

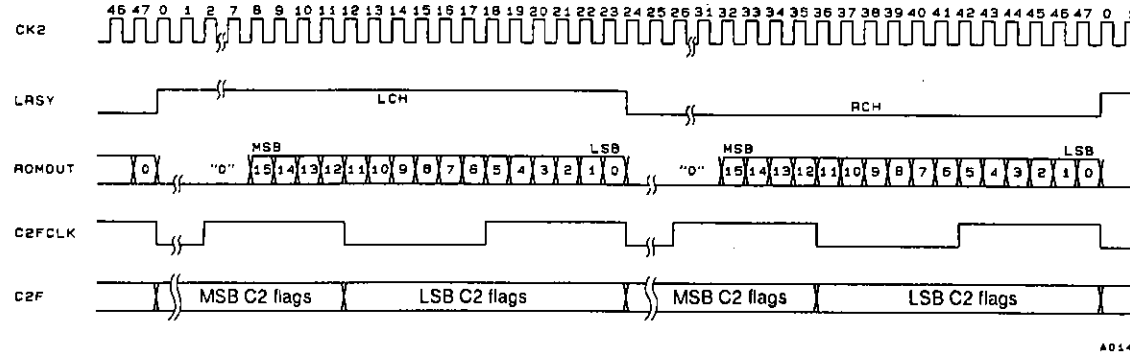
- LC78681KE D/A converter interface

DACLK = 2.1168MHz



17. CD-ROM outputs; Pin 39: CK2, pin 37: LRSY, pin 40: ROMOUT, pin 42: C2F, pin 41: C2FCLK
Data is output MSB first from the ROMOUT pin in synchronization with the LRSY signal. This data is appropriate for input to a CD-ROM LSI, since it is not interpolated, previous value held, or processed by the digital filter circuits. CK2 is a 2.1168 MHz clock, and data is output on the CK2 rising edge. C2F is the flag information for data in 8-bit units. C2FCLK is the synchronization signal for that flag.

Interface between the LC89510 and the LC78681KE or LC78681KE-L



18. Digital output circuit; Pin 43: DOUT

This is an output pin for use with a digital audio interface. Data is output in the EIAJ format. This signal has been processed by the interpolation and muting circuits. This pin has a built-in driver circuit and can directly drive a transformer.

MSB LSB	Command	$\overline{RES}$ = low
0 1 0 0 0 0 1 0	DOUT ON	O
0 1 0 0 0 0 1 1	DOUT OFF	
0 1 0 0 0 0 0 0	UBIT ON	O
0 1 0 0 0 0 0 1	UBIT OFF	

- The DOUT pin can be locked at the low level by issuing a DOUT OFF command.
- The UBIT information in the DOUT data can be locked at zero by issuing a UBIT OFF command.

19. CONT pin: Pin 60: CONT

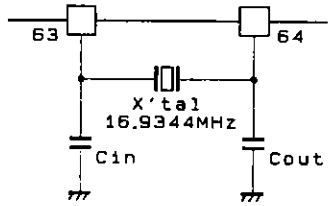
MSB LSB	Command	$\overline{RES}$ = low
0 0 0 0 1 1 1 0	CONT SET	Low
1 0 0 0 1 0 1 1	CONT AND CD-ROM XA RESET	O

The CONT pin goes high when a CONT SET command is issued.

20. Crystal clock oscillator; Pin 63: XIN, pin 64: XOUT

MSB LSB	Command	$\overline{RES}$ = low
1 0 0 0 1 1 1 0	OSC ON	O
1 0 0 0 1 1 0 1	OSC OFF	
1 1 0 0 0 0 0 1	DOUBLE SPEED MODE	
1 1 0 0 0 0 1 0	NORMAL MODE	O
0 1 1 0 0 0 0 0	VCO 8M	O
0 1 1 0 0 0 0 1	VCO 16M	

The clock that is used as the time base is generated by connecting a 16.9344 MHz crystal oscillator between these pins. The OSC OFF command turns off both the VCO and crystal oscillators. Also, the LC78681KE can be set up to handle double speed playback simply by issuing a command. The table below lists the relationships between the crystal and VCO oscillators.



VCO playback speed	Mode 8M		Mode 16M	
	Normal speed mode	Double speed mode	Normal speed mode	Double speed mode
When reset	O	—	—	—
AI pin external input (8M VCO)	8.6436 MHz			
AI pin external input (17M VCO)			17.2872 MHz	17.2872 MHz
AI pin external input (LA9210)	8.6436 MHz	17.2872 MHz		
PCK monitor output	4.3218 MHz	8.6436 MHz	4.3218 MHz	8.6436 MHz

Recommended crystal clock oscillator component values

Manufacturer	Oscillator	Cin/Cout
CITIZEN WATCH CO., LTD.	CSA-309 (16.9344 MHz)	6 pF to 10 pF (Cin = Cout)

21. 4.2M and 16M pins; Pin 59: 4.2M, pin 58: 16M

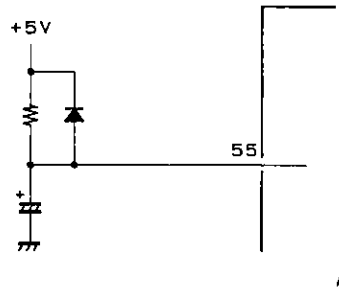
The 16.9344 MHz external crystal oscillator 16.9344 MHz buffer output signal is output from the 16M pin. That frequency divided by four (a 4.2336 MHz frequency) is output from the 4.2M pin. When the oscillator is turned off both these pins will be fixed at either high or low. These frequencies are not changed by issuing the double speed command.

22. Reset circuit; Pin 55: $\overline{\text{RES}}$

When power is first applied, this pin should be briefly set low and then set high. This will set the muting to $-\infty$ dB and stop the disk motor.

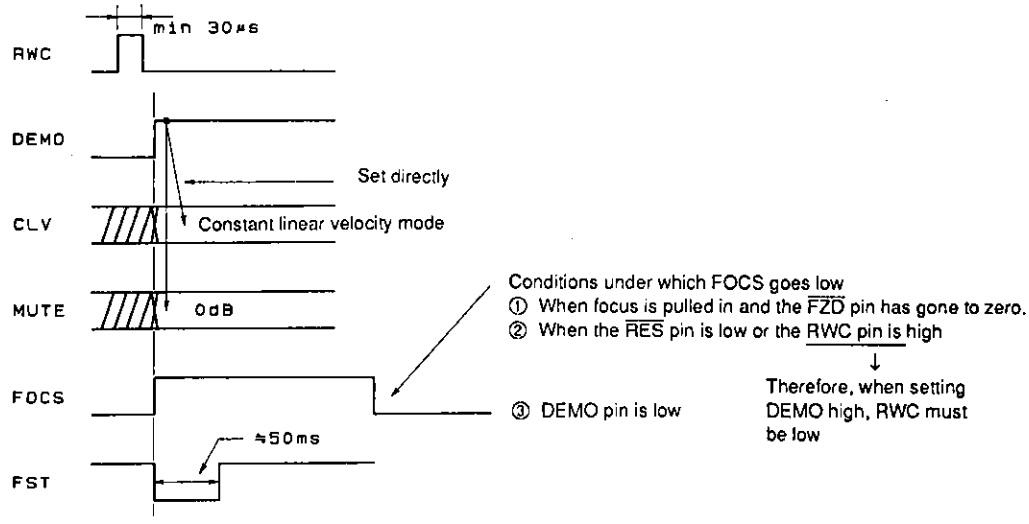
Constant linear velocity servo	START	**STOP**	BRAKE	CLV
Muting control	0 dB	−12 dB	**∞**	
Subcode Q address conditions	**Address 1**	Address free		
Laser control	ON (low)	**OFF**	(high)	
CONT	High	**Low**		
OSC	**ON**	OFF		
Track jump mode	**Former**	New		
Track count mode	Former	**New**		

Setting the $\overline{\text{RES}}$ pin low sets the LC78681KE to the settings enclosed in boxes in the table.



A01460

23. Adjustment process sound output function; Pin 27: DEMO



A01461

By setting this pin high, muting can be set to 0 dB, the disk motor can be set to CLV, and a focus start operation can be performed, even without issuing any commands from the control microprocessor. Also, since the $\overline{\text{LASER}}$ pin becomes active, if the mechanism and servo systems are complete, an EFM signal can be acquired with only this equipment, and an audio signal can be produced without the presence of a microprocessor.

24. Other pins; Pin 1: TEST1, pin 9: TEST2, pin 23: TEST3, pin 28: TEST4, pin 61: TEST5, pin 37: TEST6, pin 32: TEST7
    These pins are used for testing the LSI's internal circuits. Since the pins TEST1 to TEST5 have built-in pull-down resistors, they can be left open in normal operation.

Circuit Block Operating Descriptions

1. RAM address control
   The LC78681KE incorporates an 8-bit × 2 k-word RAM on chip. This RAM is used as a buffer memory, and has an EFM demodulated data jitter handling capacity of ±4 frames. The LC78681KE continuously checks the remaining buffer capacity and controls the data write address to fall in the center of the buffer capacity by making fine adjustments to the PCK side of the CLV servo circuit and the frequency divisor. If the ±4 frame buffer capacity is exceeded, the LC78681KE forcibly sets the write address to the ±0 position. However, since the errors that occur due to this operation cannot be handled with error flag processing, the IC applies muting to the output for a 128 frame period.

Position	Division ratio or processing	
–4 or less	Force to ±0	
–3	589	Increase ratio
–2	589	
–1	589	
±0	588	Standard ratio
+1	587	Decrease ratio
+2	587	
+3	587	
+4 or more	Force to ±0	

2. C1 and C2 error correction
   The EFM demodulated data is written to internal RAM to compensate for jitter, and the LC78681KE performs the following processing with a constant timing based on the crystal oscillator clock. First, the LC78681KE performs C1 error checking and correction in the C1 block, determines the C1 flags, and writes the C1 flag register. Next, the LC78681KE performs C2 error checking and correction in the C2 block, determines the C2 flags, and writes data to internal RAM.

C1 flag	Error correction and flag processing
No errors	No correction required · Flag reset
1 error	Correction · Flag reset
2 errors	Correction · Flag set
3 errors or more	Correction not possible · Flag set

C2 flag	Error correction and flag processing
No errors	No correction required · Flag reset
1 error	Correction · Flag reset
2 errors	Depends on C1*1
3 errors or more	Depends on C1*2

Note: 1. If the positions of the errors determined by the C2 check agree with the those specified by the C1 flags, the correction is performed and the flags are cleared. However, if the number of C1 flags is 7 or higher, C2 correction may fail. In this case correction is not performed and the C1 flags are taken as the C2 flags without change. Error correction is not possible if one error position agrees and the other does not. Furthermore, if the number of C1 flags is 5 or under, the C1 check result can be seen as unreliable. Accordingly, the flags will be set in this case. Cases where the number of C1 flags is 6 or more are handled in the same way, and the C1 flags are taken as the C2 flags without change. When there is not even one agreement between the error positions, error correction is, of course, impossible. Here, if the number of C1 flags was 2 or under, data that was seen as correct after C1 correction is now seen as incorrect data. The flags are set in this case. The other C1 flags are taken as the C2 flags without change.

2. When data is determined to have three or more errors and be uncorrectable, correction is, of course, impossible. Here, if the number of C1 flags was 2 or under, data that was seen as correct after C1 correction is now seen as incorrect data. The flags are set in this case. The other C1 flags are taken as the C2 flags without change.

Differences between the LC78681E and the LC78681KE/LC78681KE-L

1. New functions
   - CLV phase comparator divisor function (divisors of 2, 4, and 8)
   - CLV three state output
   - JP three state output

2. New commands
   - Command input

MSB	LSB	Command	$\overline{RES}$ = low	Function
1 1 1 0 1 1 1 1		COMMAND INPUT NOISE EXCLUSION MODE		Excludes noise from the $\overline{COCK}$ signal.
1 1 1 0 1 1 1 0		RESET NOISE EXCLUSION MODE (former product scheme)	○	

   - CLV servo

MSB	LSB	Command	$\overline{RES}$ = low	Function
1 0 1 1 0 0 0 1		CLV PHASE COMPARATOR DIVISOR: 1/2		The former product compared the phase for each 7.35 kHz cycle. A new frequency divisor function has been added.
1 0 1 1 0 0 1 0		CLV PHASE COMPARATOR DIVISOR: 1/4		
1 0 1 1 0 0 1 1		CLV PHASE COMPARATOR DIVISOR: 1/8		
1 0 1 1 0 0 0 0		NO CLV PHASE COMPARATOR DIVISOR USED (former product scheme)	○	
1 0 1 1 0 1 0 0		CLV THREE STATE OUTPUT MODE		CLV servo can be controlled from a single pin since a three state output function has been added to the CLV⁺ pin (and to the CLV⁻ pin as well).
1 0 1 1 0 1 0 1		RESET THREE STATE OUTPUT MODE (former product scheme)	○	

   - Track jump

MSB	LSB	Command	$\overline{RES}$ = low	Function
1 0 1 1 0 1 1 0		JP THREE STATE OUTPUT		The track jump function can be controlled from a single pin since a three state output function has been added to the JP⁺ pin (and to the JP⁻ pin as well).
1 0 1 1 0 1 1 1		RESET THREE STATE OUTPUT MODE (former product scheme)	○	
0 1 0 1 0 0 1 0		1 TRACK JUMP IN #4		TOFF is set low during the track jump "c" period.
0 1 0 1 1 0 1 0		1 TRACK JUMP OUT #4		
0 0 1 0 0 0 0 1		THLD PERIOD TOFF OUTPUT MODE		TOFF is set high during the track jump THLD period.
0 0 1 0 0 0 0 0		RESET THLD PERIOD TOFF OUTPUT MODE (former product scheme)	○	

   - Internal brake mode

MSB	LSB	Command	$\overline{RES}$ = low	Function
1 1 0 0 1 0 1 1		INTERNAL BRAKE CONTINUOUS MODE		The LC78681KE remains in continuous brake operation mode even after WRQ goes high.
1 1 0 0 1 0 1 0		RESET CONTINUOUS MODE (former product scheme)	○	
1 1 0 0 1 1 0 1		TOFF OUTPUT DISABLED MODE		TOFF goes low during internal brake operation.
1 1 0 0 1 1 0 0		RESET TOFF OUTPUT DISABLED MODE (former product scheme)	○	

3. Changed specification
   - The "c" periods (braking periods) during track jump operations have all been changed from 24 ms to 60 ms.