

| | | |
|--------------------------------------|------------|---------------|
| SANYO | No. ※4834A | DM0811 |
| LCD Dot Matrix Display Module | | |

Preliminary

Overview

The DM0811 is an LCD dot matrix display module that consists of an LCD panel and a controller/driver. It can display one line of eight characters. The DM0811 includes the data RAM, character generator ROM and control circuits required for display. Both 8-bit parallel and 4-bit parallel data interfaces are supported and data can be directly written and read by the controlling microprocessor.

General Specifications

- Drive method: 1/8 duty – 1/4 bias
- Display size: 8 characters by 1 line
- Character structure: 5 by 7 dots plus cursor display
- Display data RAM capacity: 80 characters (8 bits each)
- CG ROM capacity: 192 characters (See the description of the built-in character generator.)
- CG RAM capacity: 8 characters (64 by 8 bits)
- Instruction functions: 11 instructions (See the description of the instruction function.)
- Circuit structure: See the block diagram.

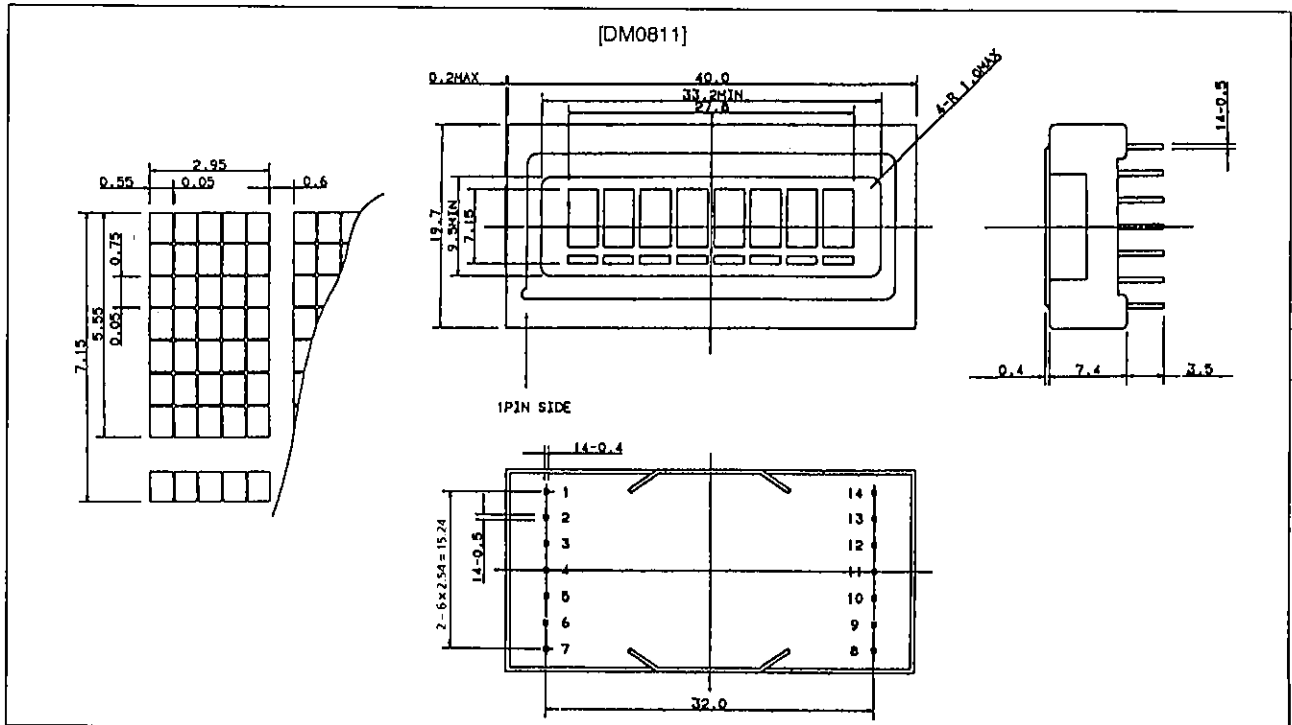
Physical Specifications

- Module dimensions (mm): 40.0 (W) x 19.7 (H) x 7.4 (T)
- Effective display area (mm): 33.2 (W) x 9.5 (H)
- Dot pitch (mm): 0.60 (W) x 0.80 (H)
- Dot size (mm): 0.55 (W) x 0.75 (H)
- Weight (g): approx. 9.0

Module Dimensions

(unit: mm)

5012



Module Options

DM0811-□△

(□: First digit) LCD Characteristics

(△: Second digit)

| | LCD type | LCD operating temperature | Power supply specifications | Viewing angle direction |
|---|----------|---------------------------|-----------------------------|-------------------------|
| 0 | TN | 0 to 50°C | Single-voltage supply | 6 H |
| 1 | TN | 0 to 50°C | Single-voltage supply | 12 H |

| | LCD mode CD |
|---|-----------------------|
| S | Positive, reflective |
| B | Positive, transparent |

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$, $V_{DD} - V_{SS} = 5 \pm 0.25\text{ V}$

| Parameter | Symbol | Ratings | Unit |
|----------------------------|-------------------|------------------------|------|
| Logic power supply voltage | $V_{DD} - V_{SS}$ | -0.3 to +7.0 | V |
| LCD power supply voltage | $V_{DD} - V_O$ | -0.3 to +13.5 | V |
| Input voltage | V_I | -0.3 to $V_{DD} + 0.3$ | V |
| Operating temperature | T_{opr} | 0 to +50 | °C |
| Storage temperature | T_{stg} | -20 to +70 | °C |

Electrical and Optical Characteristics at $T_a = 25^\circ\text{C}$, $V_{DD} - V_{SS} = 5 \pm 0.25\text{ V}$

| Parameter | Symbol | Conditions | min | typ | max | Unit | Note | |
|--|-----------------------|-----------------------------|--------------------------|-----|----------|------|-----------------|-----------------|
| Input high-level voltage | V_{IH} | | 2.2 | | V_{DD} | V | | |
| Input low-level voltage | V_{IL} | | 0 | | 0.6 | V | | |
| Output high-level voltage | V_{OH} | $I_{OH} = 0.2\text{ mA}$ | 2.4 | | V_{DD} | mA | | |
| Output low-level voltage | V_{OL} | $I_{OL} = 1.2\text{ mA}$ | 0 | | 0.4 | mA | | |
| Current drain | I_{DD} | | | 1.5 | 3.0 | mA | | |
| [TN type, normal temperature range specifications] | | | | | | | | |
| LCD drive voltage | $V_{DD} - V_O$ | $T_a = 0^\circ\text{C}$ | 3.7 | 3.8 | 3.9 | V | 1 | |
| | | $T_a = 25^\circ\text{C}$ | 3.4 | 3.5 | 3.6 | V | | |
| | | $T_a = 50^\circ\text{C}$ | 2.7 | 2.8 | 2.9 | V | | |
| Response time | Reset time | $t_r, \theta = 0^\circ$ | $T_a = 0^\circ\text{C}$ | | 200 | 300 | ms | Figures 1 and 2 |
| | | | $T_a = 25^\circ\text{C}$ | | 60 | 100 | ms | |
| | Fall time | $t_f, \theta = 0^\circ$ | $T_a = 0^\circ\text{C}$ | | 300 | 450 | ms | |
| | | | $T_a = 25^\circ\text{C}$ | | 100 | 150 | ms | |
| Contrast ratio | K | $\theta = 0^\circ$ | 5 | 10 | | | Figures 2 and 3 | |
| Viewing angle range | $\theta_2 - \theta_1$ | $\theta = 0^\circ, K > 1.4$ | 30 | 40 | | deg | Figures 2 and 3 | |

Note: 1. The contrast provided by an LCD display varies greatly with the angle of view.

An LCD drive voltage appropriate for the actual product must be used.

The indicated values are reference values only. Please contact your Sanyo representative before using this product.

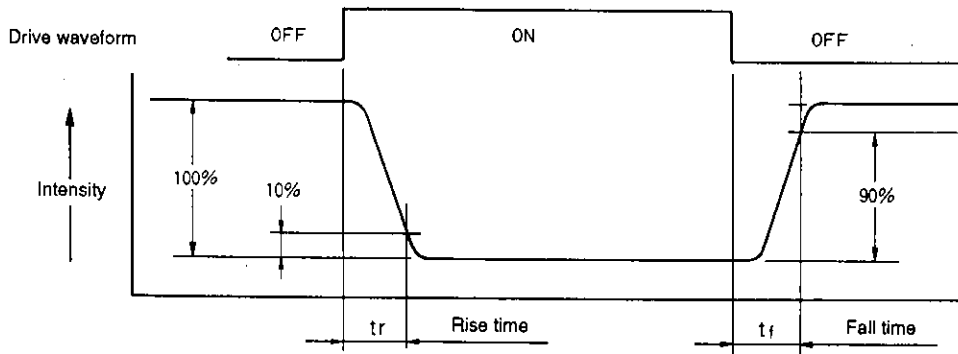


Figure 1 Response Time Definitions

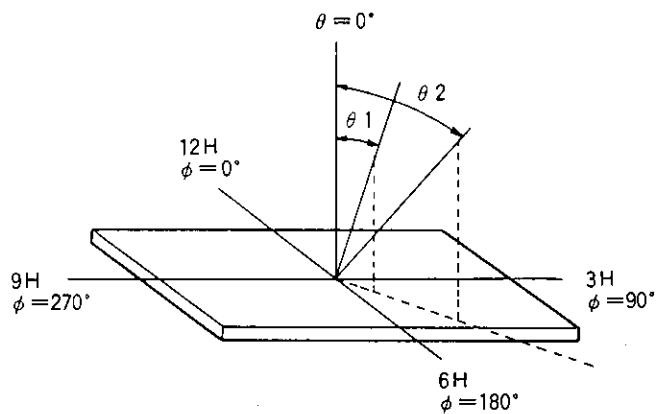


Figure 2 Definition of Angles θ and ϕ

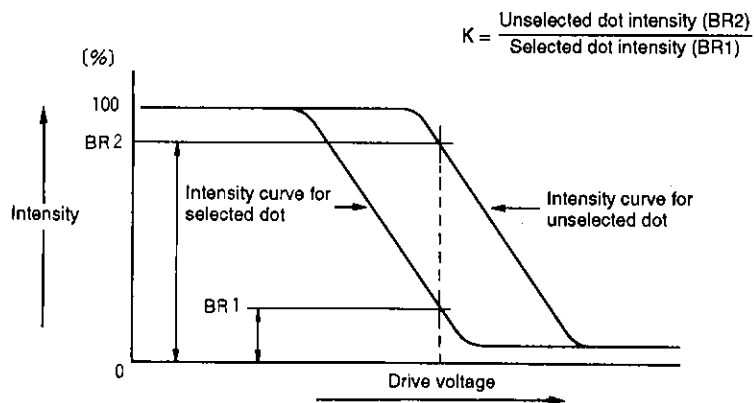
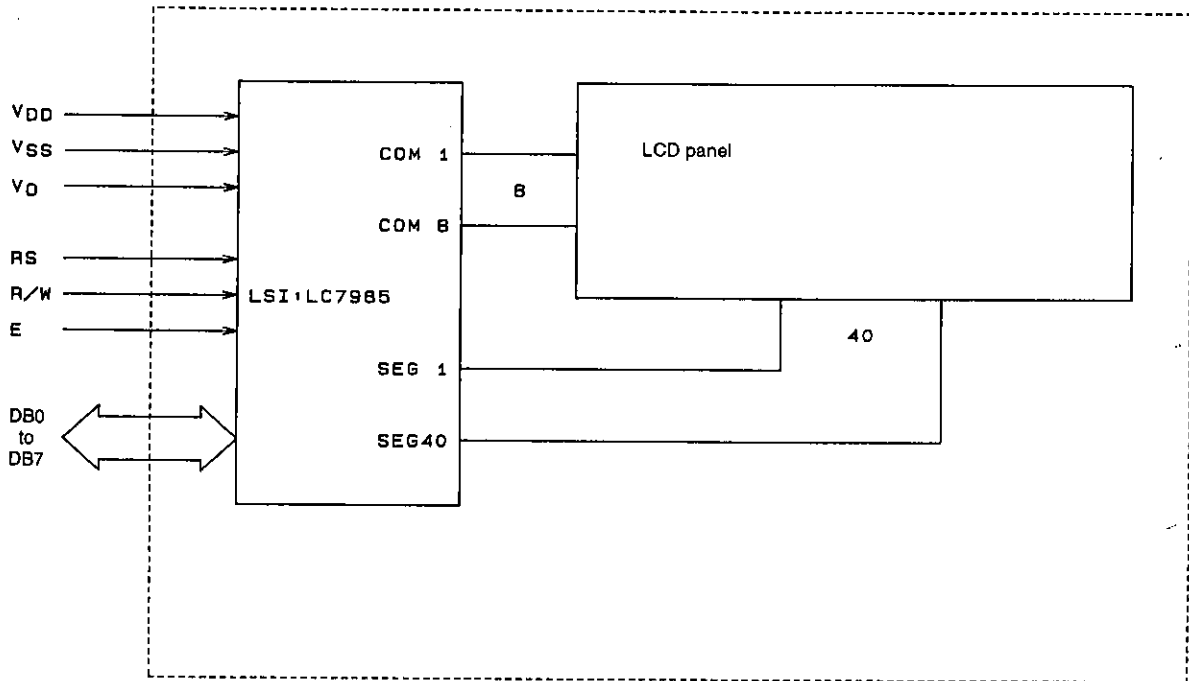


Figure 3 Definition of Contrast Ratio

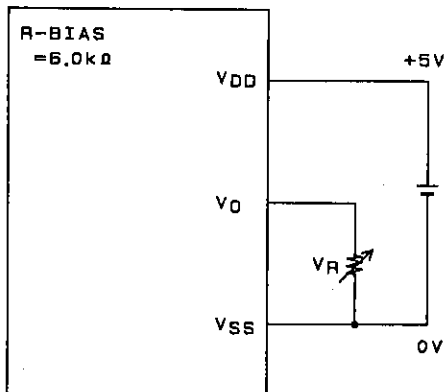
Block Diagram



A02273

Power Supply Circuit Examples

Normal temperature range circuit
(Single voltage supply specifications)

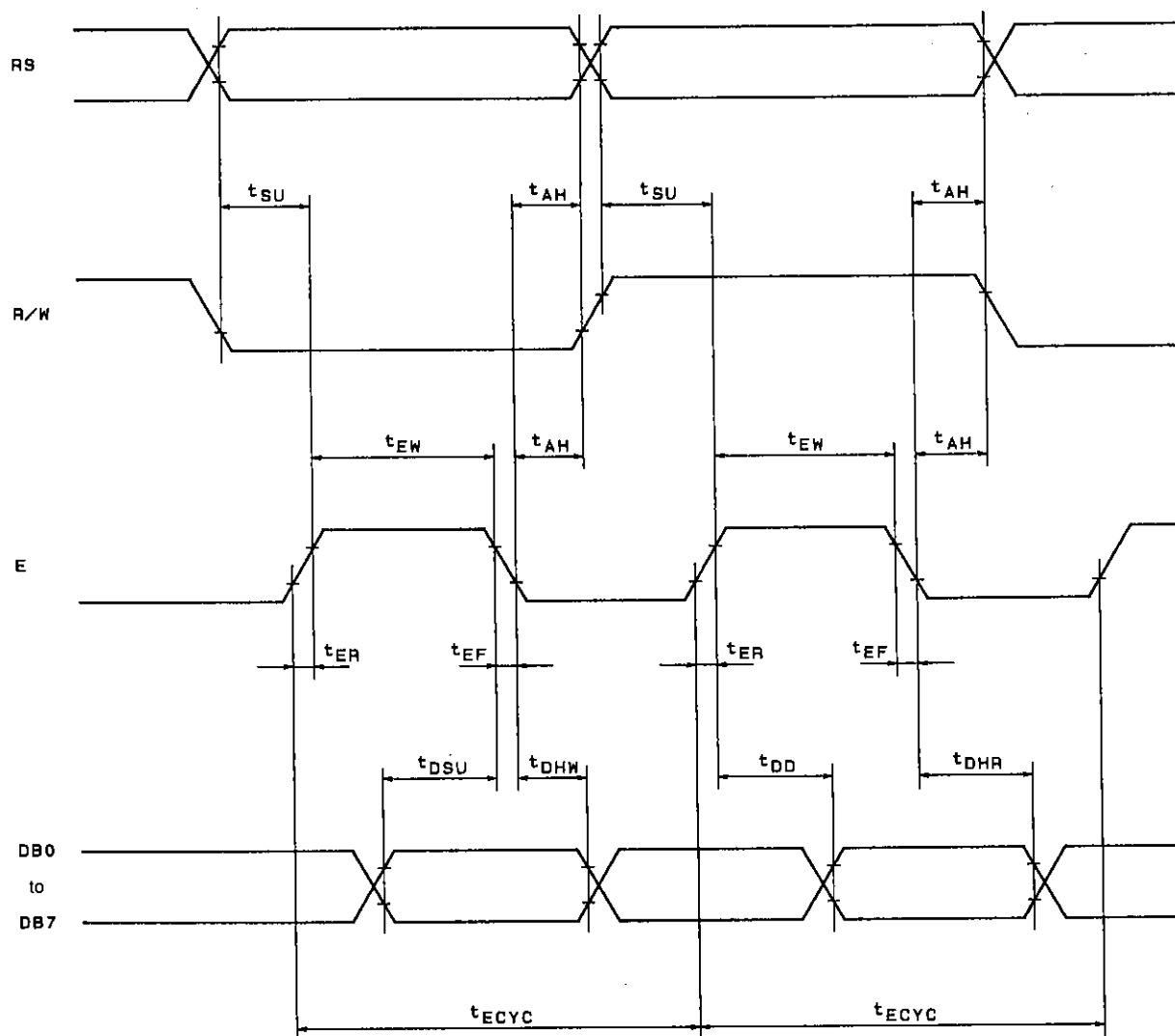


Note: When VR is 5 kΩ, the LCD drive voltage will be variable over the range 2.7 to 5.0 V.

Timing Characteristics at $T_a = 25^\circ\text{C}$, $V_{DD} - V_{SS} = 5 \pm 0.25\text{ V}$

| Parameter | Symbol | min | typ | max | Unit |
|--------------------|------------|------|-----|-----|------|
| Enable cycle time | t_{ECYC} | 1000 | | | ns |
| Enable pulse width | t_{WE} | 450 | | | ns |
| Enable rise time | t_{ER} | | | 25 | ns |
| Enable fall time | t_{EF} | | | 25 | ns |
| Setup time | t_{SU} | 140 | | | ns |
| Address hold time | t_{AH} | 10 | | | ns |
| Data setup time | t_{DSU} | 195 | | | ns |
| Data hold time | t_{DHW} | 10 | | | ns |
| Data delay time | t_{DD} | | | 320 | ns |
| Data hold time | t_{DHR} | 20 | | | ns |

Write and Read Operations



A02272

Interface Pin Connections

| Pin No. | Symbol | Function |
|---------|-----------------|---|
| 1 | V _{SS} | Ground (0 V) |
| 2 | V _{DD} | +5 V |
| 3 | V _O | LCD drive power supply |
| 4 | RS | Register selection pin 0: Instruction register (write) Busy flag, address counter (read) 1: Data register (write or read) |
| 5 | R/W | Read/write pin 0: Write Microprocessor → LCD module 1: Read LCD module → microprocessor |
| 6 | E | Enable |
| 7 | DB0 | Data bus (tristate bidirectional connections) Used as the lower 4 bits when an 8-bit interface is used. Unused when a 4-bit interface is used. |
| 8 | DB1 | |
| 9 | DB2 | |
| 10 | DB3 | |
| 11 | DB4 | Data bus (tristate bidirectional connections) Used as the upper 4 bits when an 8-bit interface is used. Used as the data bus itself when a 4-bit interface is used. DB7 is also used as the busy flag. |
| 12 | DB5 | |
| 13 | DB6 | |
| 14 | DB7 | |

Note: This module is designed so that it can be used with either a 4-bit or an 8-bit microprocessor. In four-bit mode, data is transferred in two 4-bit operations, and in 8-bit mode data is transferred in a single 8-bit operation.

CG ROM: Built-in character generator

| Lower 4 bits \ Upper 4 bits | 0000 | 0010 | 0011 | 0100 | 0101 | 0110 | 0111 | 1010 | 1011 | 1100 | 1101 | 1110 | 1111 |
|-----------------------------|------------|------|------|------|------|------|------|------|------|------|------|------|------|
| xxxx0000 | CG RAM (1) | | o | a | P | ^ | P | - | o | e | | o | P |
| xxxx0001 | (2) | ! | l | A | Q | a | q | u | 7 | 7 | u | a | q |
| xxxx0010 | (3) | " | 2 | B | R | b | r | f | f | u | u | p | e |
| xxxx0011 | (4) | # | 3 | C | S | c | s | j | 7 | 7 | e | e | e |
| xxxx0100 | (5) | \$ | 4 | D | T | d | t | . | l | l | + | p | a |
| xxxx0101 | (6) | % | 5 | E | U | e | u | . | + | + | l | e | o |
| xxxx0110 | (7) | & | 6 | F | V | f | v | 7 | 7 | u | e | p | z |
| xxxx0111 | (8) | ' | 7 | G | W | g | w | 7 | + | 7 | 7 | g | π |
| xxxx1000 | (1) | (| 8 | H | X | h | x | 4 | o | 7 | u | 7 | x |
| xxxx1001 | (2) |) | 9 | I | Y | i | y | 7 | 7 | u | u | 7 | y |
| xxxx1010 | (3) | * | : | J | Z | j | z | 7 | 7 | u | u | j | 7 |
| xxxx1011 | (4) | + | ; | K | L | k | l | 7 | 7 | u | u | * | 7 |
| xxxx1100 | (5) | , | < | L | # | l | l | 7 | 7 | u | u | o | 7 |
| xxxx1101 | (6) | - | = | M | I | m | i | 7 | 7 | u | u | 7 | + |
| xxxx1110 | (7) | . | > | N | ^ | n | + | 7 | 7 | u | u | 7 | |
| xxxx1111 | (8) | / | ? | O | _ | o | + | u | y | 7 | 7 | o | |

Instruction Function

| Instruction | Code | | | | | | | | | | | Function | Execution time (when $f_{OSC} = 250$ kHz) |
|------------------------------|---|-----|------------|-----------------|-----------------|-----|-----|-----|-----------------------------------|--|--|--|---|
| | RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | | | |
| Display clear | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Clears the whole display and sets the address counter to DD RAM location 0. | 1.64 ms |
| Cursor home | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | * | Sets the address counter to DD RAM location 0. The shifted display also returns to its original position. The contents of DD RAM is not changed. | 1.64 ms |
| Entry mode set | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | I/D | S | Sets the cursor advance direction and whether or not the display is shifted. These operations are performed on data write and data read. | 40 μ s |
| Display on/off control | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | C | B | Sets the whole display on/off state (D), the cursor on/off state (C) and whether or not the character at the cursor position blinks (B). | 40 μ s |
| Cursor/display off | 0 | 0 | 0 | 0 | 0 | 1 | S/C | R/L | * | * | | Moves the cursor and shifts the display without changing the contents of DD RAM. | 40 μ s |
| Set function | 0 | 0 | 0 | 0 | 1 | DL | N | F | * | * | | Sets the interface data length (DL), the number of display lines (N) and the font (F). | 40 μ s |
| Set CG RAM address | 0 | 0 | 0 | 1 | A _{CG} | | | | | | Sets the CG RAM address. The data transmitted after this instruction is CG RAM data. | 40 μ s | |
| Set DD RAM address | 0 | 0 | 1 | A _{DD} | | | | | | Sets the DD RAM address. The data transmitted after this instruction is DD RAM data. | 40 μ s | | |
| Read busy flag/address | 0 | 1 | BF | AC | | | | | | Reads out the contents of the address counter and the busy flag (BF), which indicates whether or not an internal operation is in progress. | 0 μ s | | |
| Write CG RAM/ DD RAM data | 1 | 0 | Write data | | | | | | Writes data to CG RAM or DD RAM. | 40 μ s | | | |
| Read CG RAM/ DD RAM data | 1 | 1 | Read data | | | | | | Reads data from CG RAM or DD RAM. | 40 μ s | | | |
| | I/D = 1: Increment, I/D = 0: Decrement S = 1: Also shift display. S/C = 1: Shift display, S/C = 0: Move cursor R/L = 1: Right shift, R/L = 0: Left shift DL = 1: 8 bit mode, DL = 0: 4 bit mode N = 1: 2 row, N = 0: 1 row F = 1: 5 x 10 dot, F = 0: 5 x 7 dot BF = 1: Internal operation in progress, BF = 0: Instruction accepted | | | | | | | | | | | DD RAM: Display data RAM CG RAM: Character generator RAM A _{CG} : CG RAM address A _{DD} : DD RAM address AC: Address counter. The AC is used for both DD RAM and CG RAM. | The execution times will change if the frequency is changed. (Example) When $f_{OSC} = 270$ kHz $40 \mu s \times \frac{250}{270} = 37 \mu s$ |

Note: * Invalid bit.

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