

SANYO	No. 1860A	DM161B
		LIQUID CRYSTAL DOT MATRIX DISPLAY MODULE 16 characters x 1 line

General Description

The DM161B is a liquid crystal dot matrix display module that consists of LCD panel LCD-5013, LCD control driver HD44780 is capable of providing (16 characters x 1 line) display. It contains a controller, a data RAM, and a character generator ROM required for providing display. Data interfacing is in 8-bit parallel or 4-bit parallel and data can be written in or read from a microprocessor.

General Specifications

<ol style="list-style-type: none"> 1. Display system 2. Display content 3. Dots organizing 1 character 4. Display data RAM 5. Character generator ROM 6. Character generator RAM 7. Instruction function 8. Circuit diagram 	1/5bias 1/16duty 16 characters x 1 line 5 x 7 dots/character + cursor 80 x 8 bits 160-character JIS font set + 32-character special font set Refer to Table 1. 64 x 8 bits 5 x 7 dots 8 characters Refer to Table 2. Refer to Fig. 3.
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Outline

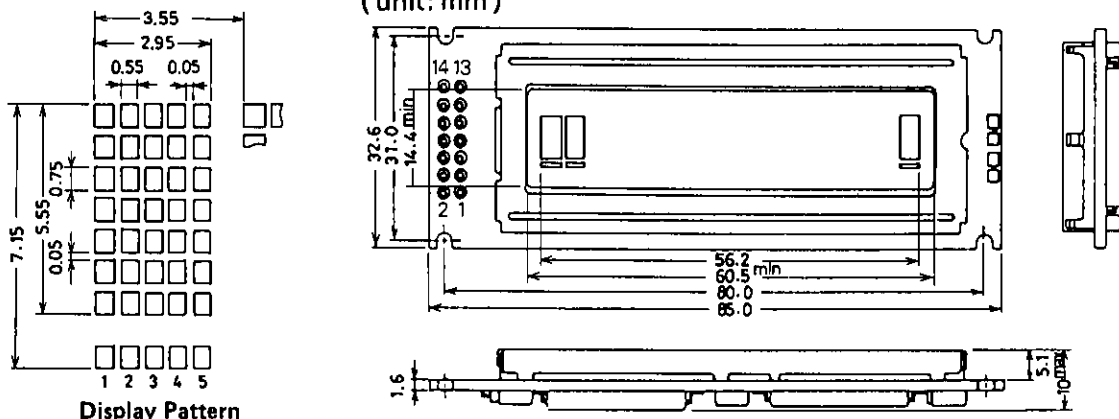
<ol style="list-style-type: none"> 1. Module outline 2. View area 3. Dot size 4. Dot pitch 5. Character size 	32.6(W) x 85.0(L) x 10(T) (mm) 60.5 x 14.4 (mm) 0.55 x 0.75 (mm) 0.60 x 0.80 (mm) 2.95 x 5.55 (mm)
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Absolute Maximum Ratings/T_a=25°C

			unit
Supply Voltage	V _{DD} -V _{SS}	-0.3 to +7	V
Input Voltage	V _I	-0.3 to V _{DD} +0.3	V
Drive Voltage	V _{DD} -V _O	-0.3 to +13.5	V
Operating Temperature	T _{opr.}	0 to 50	°C
Storage Temperature	T _{stg}	-20 to 60	°C

Module Dimensions 5002A

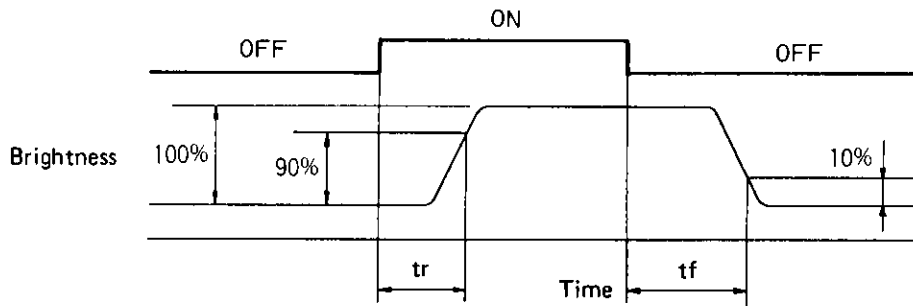
(unit: mm)



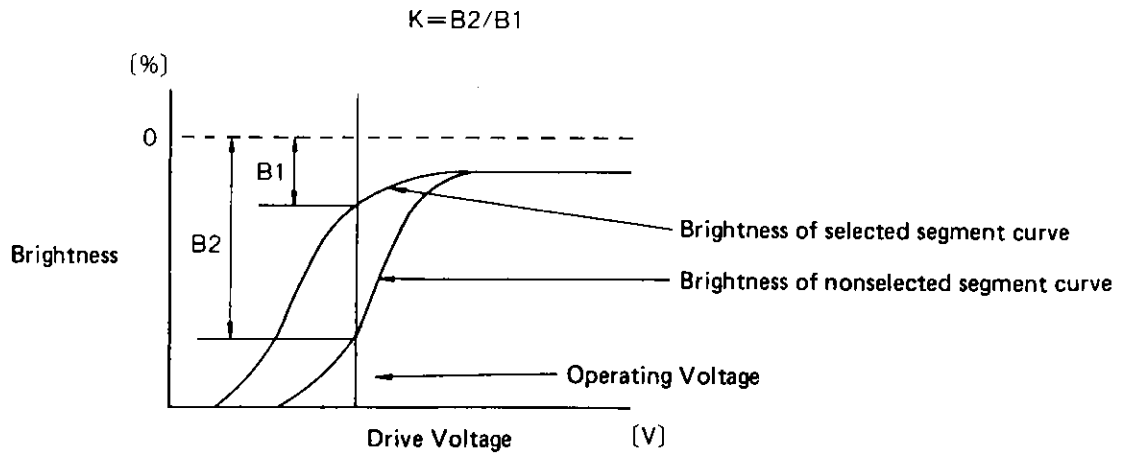
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Electro-optical Characteristics/V _{DD} =5.0V, T _a =25°C V _{SS} =0V unless otherwise specified		min	typ	max	unit
Input "High" Voltage	V _{IH}	2.2		5.0	V
Input "Low" Voltage	V _{IL}	0		0.6	V
Output "High" Voltage	V _{OH}	2.4	DB0 to DB7, -I _{OH} =0.2mA I _{OH} =40μA		V
Output "Low" Voltage	V _{OL}		DB0 to DB7, -I _{OL} =1.2mA	0.4	V
Input Current	I _p	50	Pull-up MOS V _{DD} =5V	125	250 μA
Current Dissipation	I _{DD}		No input/output current included	(1.2)	2.5 mA
Oscillation Frequency	F _{OSC}	190		270	350 kHz
Viewing Angle	φ ₂ - φ ₁	K=1.4	θ = 0°		20 degree
Contrast Ratio	K	3.0	φ = 20° θ = 0°		
Rise Time	t _r		φ = 20° θ = 0°	150	250 ms
Fall Time	t _f		φ = 20° θ = 0°	150	250 ms
LCD Drive Voltage	V _{DD} -V _O	4.2	T _a =0°C φ=20°, θ=0°, K≅3	4.3	4.4 V
(Recommend Value)	V _{DD} -V _O	3.8	T _a =25°C " " "	3.9	4.0 V
1/16 duty	V _{DD} -V _O	3.4	T _a =50°C " " "	3.5	3.6 V

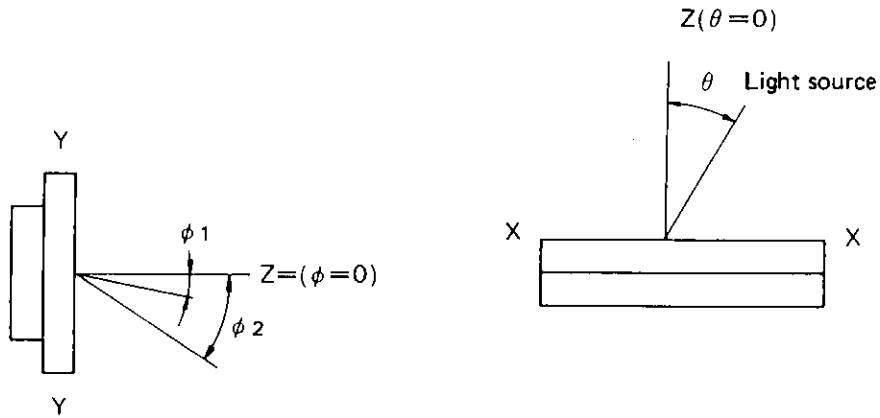
(1) Test Condition for Response Time (t_r, t_f)



(2) Definition of Contrast (K)



(3) Contrast Ratio Measuring Method



Angles ϕ and θ are defined shown above.

The light source is placed in the θ direction at an angle of 30° and the sensor is placed in the ϕ direction to measure the contrast.

Pin Description

No.	Pin Name	Function
1	VSS	(-) power supply pin 0V
2	VDD	(+) power supply pin +5V
3	VO	Pin for applying LCD drive voltage
4	RS	Input pin HI=Data LOW=Instruction
5	R/W	Input pin HI=Read LOW=Write
6	E	Input pin Enable signal
7	DB0	Data bus line
8	DB1	
9	DB2	
10	DB3	
11	DB4	
12	DB5	
13	DB6	
14	DB7	

Note 1. The LCD drive voltage can be varied from 3V to 5V by a variable resistor of 5kohm connected across VSS and VO.

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Timing Characteristics

			min	typ	max	unit
Enable Cycle Time		t_{cycE}	1000			ns
Enable Pulse Width	High level	P_{WEH}	450			ns
Enable Rise/Fall Time		t_{Er}, t_{Ef}			25	ns
Set Up Time	RS/RW-E	t_{As}	140			ns
Address Hold Time		t_{AH}	10			ns
Data Delay Time		t_{DDR}			320	ns
Data Set Up Time		t_{DSW}	195			ns
Data Hold Time		$t_H(t_{DHR})$	10(20)			ns

Figs. 1, 2

Write Operation

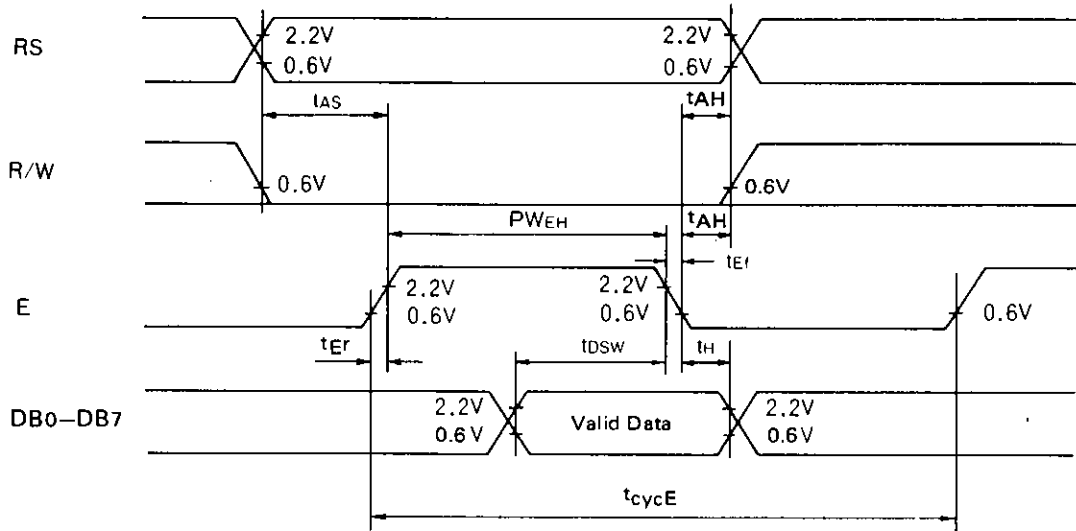


Fig. 1 Interface Timing (Data Write)

Read Operation

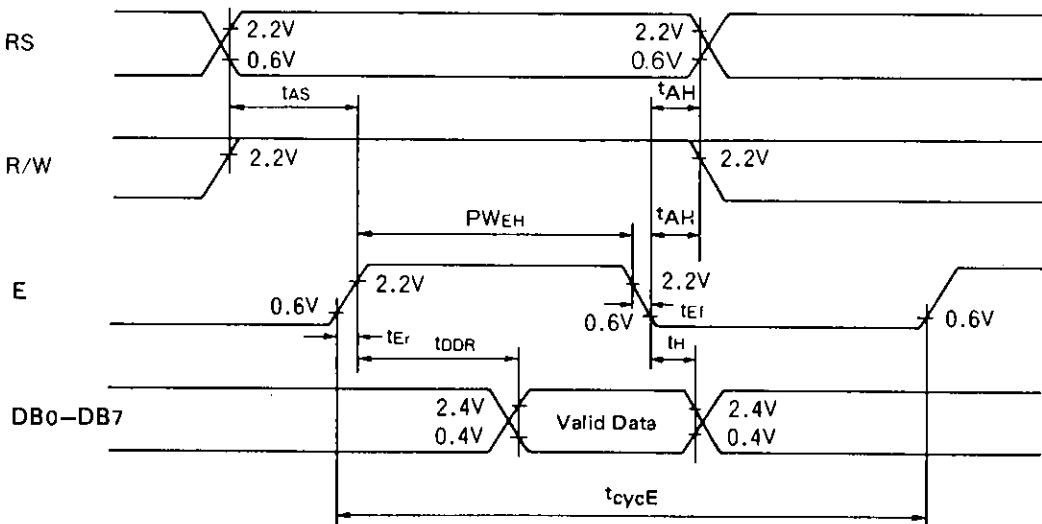


Fig. 2 Interface Timing (Data Read)

Table 1 Character code

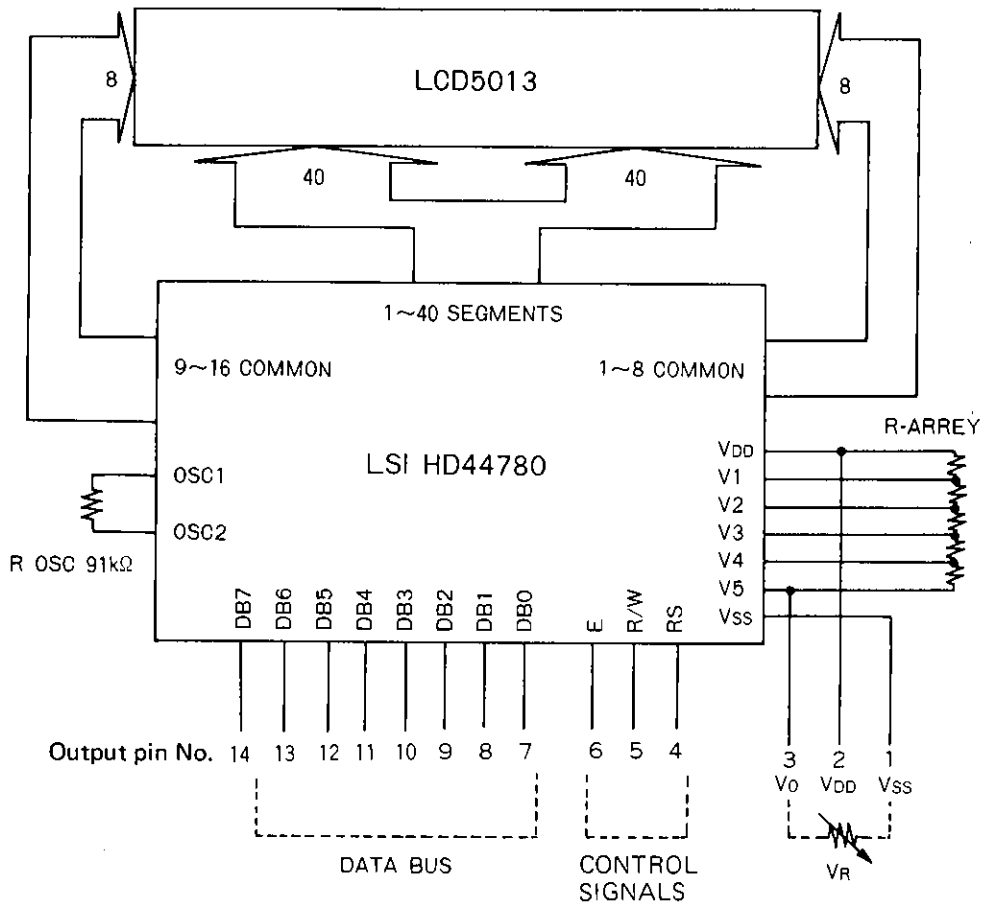
Hi-order Low-order 4bit	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)		0	a	P	'	P	-	9	E	e	P	
xxxx0001	(2)	!	1	A	O	a	9	e	7	+	4	a	q
xxxx0010	(3)	"	2	B	R	b	r	'	4	W	W	P	e
xxxx0011	(4)	#	3	C	S	c	s	u	0	7	E	e	e
xxxx0100	(5)	\$	4	D	T	d	t	,	I	t	P	P	a
xxxx0101	(6)	%	5	E	U	e	u	.	7	+	1	e	u
xxxx0110	(7)	&	6	F	V	f	v	7	0	2	a	P	Z
xxxx0111	(8)	'	7	G	W	g	w	7	+	7	7	g	π
xxxx1000	(1)	(8	H	X	h	x	4	0	*	U	J	X
xxxx1001	(2))	9	I	Y	i	y	9	7	U	U	'	y
xxxx1010	(3)	*	:	J	Z	j	z	z	3	0	U	J	+
xxxx1011	(4)	+	:	K	L	k	l	7	7	E	0	*	π
xxxx1100	(5)	,	<	L	*	l	l	7	9	7	7	e	π
xxxx1101	(6)	-	=	M	I	m	i	3	7	7	7	t	+
xxxx1110	(7)	.	>	N	^	n	+	3	E	7	7	n	
xxxx1111	(8)	/	?	0	_	o	+	w	y	7	7	o	π

(Note) The CG RAM is a character generator RAM used to store the character patterns that can be program-rewritten, as desired, by the user.

Table 2 Instruction function

Instruction	Code										Contents	Execution Time (f _{OSC} =250kHz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Display clear	0	0	0	0	0	0	0	0	0	1	Clears all display and returns the cursor to the home position (address 0).	82μs ~ 1.64ms
Cursor home	0	0	0	0	0	0	0	0	0	1 *	Returns the cursor to the home position (address 0). Also returns the display being shifted to the original position. The DD RAM contents remain unaffected.	40μs ~ 1.6ms
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Sets the cursor move direction and specifies whether or not to shift the display. These operations are performed during data write and read.	40μs
Display ON/OFF control	0	0	0	0	0	0	1	D	C	B	Sets all display ON/OFF(D), cursor ON/OFF(C), cursor position character blink (B).	40μs
Cursor/display shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves the cursor and shifts the display without affecting the DD RAM contents.	40μs
Function set	0	0	0	0	1	DL	N	F	*	*	Sets the interface data length (DL), number of display lines (L), and character font (F).	40μs
CG RAM address set	0	0	0	1	A _{CG}					Sets the CG RAM address. RAM data is sent/received after this setting.		40μs
DD RAM address set	0	0	1	A _{DD}					Sets the DD RAM address. DD RAM data is sent/received after this setting.		40μs	
Busy flag/ address read	0	1	BF	AC					Reads the contents of busy flag (BF) indicating internal operation is in progress and reads the contents of address counter.		1μs	
CG RAM/DD RAM data write	1	0	Write Data					Writes data into the DD RAM or CG RAM.		40μs		
CG RAM/DD RAM data read	1	1	Read Data					Reads data from the DD RAM or CG RAM.		40μs		
	I/D = 1 : Increment (+1) I/D = 0 : Decrement (-) S = 1 : Accompanied by display shift S/C = 1 : Display shift S/C = 0 : Cursor move R/L = 1 : Right-shift R/L = 0 : Left-shift DL = 1 : 8 bits DL = 0 : 4 bits N = 1 : 2 lines N = 0 : 1 line F = 1 : 5 x 10 dots F = 0 : 5 x 7 dots BF = 1 : Internally operating BF = 0 : Possible to accept instruction										DD RAM : Display data RAM CG RAM : Character generator RAM A _{CG} : CG RAM address A _{DD} : DD RAM address Corresponds to cursor address. AC : Address counter used for both DD RAM and CG RAM.	The change in the frequency (f _{OSC}) also causes the execution time to be changed. (Example) When f _{OSC} =270kHz, 40μs x 250/270 = 37μs.

Fig. 3 Circuit Diagram DM161B



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