Ordering number : EN5252

CMOS LSI

SANYO No. 5252

LC75824E, 75824W

1/4-Duty General-Purpose LCD Display Driver

Overview

The LC75824E and LC75824W are general-purpose LCD display drivers that can be used for frequency display in microprocessor-controlled radio receivers and in other display applications. In addition to being able to directly drive up to 204 LCD segments, the LC75824E and LC75824W can also control up to 12 general-purpose output ports.

Features

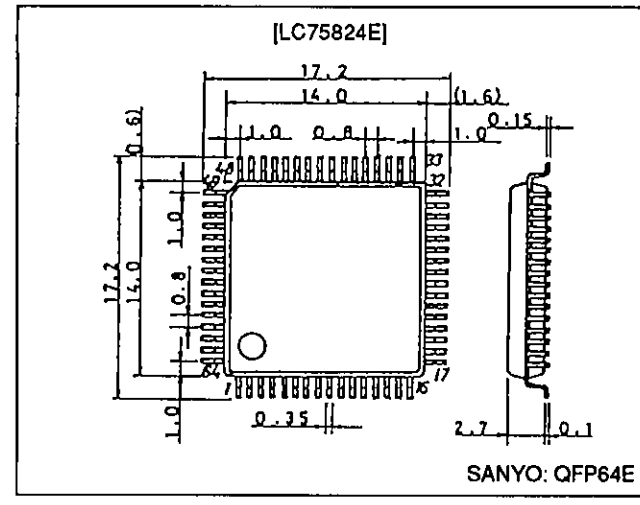
- Support for 1/4-duty 1/2-bias or 1/4-duty 1/3-bias drive of up to 204 segments under serial data control
- Serial data input supports CCB* format communication with the system controller.
- Serial data control of the power-saving mode based backup function and all the segments forced off function
- Serial data control of switching between the segment output port and general-purpose output port functions
- Serial data control of the normal mode current drain
- High generality since display data is displayed directly without decoder intervention.
- The $\overline{\text{INH}}$ pin can force the display to the off state.
- RC oscillator circuit

• CCB is a trademark of SANYO ELECTRIC CO., LTD.
• CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.

Package Dimensions

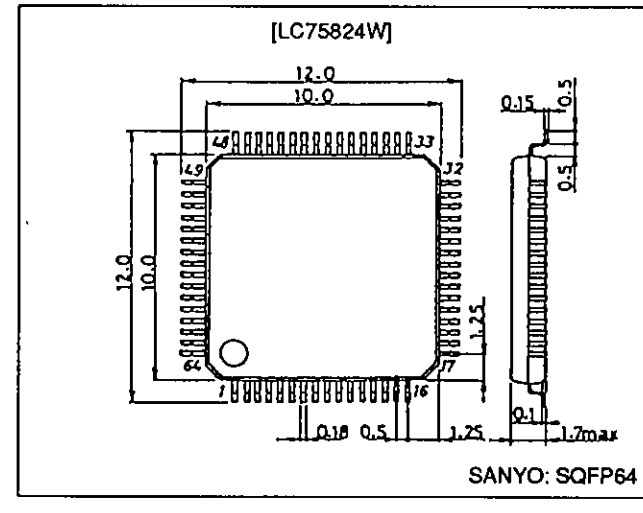
unit: mm

3159-QFP64E



unit: mm

3190-SQFP64



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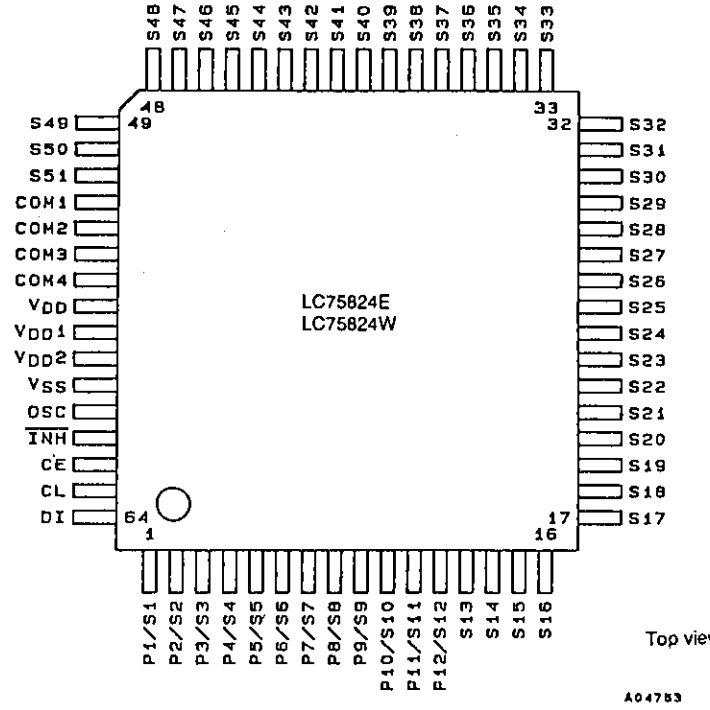
Pin Assignment



Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	−0.3 to +7.0	V
Input voltage	$V_{IN}1$	CE, CL, DI, $\overline{INH}$	−0.3 to +7.0	V
	$V_{IN}2$	OSC, $V_{DD}1$, $V_{DD}2$	−0.3 to V_{DD} + 0.3	
Output voltage	V_{OUT}	OSC, S1 to S51, COM1 to COM4, P1 to P12	−0.3 to V_{DD} + 0.3	V
Output current	$I_{OUT}1$	S1 to S51	300	μA
	$I_{OUT}2$	COM1 to COM4	3	mA
	$I_{OUT}3$	P1 to P12	5	
Allowable power dissipation	Pd max	Ta = 85°C	200	mW
Operating temperature	Topr		−40 to +85	°C
Storage temperature	Tstg		−55 to +125	°C

Allowable Operating Ranges at Ta = –40 to 85°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}	V_{DD}	3.0		6.0	V
Input voltage	$V_{DD}1$	$V_{DD}1$		2/3 V_{DD}	V_{DD}	V
	$V_{DD}2$	$V_{DD}2$		1/3 V_{DD}	V_{DD}	
Input high-level voltage	V_{IH}	CE, CL, DI, $\overline{INH}$	0.8 V_{DD}		6.0	V
Input low-level voltage	V_{IL}	CE, CL, DI, $\overline{INH}$	0		0.2 V_{DD}	V
Recommended external resistance	R_{OSC}	OSC		270		kΩ
Recommended external capacitance	C_{OSC}	OSC		100		pF
Guaranteed oscillation range	f_{OSC}	OSC	25	50	100	kHz
Data setup time	t_{ds}	CL, DI: Figure 2	160			ns
Data hold time	t_{dh}	CL, DI: Figure 2	160			ns
CE wait time	t_{cp}	CE, CL: Figure 2	160			ns
CE setup time	t_{cs}	CE, CL: Figure 2	160			ns
CE hold time	t_{ch}	CE, CL: Figure 2	160			ns
High-level clock pulse width	$t_{\phi H}$	CL: Figure 2	160			ns
Low-level clock pulse width	$t_{\phi L}$	CL: Figure 2	160			ns
Rise time	t_r	CE, CL, DI: Figure 2		160		ns
Fall time	t_f	CE, CL, DI: Figure 2		160		ns
$\overline{INH}$ switching time	t_c	$\overline{INH}$, CE: Figure 3	10			μs

Electrical Characteristics for the Allowable Operating Ranges

Parameter	Symbol	Conditions	min	typ	max	Unit
Hysteresis	V_H	CE, CL, DI, $\overline{INH}$		0.1 V_{DD}		V
Input high-level current	I_{IH}	CE, CL, DI, $\overline{INH}$: V_I = 6.0 V			5.0	μA
Input low-level current	I_{IL}	CE, CL, DI, $\overline{INH}$: V_I = 0 V	–5.0			μA
Output high-level voltage	$V_{OH}1$	S1 to S51: I_O = –20 μA	V_{DD} – 1.0			V
	$V_{OH}2$	COM1 to COM4: I_O = –100 μA	V_{DD} – 1.0			
	$V_{OH}3$	P1 to P12: I_O = –1 mA	V_{DD} – 1.0			
Output low-level voltage	$V_{OL}1$	S1 to S51: I_O = 20 μA			1.0	V
	$V_{OL}2$	COM1 to COM4: I_O = 100 μA			1.0	
	$V_{OL}3$	P1 to P12: I_O = 1 mA			1.0	
Output middle-level voltage*	$V_{MID}1$	COM1 to COM4: 1/2 bias, I_O = ±100 μA	1/2 V_{DD} – 1.0		1/2 V_{DD} + 1.0	V
	$V_{MID}2$	S1 to S51: 1/3 bias, I_O = ±20 μA	2/3 V_{DD} – 1.0		2/3 V_{DD} + 1.0	
	$V_{MID}3$	S1 to S51: 1/3 bias, I_O = ±20 μA	1/3 V_{DD} – 1.0		1/3 V_{DD} + 1.0	
	$V_{MID}4$	COM1 to COM4: 1/3 bias, I_O = ±100 μA	2/3 V_{DD} – 1.0		2/3 V_{DD} + 1.0	
	$V_{MID}5$	COM1 to COM4: 1/3 bias, I_O = ±100 μA	1/3 V_{DD} – 1.0		1/3 V_{DD} + 1.0	
Oscillator frequency	f_{OSC}	OSC: R_{OSC} = 270 kΩ, C_{OSC} = 100 pF	40	50	60	kHz
Current drain	$I_{DD}1$	Power-saving mode			5	μA
	$I_{DD}2$	V_{DD} = 3.0 V, outputs open, 1/2 bias, f_{OSC} = 50 kHz, control data CU = 0		70	140	
	$I_{DD}3$	V_{DD} = 6.0 V, outputs open, 1/2 bias, f_{OSC} = 50 kHz, control data CU = 0		200	400	
	$I_{DD}4$	V_{DD} = 3.0 V, outputs open, 1/3 bias, f_{OSC} = 50 kHz, control data CU = 0		80	160	
	$I_{DD}5$	V_{DD} = 6.0 V, outputs open, 1/3 bias, f_{OSC} = 50 kHz, control data CU = 0		250	500	
	$I_{DD}6$	V_{DD} = 3.0 V, outputs open, 1/2 bias, f_{OSC} = 50 kHz, control data CU = 1		30	60	
	$I_{DD}7$	V_{DD} = 6.0 V, outputs open, 1/2 bias, f_{OSC} = 50 kHz, control data CU = 1		130	260	
	$I_{DD}8$	V_{DD} = 3.0 V, outputs open, 1/3 bias, f_{OSC} = 50 kHz, control data CU = 1		40	80	
	$I_{DD}9$	V_{DD} = 6.0 V, outputs open, 1/3 bias, f_{OSC} = 50 kHz, control data CU = 1		150	300	

Note: * Excluding the bias voltage generation divider resistors built into the $V_{DD}1$ and $V_{DD}2$. (See Figure 1)

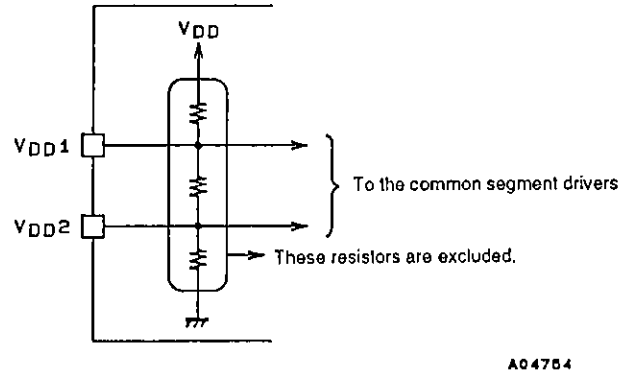
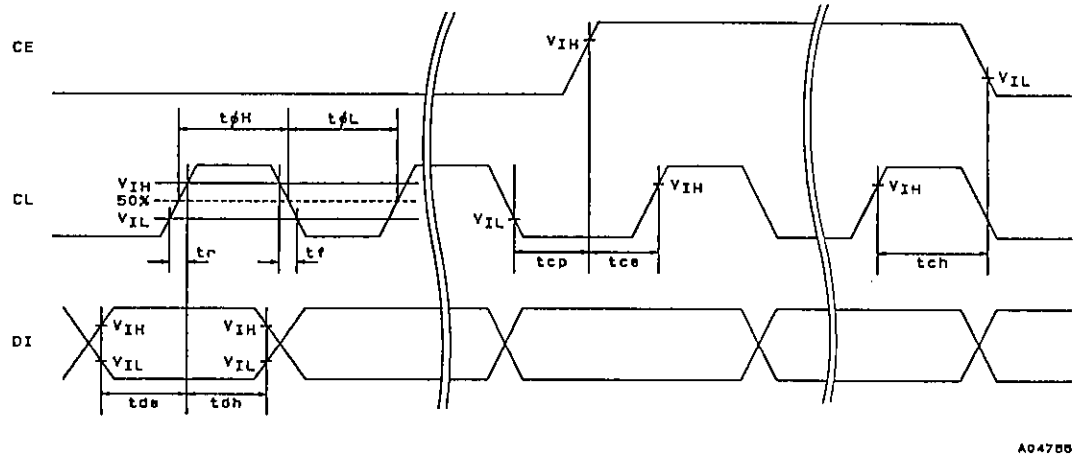


Figure 1

1. When CL is stopped at the low level



2. When CL is stopped at the high level

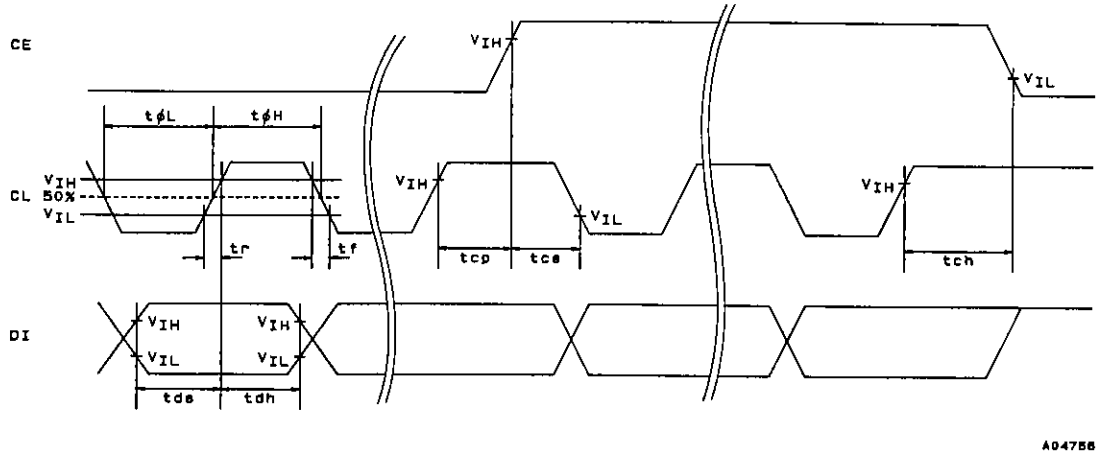
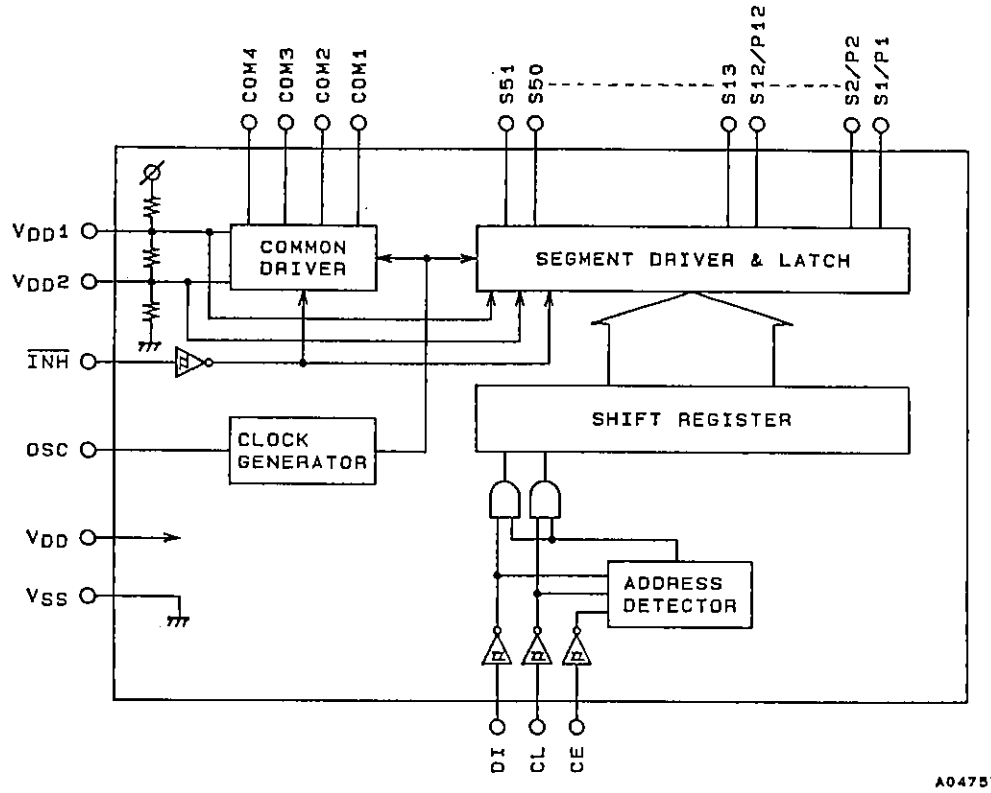


Figure 2

Block Diagram

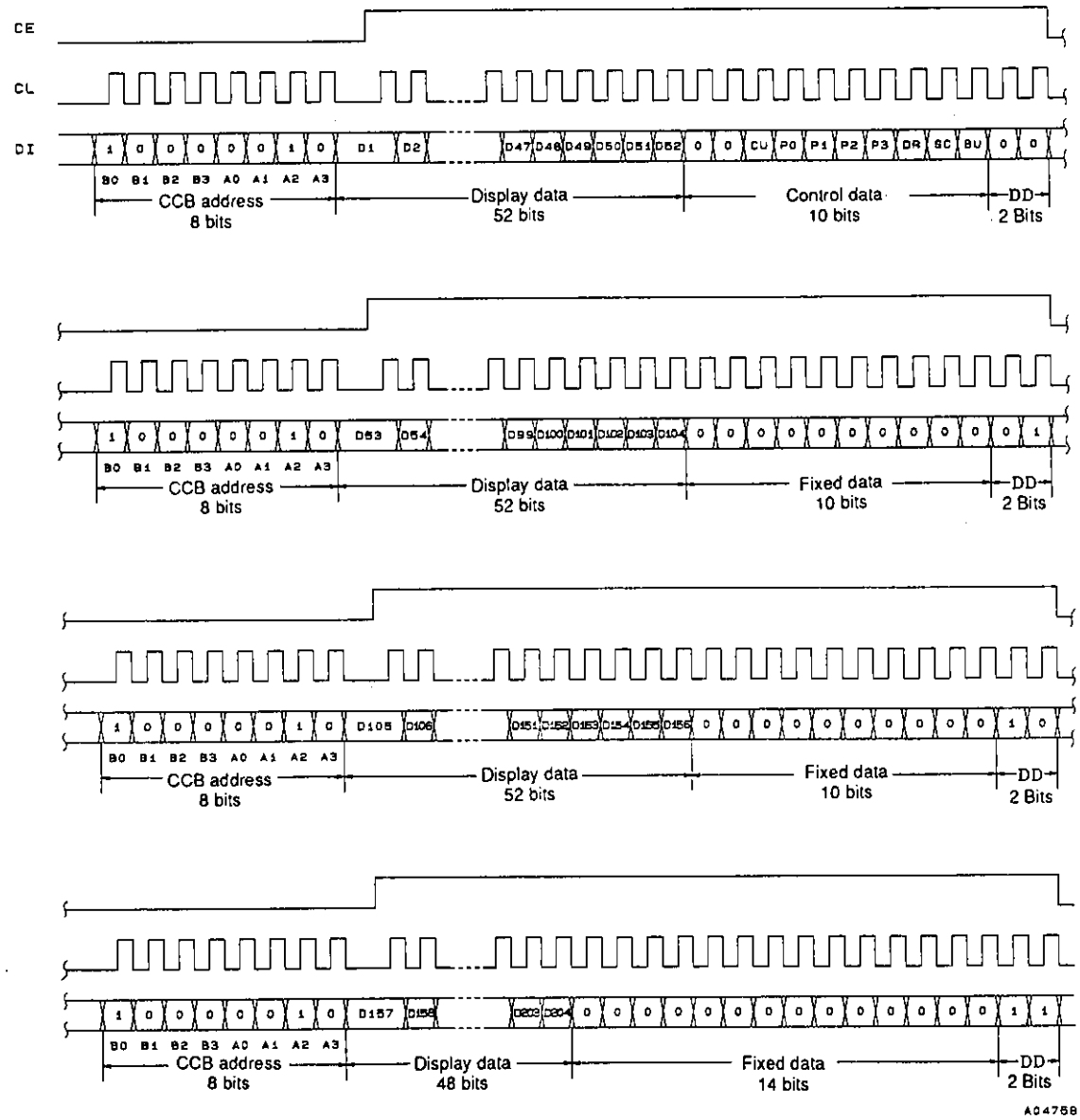


Pin Functions

Pin	Pin No.	Function		Active	I/O	Handling when unused
S1/P1 to S12/P12, S13 to S51	1 to 12, 13 to 51	Segment outputs for displaying the display data transferred by serial data input. Pins S1/P1 to S12/P12 can be used as general-purpose output ports when so specified by the control data.		—	O	Open
COM1 to COM4	52 to 55	Common driver outputs. The frame frequency f_O is given by: $f_O = (f_{OSC}/512)$ Hz.		—	O	Open
OSC	60	Oscillator connection. An oscillator circuit is formed by connecting an external resistor and capacitor to this pin.		—	I/O	GND
CE	62	Serial data transfer inputs. These pins are connected to the control microprocessor.	CE: Chip enable	H	I	GND
CL	63		CL: Synchronization clock	↑	I	
DI	64		DI: Transfer data	—	I	
$\overline{INH}$	61	Display off control input • $\overline{INH}$ = low (V_{SS}) .....Display forced off Pins S1/P1 to S12/P12 = low (These pins are forced to the segment output port function and held low.) S13 to S51 = low COM1 to COM4 = low • $\overline{INH}$ = high (V_{DD}).....Display on Note that serial data transfers can be performed when the display is forced off.		L	I	GND
$V_{DD}1$	57	Used to apply the LCD drive 2/3 bias voltage. Short this pin to $V_{DD}2$ if a 1/2-bias drive scheme is used.		—	I	Open
$V_{DD}2$	58	Used to apply the LCD drive 1/3 bias voltage. Short this pin to $V_{DD}1$ if a 1/2-bias drive scheme is used.		—	I	Open
V_{DD}	56	Power supply. Provide a voltage of between 3.0 and 6.0 V.		—	—	—
V_{SS}	59	Ground. Connect this pin to the system ground.		—	—	—

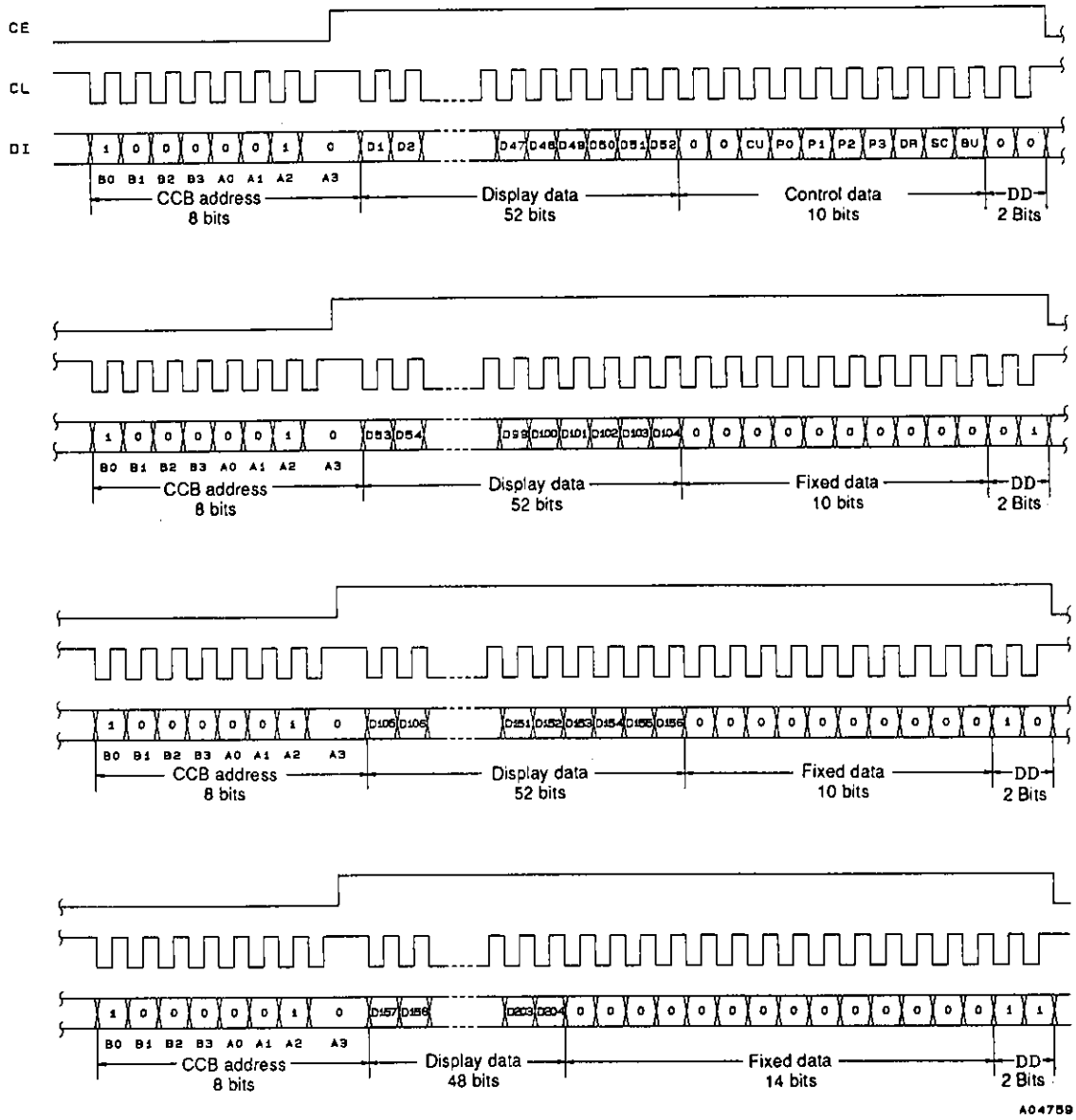
Serial Data Input

1. When CL is stopped at the low level



Note: DD is the direction data.

2. When CL is stopped at the high level

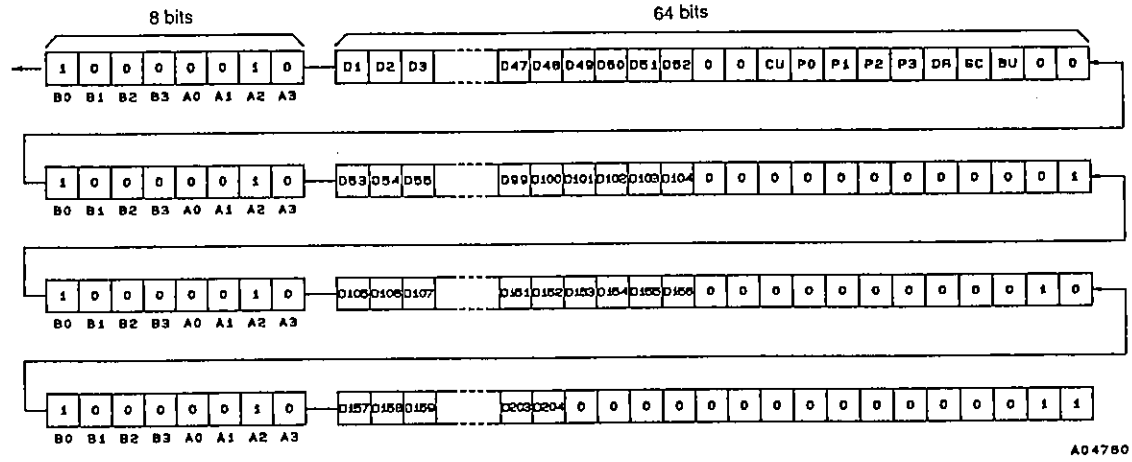


Note: DD is the direction data.

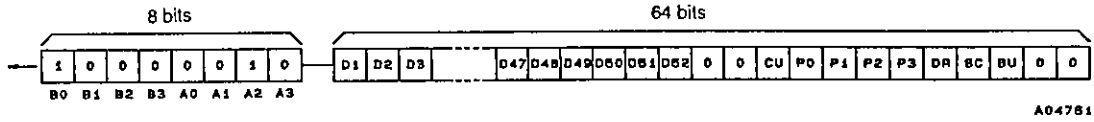
- CCB address.....41H
- D1 to D204.....Display data
- CU.....Normal mode current drain control data
- P0 to P3.....Segment output port/general-purpose output port switching control data
- DR.....1/2-bias drive or 1/3-bias drive switching control data
- SC.....Segments on/off control data
- BU.....Normal mode/power-saving mode control data

Serial Data Transfer Examples

1. When 157 or more segments are used
   All 256 bits of the serial data must be sent.



2. When fewer than 157 segments are used
   Either 64 bits, 128 bits, or 192 bits of serial data must be sent, depending on the number of segments actually used. However, the serial data shown in the figure below (the display data D1 to D52 and the control data) must always be sent.



Control Data Functions

1. CU: Normal mode current drain control data
   This control data bit controls the current drain in normal mode.

CU	Current drain mode in normal mode
0	Normal current drain mode ($I_{DD}2$, $I_{DD}3$, $I_{DD}4$, and $I_{DD}5$)
1	Low current drain mode ($I_{DD}6$, $I_{DD}7$, $I_{DD}8$, and $I_{DD}9$)

However, note that the common and segment output waveforms are easily caused distortion when the low current drain mode is selected by setting CU to 1, because in this mode the capacity to supply current to the LCD panel from the common and segment pins is mode less than that in the normal current drain mode (CU = 0).

2. P0 to P3: Segment output port/general-purpose output port switching control data
   These control data bits switch the segment output port/general-purpose output port functions of the S1/P1 to S12/P12 output pins.

Control data				Output pin states											
P0	P1	P2	P3	S1/P1	S2/P2	S3/P3	S4/P4	S5/P5	S6/P6	S7/P7	S8/P8	S9/P9	S10/P10	S11/P11	S12/P12
0	0	0	0	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
0	0	0	1	P1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
0	0	1	0	P1	P2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
0	0	1	1	P1	P2	P3	S4	S5	S6	S7	S8	S9	S10	S11	S12
0	1	0	0	P1	P2	P3	P4	S5	S6	S7	S8	S9	S10	S11	S12
0	1	0	1	P1	P2	P3	P4	P5	S6	S7	S8	S9	S10	S11	S12
0	1	1	0	P1	P2	P3	P4	P5	P6	S7	S8	S9	S10	S11	S12
0	1	1	1	P1	P2	P3	P4	P5	P6	P7	S8	S9	S10	S11	S12
1	0	0	0	P1	P2	P3	P4	P5	P6	P7	P8	S9	S10	S11	S12
1	0	0	1	P1	P2	P3	P4	P5	P6	P7	P8	P9	S10	S11	S12
1	0	1	0	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	S11	S12
1	0	1	1	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	S12
1	1	0	0	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12

Note: Sn (n = 1 to 12): Segment output port function
Pn (n = 1 to 12): General-purpose output port function

When the general-purpose output port function is selected the output pins and the display data have the correspondence listed in the tables below.

Output pin	Corresponding display data
S1/P1	D1
S2/P2	D5
S3/P3	D9
S4/P4	D13
S5/P5	D17
S6/P6	D21

Output pin	Corresponding display data
S7/P7	D25
S8/P8	D29
S9/P9	D33
S10/P10	D37
S11/P11	D41
S12/P12	D45

For example, when the general-purpose output port function is selected for the S4/P4 output pin, that output pin will output a high level when display data D13 is 1, and will output a low level when D13 is 0.

3. DR: 1/2-bias drive or 1/3-bias drive switching control data
   This control data bit selects either 1/2-bias drive or 1/3-bias drive.

DR	Drive type
0	1/3-bias drive
1	1/2-bias drive

4. SC: Segments on/off control data
   This control data bit controls the on/off state of the segments.

SC	Display state
0	On
1	Off

   However, note that when the segments are turned off by setting SC to 1, the segments are turned off by outputting segment off waveforms from the segment output pins.

5. BU: Normal mode/power-saving mode control data
   This control data bit selects either normal mode or power-saving mode.

BU	Mode
0	Normal mode
1	Power-saving mode. In this mode the OSC pin oscillator is stopped and the common and segment pins output low levels. However, the S1/P1 to S12/P12 output pins can still be used as general-purpose output ports under the control of the control data bits P0 to P3.

Display Data to Output Pin Correspondence

Output pin	COM1	COM2	COM3	COM4
S1/P1	D1	D2	D3	D4
S2/P2	D5	D6	D7	D8
S3/P3	D9	D10	D11	D12
S4/P4	D13	D14	D15	D16
S5/P5	D17	D18	D19	D20
S6/P6	D21	D22	D23	D24
S7/P7	D25	D26	D27	D28
S8/P8	D29	D30	D31	D32
S9/P9	D33	D34	D35	D36
S10/P10	D37	D38	D39	D40
S11/P11	D41	D42	D43	D44
S12/P12	D45	D46	D47	D48
S13	D49	D50	D51	D52
S14	D53	D54	D55	D56
S15	D57	D58	D59	D60
S16	D61	D62	D63	D64
S17	D65	D66	D67	D68
S18	D69	D70	D71	D72
S19	D73	D74	D75	D76
S20	D77	D78	D79	D80
S21	D81	D82	D83	D84
S22	D85	D86	D87	D88
S23	D89	D90	D91	D92
S24	D93	D94	D95	D96
S25	D97	D98	D99	D100

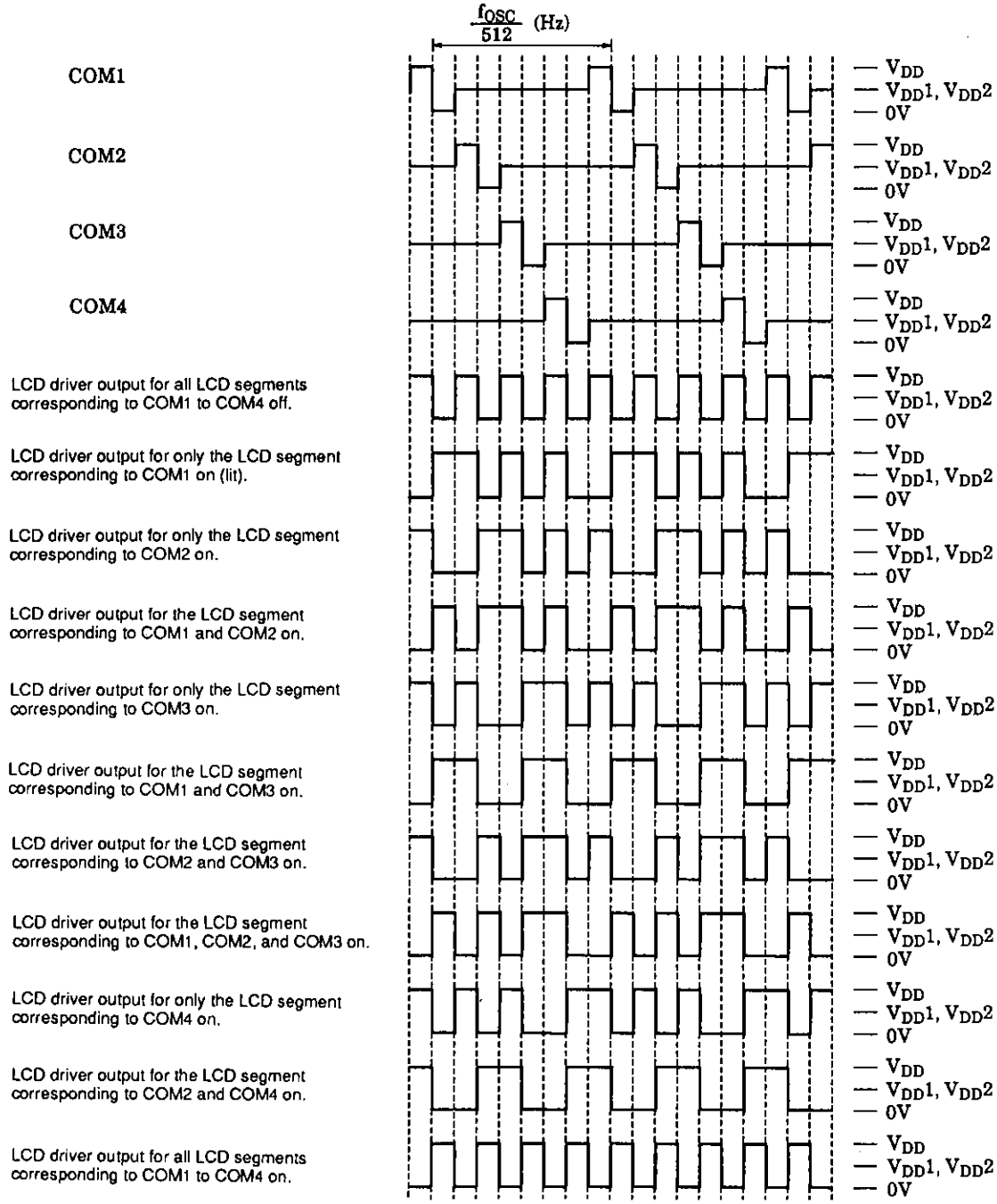
Output pin	COM1	COM2	COM3	COM4
S26	D101	D102	D103	D104
S27	D105	D106	D107	D108
S28	D109	D110	D111	D112
S29	D113	D114	D115	D116
S30	D117	D118	D119	D120
S31	D121	D122	D123	D124
S32	D125	D126	D127	D128
S33	D129	D130	D131	D132
S34	D133	D134	D135	D136
S35	D137	D138	D139	D140
S36	D141	D142	D143	D144
S37	D145	D146	D147	D148
S38	D149	D150	D151	D152
S39	D153	D154	D155	D156
S40	D157	D158	D159	D160
S41	D161	D162	D163	D164
S42	D165	D166	D167	D168
S43	D169	D170	D171	D172
S44	D173	D174	D175	D176
S45	D177	D178	D179	D180
S46	D181	D182	D183	D184
S47	D185	D186	D187	D188
S48	D189	D190	D191	D192
S49	D193	D194	D195	D196
S50	D197	D198	D199	D200
S51	D201	D202	D203	D204

Note: These tables assume that the segment output port function is selected for the S1/P1 to S12/P12 output pins.

The table presents the states of the S21 output pin as an example.

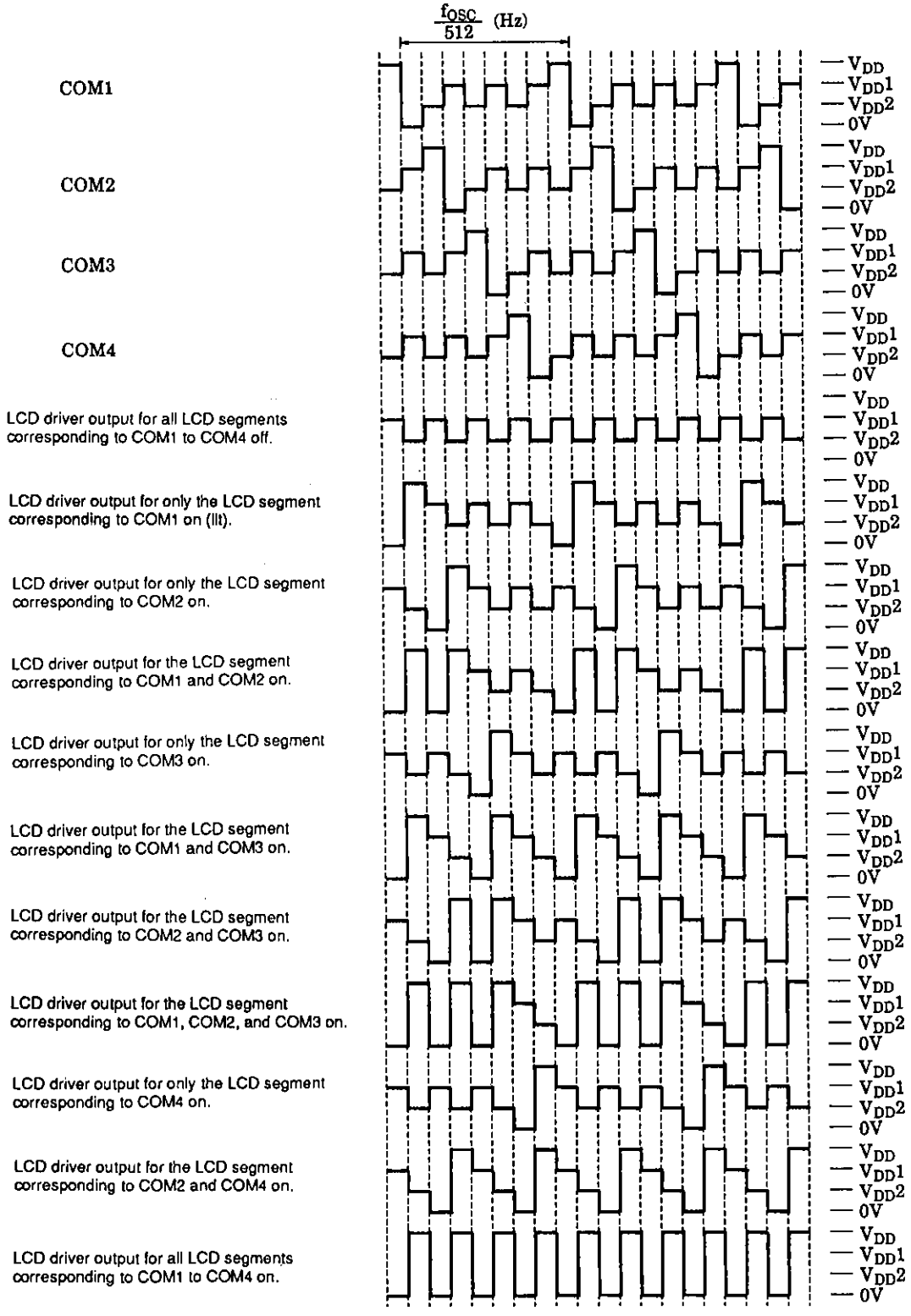
Display data				Output pin (S21) state
D81	D82	D83	D84	
0	0	0	0	The LCD segments corresponding to COM1 to COM4 are off.
0	0	0	1	The LCD segment corresponding to COM4 is on (lit).
0	0	1	0	The LCD segment corresponding to COM3 is on.
0	0	1	1	The LCD segments corresponding to COM3 and COM4 are on.
0	1	0	0	The LCD segment corresponding to COM2 is on.
0	1	0	1	The LCD segments corresponding to COM2 and COM4 are on.
0	1	1	0	The LCD segments corresponding to COM2 and COM3 are on.
0	1	1	1	The LCD segments corresponding to COM2, COM3, and COM4 are on.
1	0	0	0	The LCD segment corresponding to COM1 is on.
1	0	0	1	The LCD segments corresponding to COM1 and COM4 are on.
1	0	1	0	The LCD segments corresponding to COM1 and COM3 are on.
1	0	1	1	The LCD segments corresponding to COM1, COM3, and COM4 are on.
1	1	0	0	The LCD segments corresponding to COM1 and COM2 are on.
1	1	0	1	The LCD segments corresponding to COM1, COM2, and COM4 are on.
1	1	1	0	The LCD segments corresponding to COM1, COM2, and COM3 are on.
1	1	1	1	The LCD segments corresponding to COM1 to COM4 are on.

1/4-Duty 1/2-Bias Drive Scheme



1/4-Duty 1/2-Bias Waveforms A04762

1/4-Duty 1/3-Bias Drive Scheme



1/4-Duty 1/3-Bias Waveforms

A04763

Display Control and the $\overline{\text{INH}}$ Pin

Since the LSI internal data (the display data D1 to D204 and the control data) is undefined when power is first applied, applications should prevent meaningless displays with the following procedure. First, set the $\overline{\text{INH}}$ pin low at the same time as power is applied to turn off the display. This will set the S1/P1 to S12/P12, S13 to S51, and COM1 to COM4 pins low. While the $\overline{\text{INH}}$ pin is held low, the control microprocessor should send the serial data. Finally, the application can set the $\overline{\text{INH}}$ pin to high. (See Figure 3.)

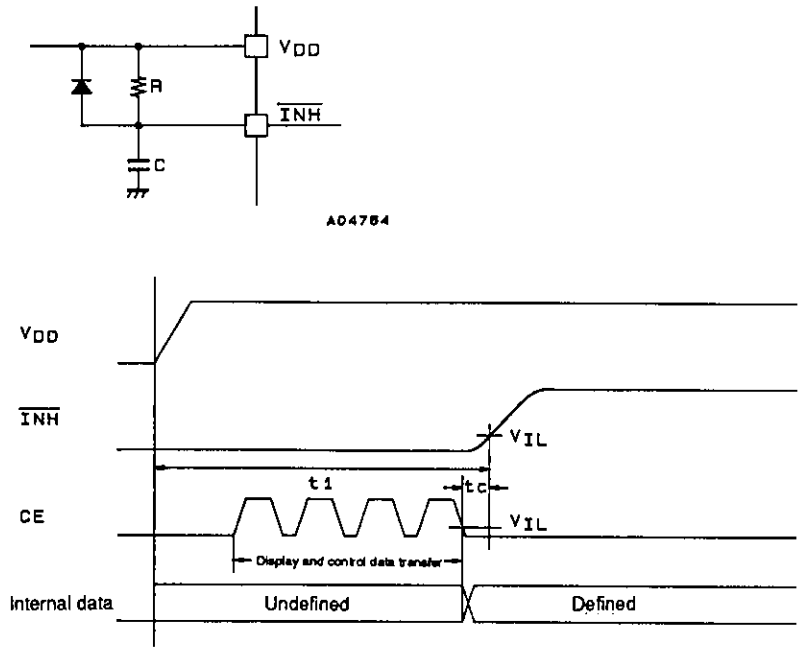


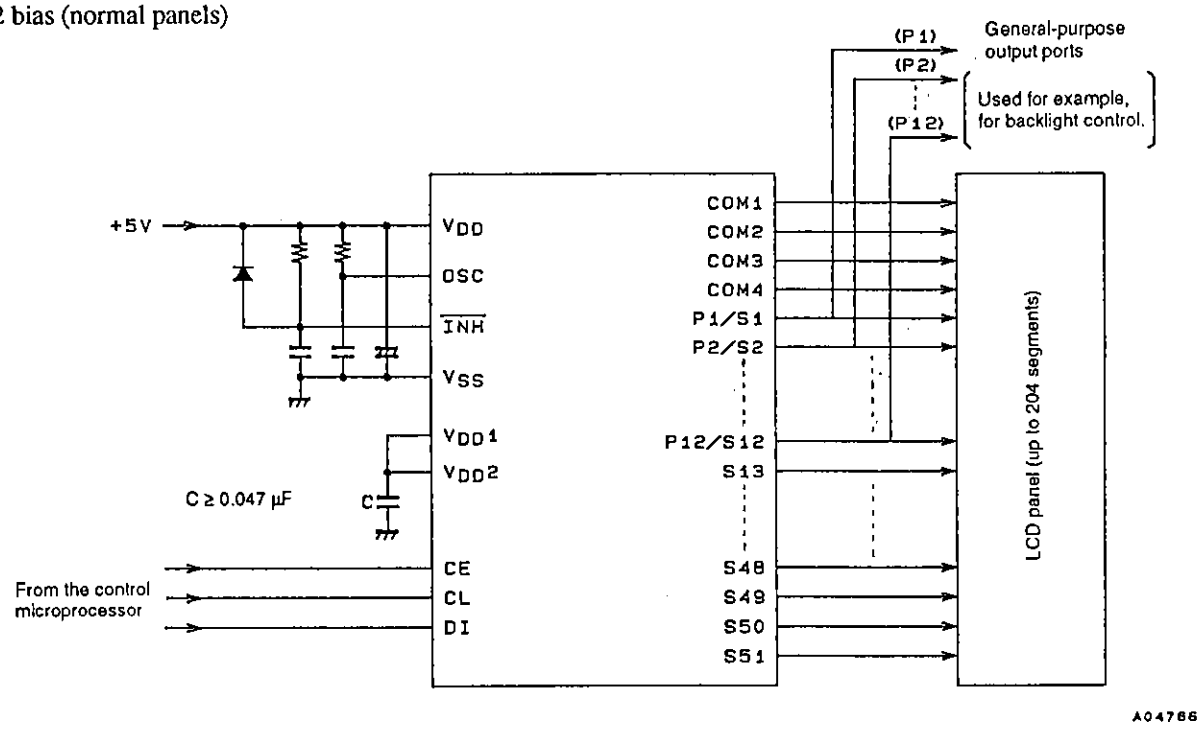
Figure 3

Notes on Microprocessor Transfer of Display Data

Since the LC75824E and LC75824W accept the display data divided into four separate transfer operations, we recommend that applications make a point of completing all four data transfers within a period of no more than 30 ms to guarantee the quality of the displayed image.

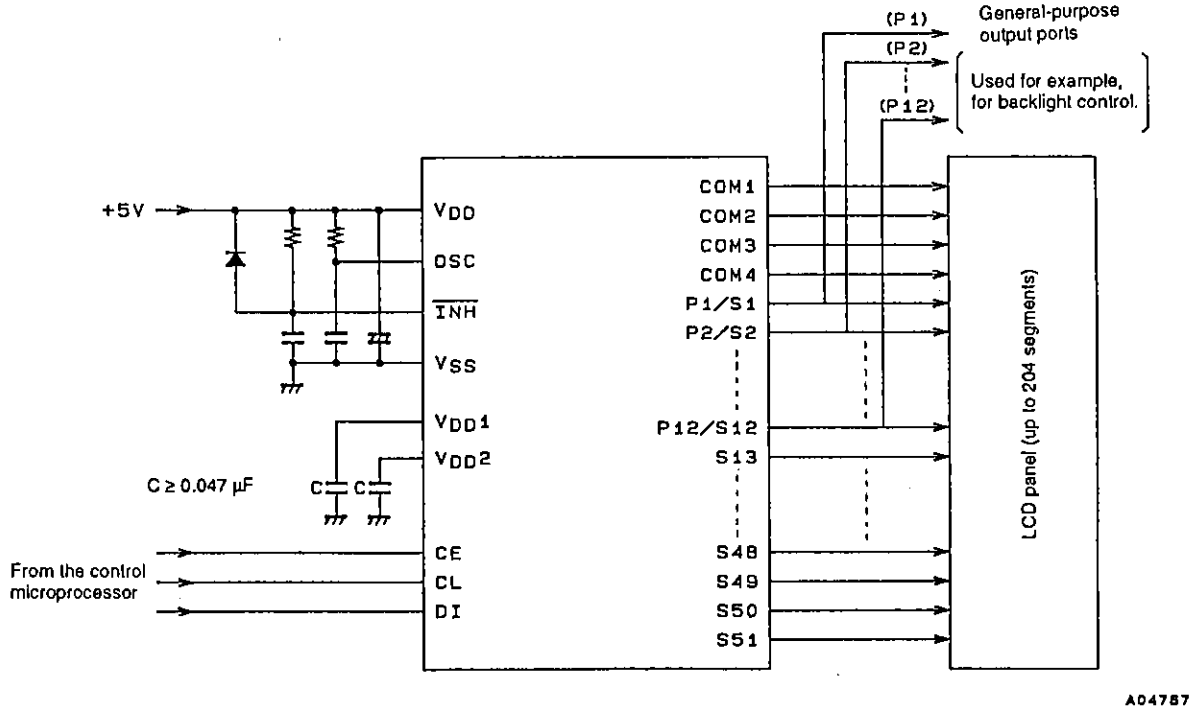
Application Circuit Example 1

1/2 bias (normal panels)



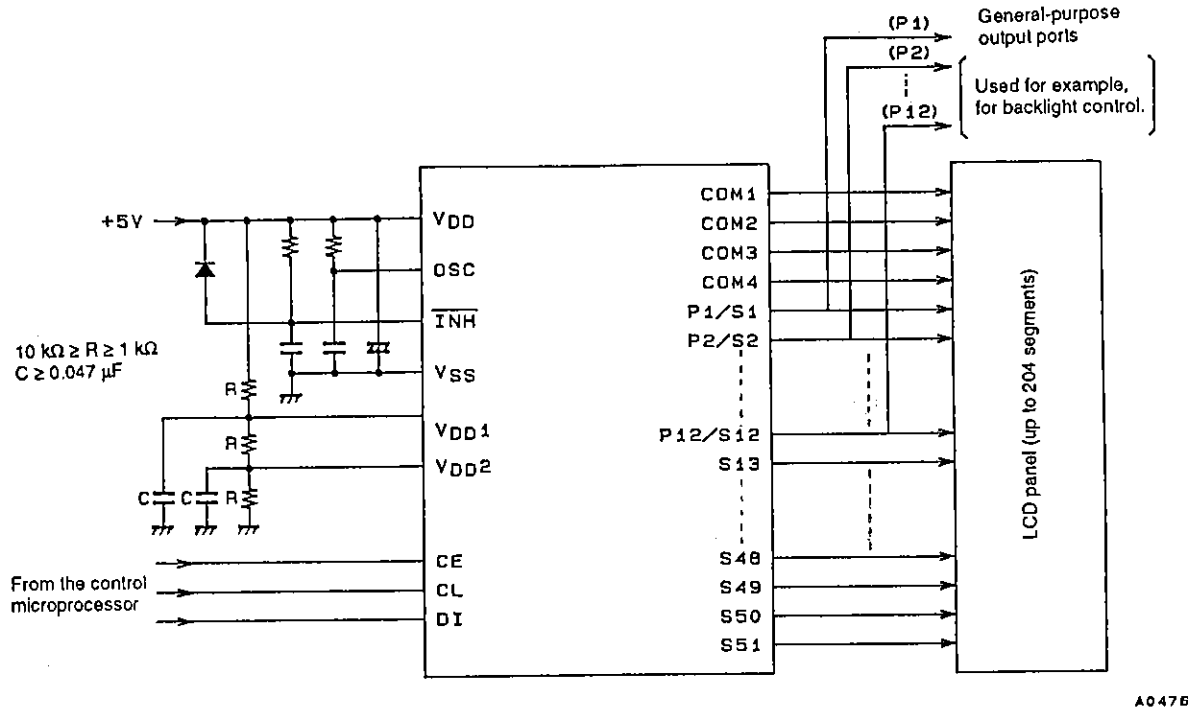
Application Circuit Example 2

1/3 bias (normal panels)



Application Circuit Example 3

1/3 bias (large panels)



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