Ordering number : EN4467

CMOS LSI

No. 4467

LC75850E, 75850W

1/3 Duty General Purpose LCD Drivers

Overview

The LC75850E and LC75850W are general purpose LCD drivers for use in microprocessor controlled applications such as radio tuner frequency displays.

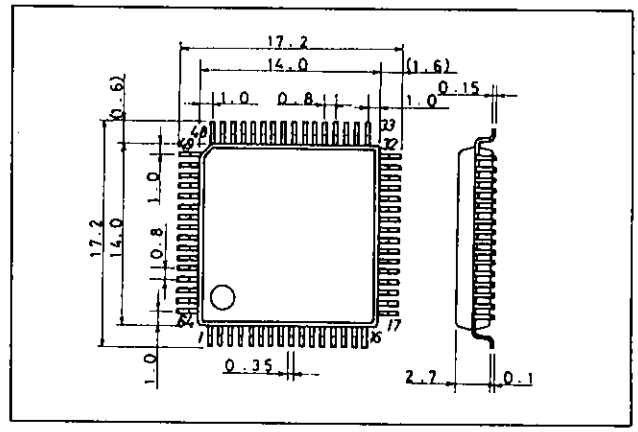
Functions

- Supports both 1/3 duty 1/2 bias and 1/3 duty 1/3 bias LCD drive techniques for a maximum of 156 segments.
- Power saving mode allows the backup function to be switched on or off and all segments to be turned off unconditionally.
- Can be controlled by three serial data lines (CE, CL, and DI) from the microprocessor. (CCB handling)
- High generality, since segment data can be displayed without going through a decoder
- The $\overline{\text{INH}}$ pin unconditionally turns off display.
- The LCD drive bias voltage can be provided internally or externally.
- Power supply voltage: 4.5 to 8 V

Package Dimensions

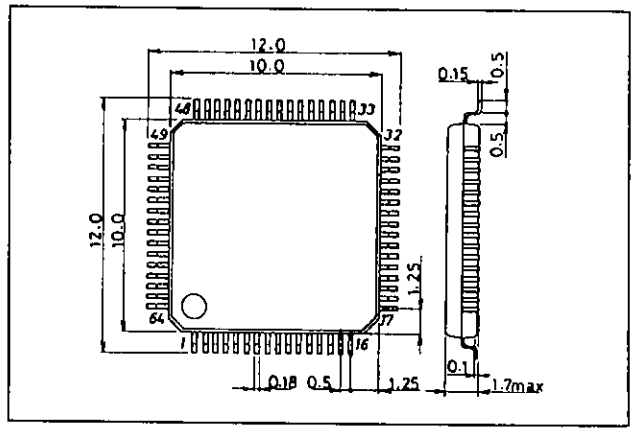
unit: mm

3159-QIP64E (LC75850E)



unit: mm

3190-SQFP64 (LC75850W)



Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Condition	Rating	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	−0.3 to +9.0	V
Input voltage	V_{IN} (1)	CE, CL, DI, $\overline{\text{INH}}$	−0.3 to +9.0	V
	V_{IN} (2)	OSC	−0.3 to V_{DD} + 0.3	V
Output voltage	V_{OUT}	OSC	−0.3 to V_{DD} + 0.3	V
Output current	I_{OUT} (1)	S1 to S52	300	μA
	I_{OUT} (2)	COM1 to COM3	3	mA
Allowable power dissipation	Pd max	Ta ≤ 85°C	200	mW
Operating temperature	Topr		−40 to +85	°C
Storage temperature	Tstg		−55 to +125	°C

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Allowable Operating Ranges at Ta = –40 to +85°C, V_{SS} = 0 V

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply voltage	V_{DD}	V_{DD}	4.5		8.0	V
Input voltage	$V_{DD}1$	$V_{DD}1$		2/3 V_{DD}	8.0	V
	$V_{DD}2$	$V_{DD}2$		1/3 V_{DD}	8.0	V
Input high level voltage	V_{IH}	CE, CL, DI, $\overline{INH}$	4.0		8.0	V
Input low level voltage	V_{IL}	CE, CL, DI, $\overline{INH}$	0		0.7	V
Recommended external resistance	R_{OSC}	OSC		47		kΩ
Recommended external capacitance	C_{OSC}	OSC		1000		pF
Guaranteed oscillator range	f_{OSC}	OSC	19	38	76	kHz
Data setup time	t_{ds}	CL, DI: Figure 2	100			ns
Data hold time	t_{dh}	CL, DI: Figure 2	100			ns
CE wait time	t_{cp}	CE, CL: Figure 2	100			ns
CE setup time	t_{cs}	CE, CL: Figure 2	100			ns
CE hold time	t_{ch}	CE, CL: Figure 2	100			ns
CL high level time	$t_{\phi H}$	CL: Figure 2	100			ns
CL low level time	$t_{\phi L}$	CL: Figure 2	100			ns
Rise time	t_r	CE, CL, DI: Figure 2		100		ns
Fall time	t_f	CE, CL, DI: Figure 2		100		ns
$\overline{INH}$ switching time	t2	Figure 3	10			µs

Electrical Characteristics at Ta = –40 to +85°C, V_{SS} = 0 V

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Input high level current	I_{IH} (1)	CE, CL DI $\overline{INH}$; V_{IH} = 8 V			5	µA
Input low level current	I_{IL} (2)	CE, CL DI $\overline{INH}$; V_{IL} = 0 V			5	µA
Oscillator frequency	f_{OSC}	OSC; R_{OSC} = 47 kΩ, C_{OSC} = 1000 pF		38		kHz
Hysteresis	V_H	CE, CL DI $\overline{INH}$; V_{DD} = 5 V	0.3			V
Output high level voltage	V_{OH} (1)	S1 to S52; I_{OUT} (1) = –20 µA	V_{DD} – 1.0			V
Output low level voltage	V_{OL} (1)	S1 to S52; I_{OUT} (1) = 20 µA			1.0	V
Output high level voltage	V_{OH} (2)	COM1 to COM3; I_{OUT} (2) = –100 µA	V_{DD} – 1.0			V
Output low level voltage	V_{OL} (2)	COM1 to COM3; I_{OUT} (2) = 100 µA			1.0	V
Intermediate level voltage*	V_{MID} (1)	1/2 bias, COM1 to COM3; I_{OUT} (2) = ±100 µA	1/2 V_{DD} ± 1.0			V
	V_{MID} (2)	1/3 bias, COM1 to COM3; I_{OUT} (2) = ±100 µA	2/3 V_{DD} ± 1.0			V
	V_{MID} (3)	1/3 bias, COM1 to COM3; I_{OUT} (2) = ±100 µA	1/3 V_{DD} ± 1.0			V
	V_{MID} (4)	1/3 bias, S1 to S52; I_{OUT} (1) = ±20 µA	2/3 V_{DD} ± 1.0			V
	V_{MID} (5)	1/3 bias, S1 to S52; I_{OUT} (1) = ±20 µA	1/3 V_{DD} ± 1.0			V
Supply current	I_{DD} (1)	Power saving mode			5	µA
	I_{DD} (2)	f = 38 kHz, 1/2 bias, V_{DD} = 5 V		400	800	µA
	I_{DD} (3)	f = 38 kHz, 1/3 bias, V_{DD} = 5 V		300	600	µA
	I_{DD} (4)	f = 38 kHz, 1/2 bias, V_{DD} = 8 V		650	1300	µA
	I_{DD} (5)	f = 38 kHz, 1/3 bias, V_{DD} = 8 V		580	1200	µA

Note: * Except the bias voltage generation divider resistors that are built into $V_{DD}1$ and $V_{DD}2$. (See figure 1.)

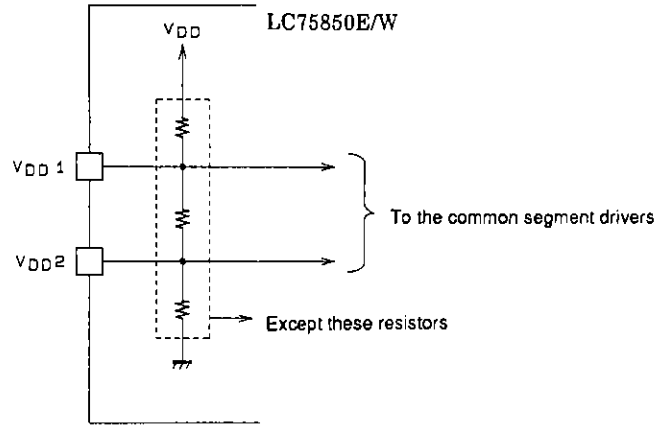
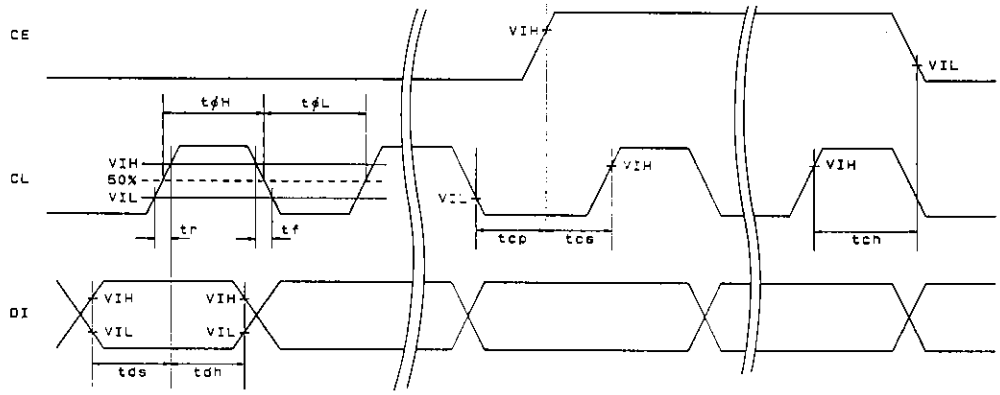


Figure 1

When CL is stopped at the low level



When CL is stopped at the high level

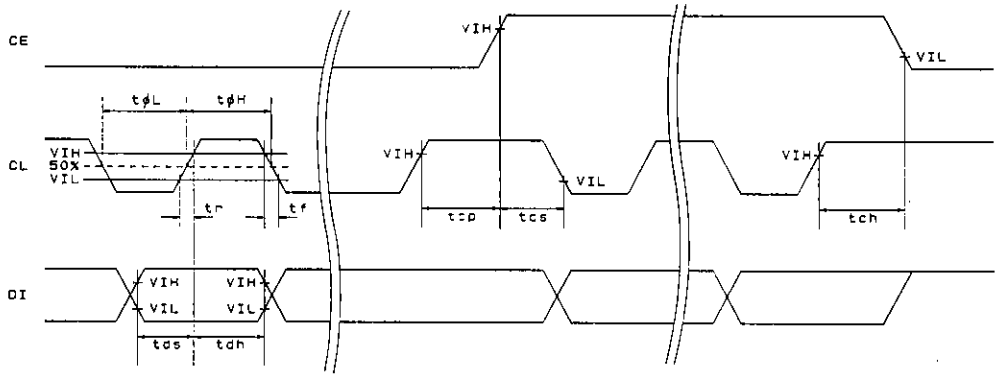
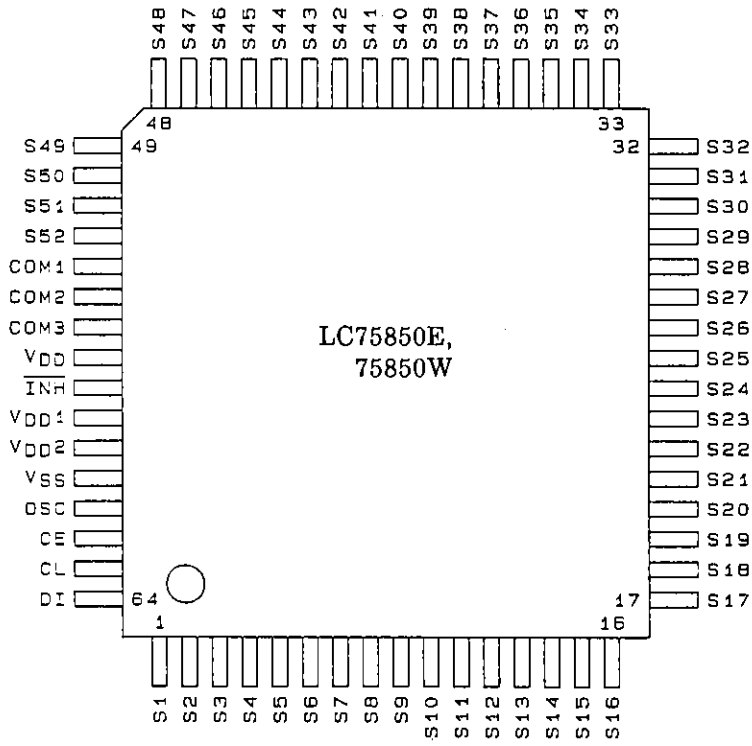
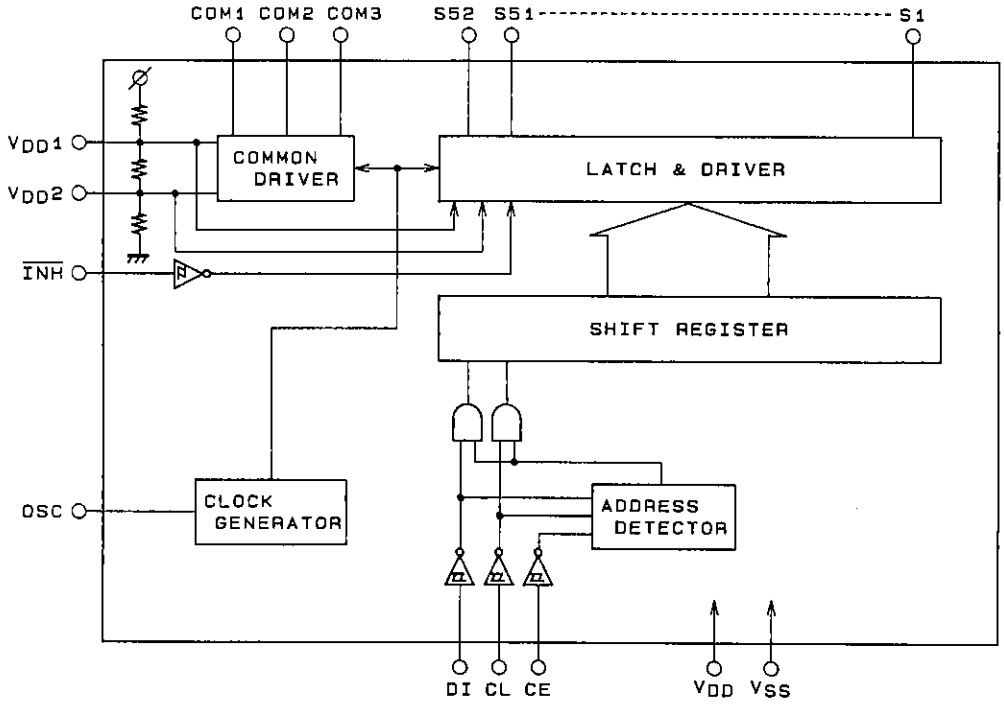


Figure 2

Pin Assignment



Block Diagram

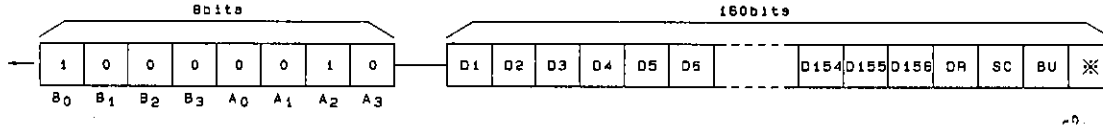


Pin Functions

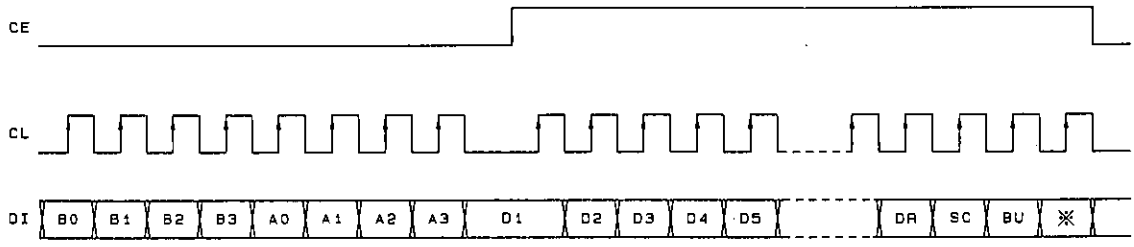
Pin	Pin No.	Function		Active	I/O	Handling when unused
S1 to S52	1 to 52	Segment outputs that display the data transferred as serial data		—	O	Open
COM1 COM2 COM3	53 54 55	Common driver outputs. The frame frequency is $f_O = (f_{OSC}/384)$ Hz.		—	O	Open
OSC	61	Oscillator connection (for generating the common segment alternation waveform)		—	I	GND
CE CL DI	62 63 64	Serial data transfer pins: connected to the microprocessor.	CE: chip enable	H	I	GND
			CL: synchronization clock	L → H		
			DI: transfer data	—		
$\overline{INH}$	57	Forcibly turns off the display without regard for the internal data. Serial data can always be input, whatever the state of this pin.		L	I	GND
$V_{DD}1$	58	Used for the 2/3 bias voltage when bias voltages are provided externally. Connect to $V_{DD}2$ when 1/2 bias is used.		—	I	Open
$V_{DD}2$	59	Used for the 1/3 bias voltage when bias voltages are provided externally. Connect to $V_{DD}1$ when 1/2 bias is used.		—	I	Open

Serial Data Transfer Format

1. Serial data



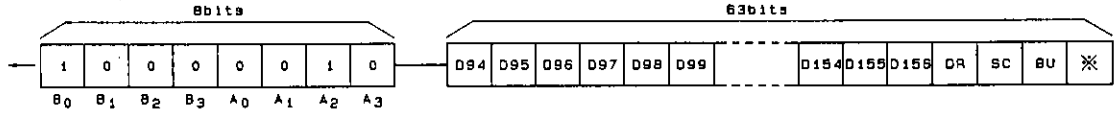
2. Data transfer format



3. When used with fewer than 156 segments

<Example> Using 63 segments

Segment allocation method .....Sixty three segments are allocated starting at D156.



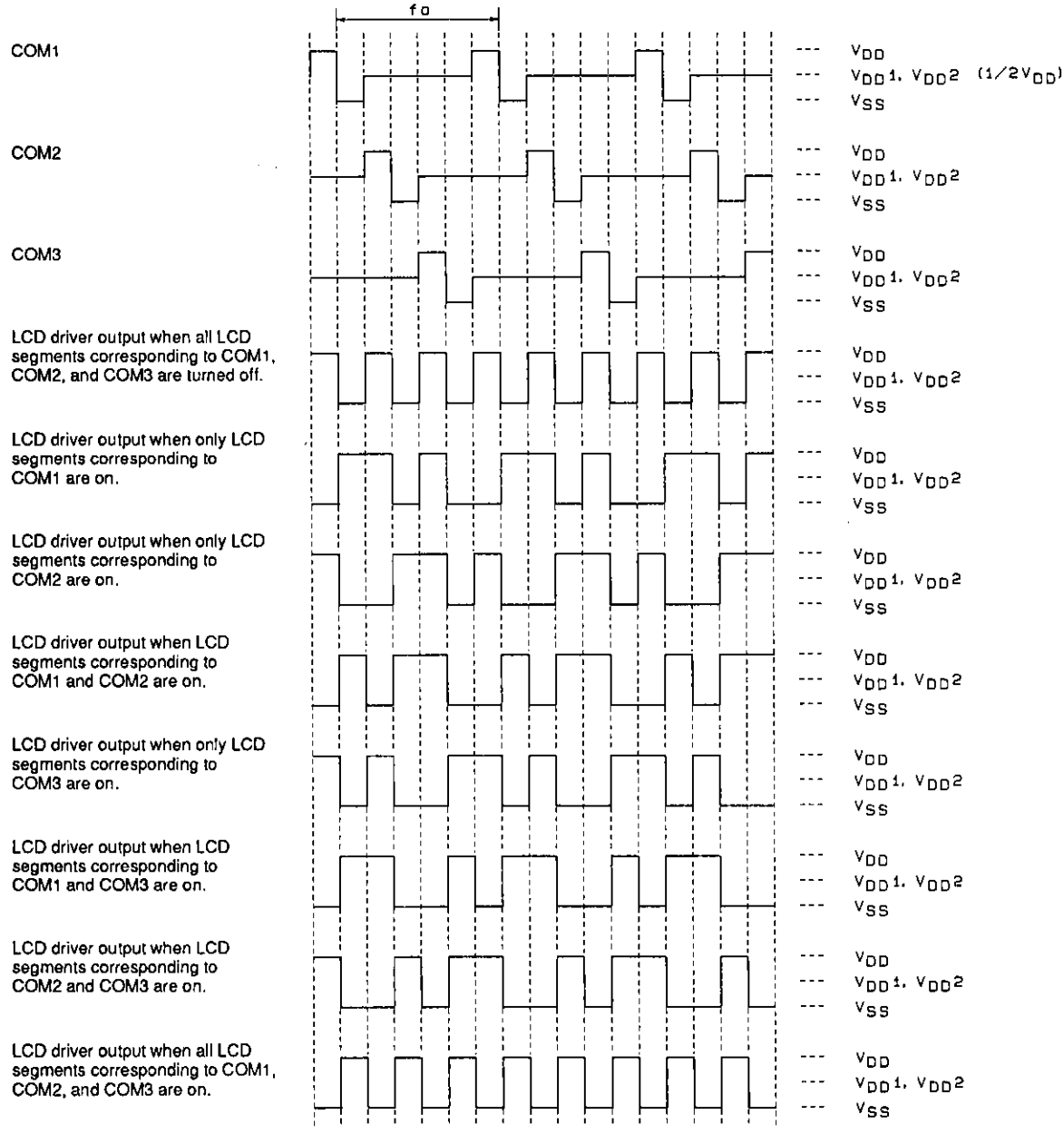
- CCB address.....41
- D1 to D156.....Display data
- DR .....Drive method selection bit
  1 = 1/3 duty, 1/3 bias
  0 = 1/3 duty, 1/2 bias
- SC.....Segment drive/clear control bit
  1 = Clear (Display clearing waveforms are output from common and segment pins.)
  0 = Drive (Normal drive)
- BU .....Normal mode/power saving mode control bit
  1 = Power saving mode (The oscillator is stopped and the common and segment pins go to the ground level.)
  0 = Normal mode
- *.....Don't care

Transferred Data/Output Pin Correspondence

	COM3	COM2	COM1
S1	D1	D2	D3
S2	D4	D5	D6
S3	D7	D8	D9
S4	D10	D11	D12
S5	D13	D14	D15
S6	D16	D17	D18
S7	D19	D20	D21
S8	D22	D23	D24
S9	D25	D26	D27
S10	D28	D29	D30
S11	D31	D32	D33
S12	D34	D35	D36
S13	D37	D38	D39
S14	D40	D41	D42
S15	D43	D44	D45
S16	D46	D47	D48
S17	D49	D50	D51
S18	D52	D53	D54
S19	D55	D56	D57
S20	D58	D59	D60
S21	D61	D62	D63
S22	D64	D65	D66
S23	D67	D68	D69
S24	D70	D71	D72
S25	D73	D74	D75
S26	D76	D77	D78

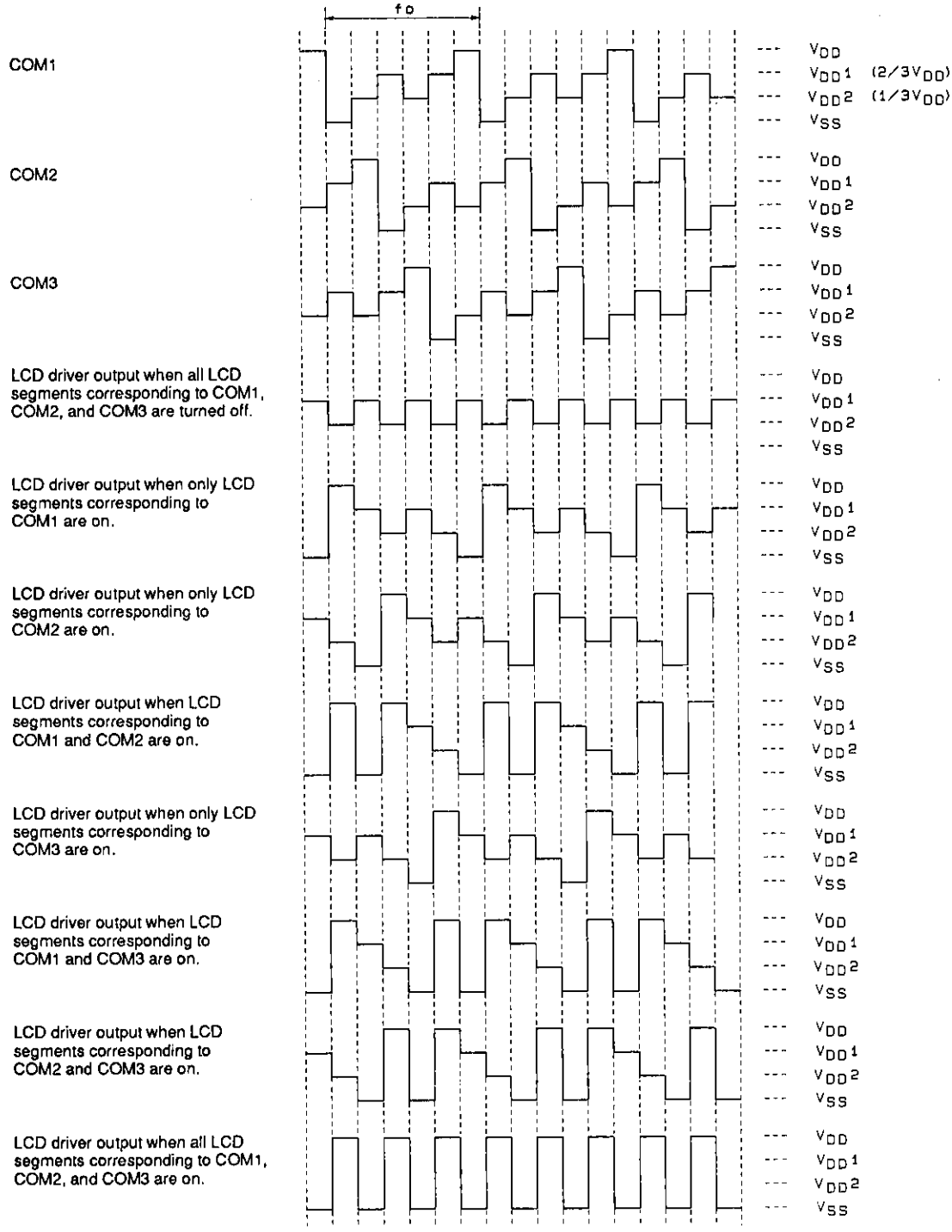
	COM3	COM2	COM1
S27	D79	D80	D81
S28	D82	D83	D84
S29	D85	D86	D87
S30	D88	D89	D90
S31	D91	D92	D93
S32	D94	D95	D96
S33	D97	D98	D99
S34	D100	D101	D102
S35	D103	D104	D105
S36	D106	D107	D108
S37	D109	D110	D111
S38	D112	D113	D114
S39	D115	D116	D117
S40	D118	D119	D120
S41	D121	D122	D123
S42	D124	D125	D126
S43	D127	D128	D129
S44	D130	D131	D132
S45	D133	D134	D135
S46	D136	D137	D138
S47	D139	D140	D141
S48	D142	D143	D144
S49	D145	D146	D147
S50	D148	D149	D150
S51	D151	D152	D153
S52	D154	D155	D156

1/2 Bias, 1/3 Duty Drive Technique



1/2 Bias, 1/3 Duty Waveforms

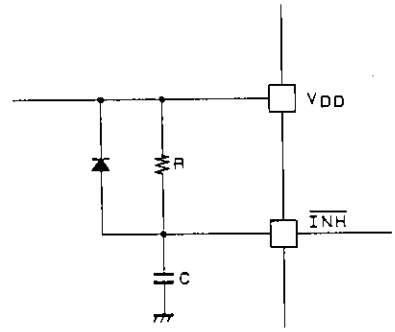
1/3 Bias, 1/3 Duty Drive Technique

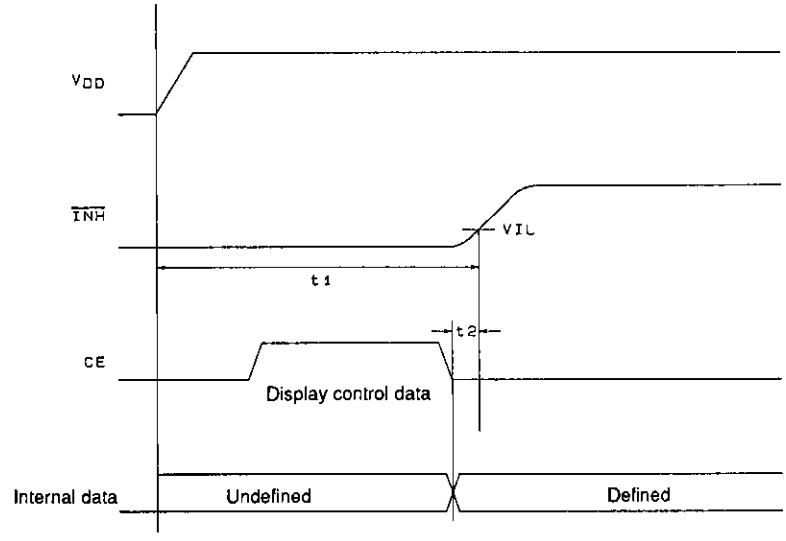


1/3 Bias, 1/3 Duty Waveforms

$\overline{\text{INH}}$ and Display Control

Since the IC internal data (D1 to D156, DR, SC, and BU) is undefined when power is first applied, $\overline{\text{INH}}$ should be set low at the same time as power is applied, and data should be transferred from the microprocessor while $\overline{\text{INH}}$ is held low. When the data transfer has completed, set $\overline{\text{INH}}$ high. This will prevent meaningless displays at power on.



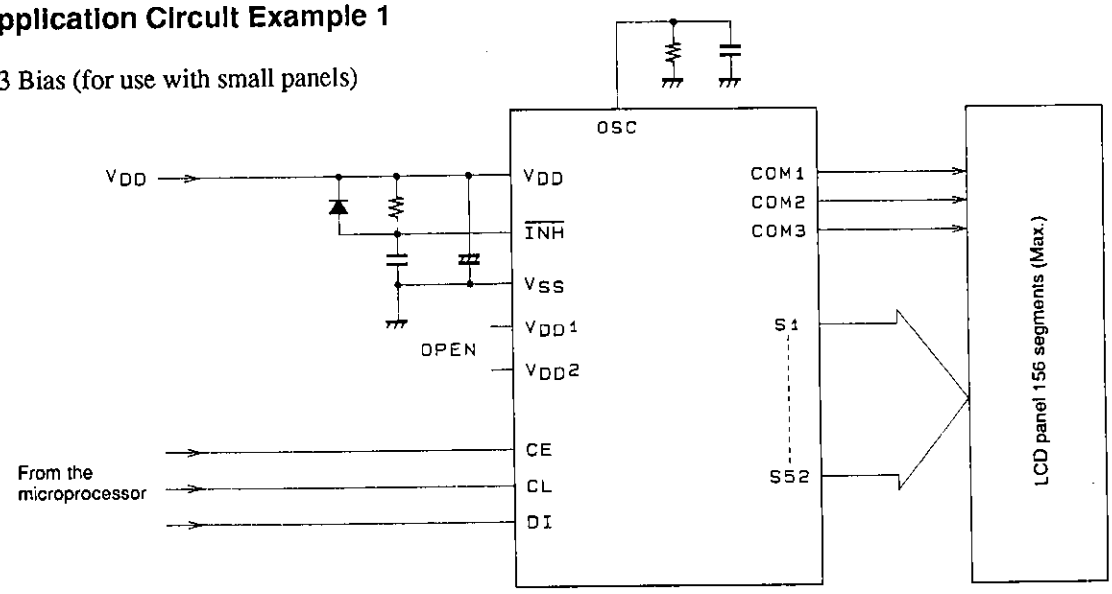


t1 .....Determined by the CR constant
t2.....10 μs (minimum)

Figure 3

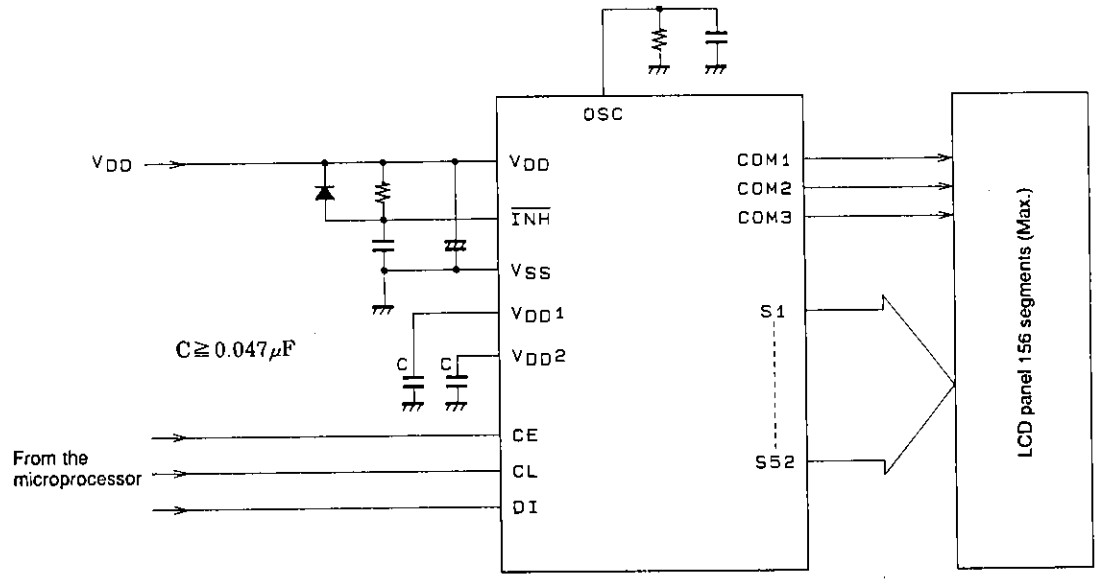
Application Circuit Example 1

1/3 Bias (for use with small panels)



Application Circuit Example 2

1/3 Bias (for use with normal size panels)



Application Circuit Example 3

1/3 Bias (for use with large panels)