Ordering number: EN3983

CMOS LSI

No. 3983

LC89583

Data Encoder for CD-WO and CD-MO

Overview

The LC89583 is a real-time CD data encoder IC designed for use with write-once and magneto-optical disks that comply with the Orange Book specifications.

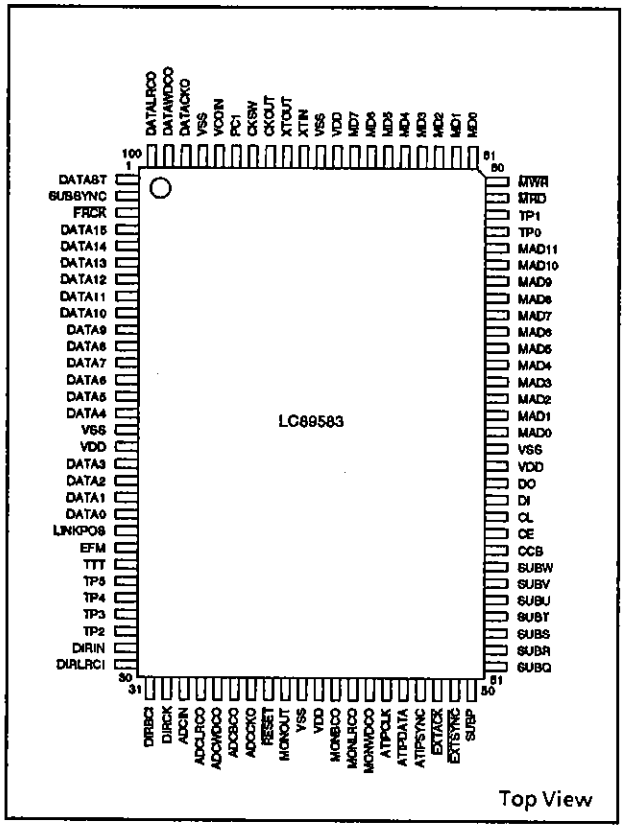
The LC89583 adds subcode data to the digital audio signals from an external A/D converter, a digital audio interface receiver or a CD-ROM encoder. The resulting data is converted to Cross Interleaved Reed-Solomon Code (CIRC) and encoded using eight-to-fourteen modulation (EFM).

The LC89583 operates from a 5 V supply and is available in 100-pin QIPs.

Features

- Two 16-bit serial data inputs
- One 16-bit parallel data input
- Clock signal generator for external A/D converters
- Data monitor circuit
- Mute circuit
- ATIP synchronization circuit
- Automatic ATIP data inserter
- Automatic power calibration area data generator
- CPU interface
- Single 5 V supply
- 100-pin QIP

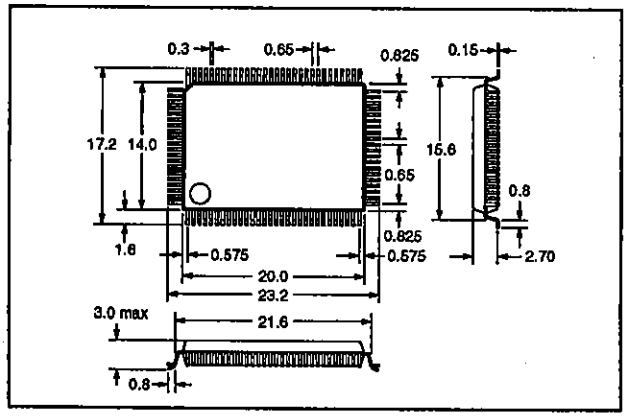
Pin Assignment



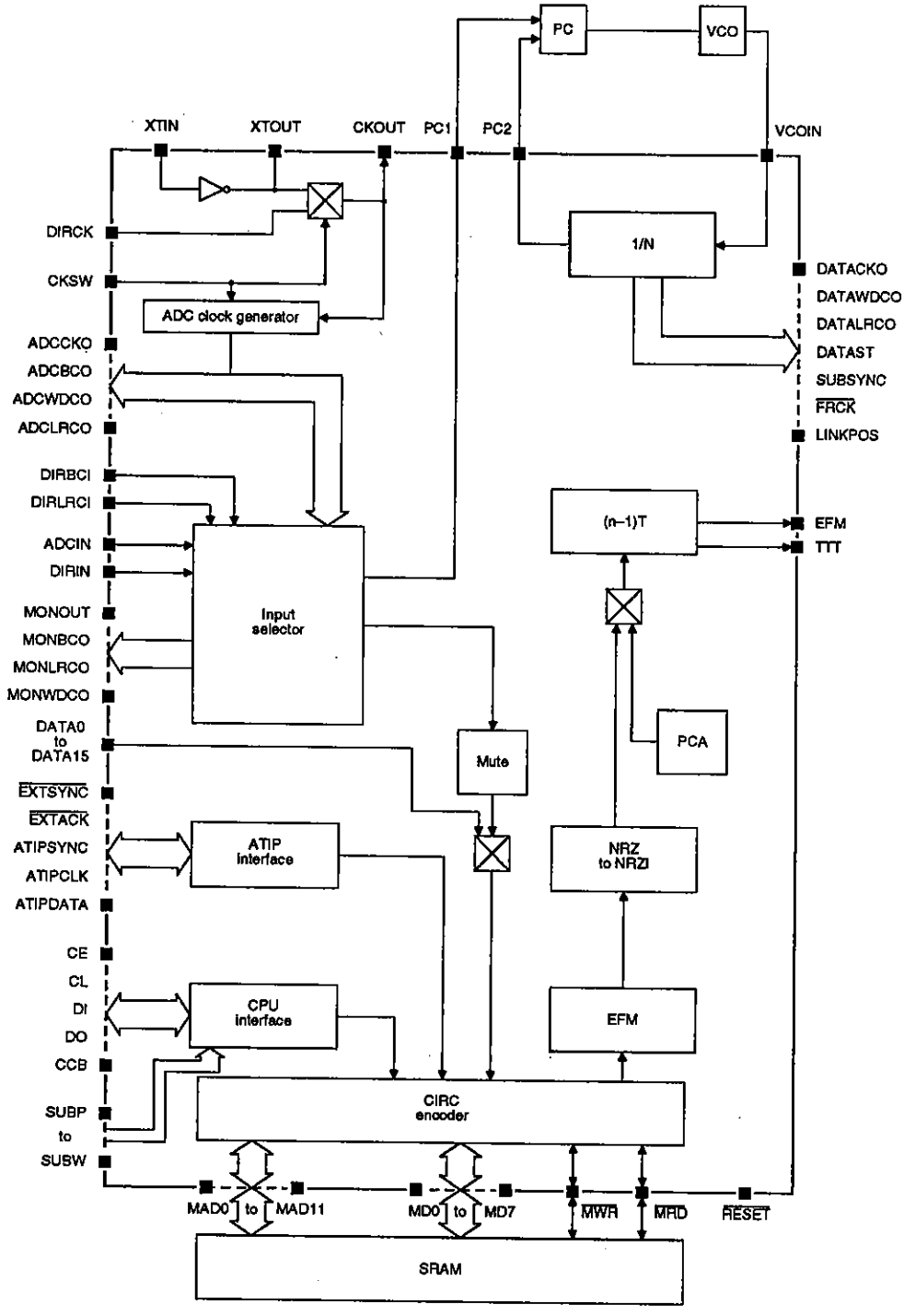
Package Dimensions

unit: mm

3151-QIP100E



Block Diagram



Pin Functions

Number	Name	Function
1	DATAST	SO clock output for the LC89581
2	SUBSYNC	Subcode synchronization signal output
3	$\overline{\text{FRCK}}$	7.35 kHz EFM frame clock output
4 to 15 and 18 to 21	DATA15 to DATA0	CD-ROM encoder data inputs
16, 40, 64, 90 and 97	VSS	Ground
17, 41, 63 and 89	VDD	Supply voltage
22	LINKPOS	Link position output
23	EFM	EFM non-return-to-zero-inverted (NRZI) CD-format serial output
24	TTT	Minimum-width signal detect output
25 to 27	TP5 to TP3	Test outputs
28, 77 and 78	TP2 to TP0	Test inputs. Tie LOW for normal operation.
29	DIRIN	Digital audio interface receiver data input
30	DIRLRCI	Digital audio interface receiver LR clock input
31	DIRBCI	Digital audio interface receiver 32fs or 64fs bit clock input
32	DIRCK	Digital audio interface receiver 384fs system clock input
33	ADCIN	External A/D converter serial data input
34	ADCLRCO	External A/D converter left/right clock output
35	ADCWDCO	External A/D converter 2fs word clock output
36	ADCBCO	External A/D converter 32fs or 64fs bit clock output
37	ADCCKO	External A/D converter 128fs system clock output
38	$\overline{\text{RESET}}$	System reset input
39	MONOUT	ADCIN or DIRIN data monitor output
42	MONBCO	Data monitor 32fs or 64fs bit clock output
43	MONLRCO	Data monitor left/right clock output
44	MONWDCO	Data monitor 2fs word clock output
45	ATIPCLK	ATIP data transfer clock input
46	ATIPDATA	ATIP data input
47	ATIPSYNC	ATIP synchronization signal input
48	$\overline{\text{EXTACK}}$	SUBSYNC synchronized output
49	$\overline{\text{EXTSYNC}}$	ATIPSYNC valid output
50	SUBP	P subcode input
51	SUBQ	Q subcode input
52	SUBR	R subcode input
53	SUBS	S subcode input
54	SUBT	T subcode input
55	SUBU	U subcode input
56	SUBV	V subcode input
57	SUBW	W subcode input

Number	Name	Function
58	CCB	CPU interface select input
59	CE	CPU interface chip enable input
60	CL	CPU interface clock input
61	DI	CPU interface data input
62	DO	CPU interface data output. Open-drain output
65 to 76	MAD0 to MAD11	External buffer memory address bus outputs
79	$\overline{MRD}$	External memory read output
80	$\overline{MWR}$	External memory write output
81 to 88	MD0 to MD7	External buffer memory bidirectional data bus
91	XTIN	16.9344 MHz, 384fs crystal oscillator amplifier input
92	XTOUT	16.9344 MHz, 384fs crystal oscillator amplifier output
93	CKOUT	System clock output
94	CKSW	System clock select input
95	PC1	44.1 kHz phase comparator clock output
96	VCOIN	8.6436 MHz, 196fs VCO clock input
98	DATACKO	CD-ROM encoder data clock output
99	DATAWDCO	CD-ROM encoder word clock output
100	DATALRCO	CD-ROM left/right parallel data clock output

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage range	V_{DD}	–0.3 to 7.0	V
Input voltage range	V_I	–0.3 to V_{DD} + 0.3	V
Output voltage range	V_O	–0.3 to V_{DD} + 0.3	V
Operating temperature range	Topr	–30 to 70	°C
Storage temperature range	T_{stg}	–55 to 125	°C
Solder temperature	T_{sld}	260	°C
Soldering duration	t_{sld}	10	s

Recommended Operating Conditions

T_a = 25 °C

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	5	V
Supply voltage range	V_{DD}	4.5 to 5.5	V

Electrical Characteristics

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = −30 to 70 °C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
LOW-level input voltage for all inputs other than XTIN	V_{IL1}		–	–	0.8	V
HIGH-level input voltage for all inputs other than XTIN	V_{IH1}		2.2	–	–	V
XTIN LOW-level input voltage	V_{IL2}		–	–	$0.3V_{DD}$	V
XTIN HIGH-level input voltage	V_{IH2}		$0.7V_{DD}$	–	–	V
LOW-level output voltage for all outputs other than XTOUT	V_{OL}	I_{OL} = 3 mA	–	–	0.4	V
HIGH-level output voltage for all outputs other than XTOUT and DO	V_{OH}	I_{OH} = 3 mA	2.4	–	–	V

Functional Description

CPU Interface

The CPU interface uses the Sanyo C²B serial bus format.

When CCB is HIGH, command input and data output are selected by the eight chip address bits—B0 to B3 and A0 to A3. When the chip address is 78H, the command input mode is selected. When the chip address is 79H, the data output mode is selected.

When CCB is LOW, no chip address is required.

Commands comprise four address bits and four data bits which are written to the selected command registers.

Command registers

Command address				Command register			
D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	RESET	LPSW	−1T	+N
0	0	0	1	DIRISW2	ADCISW	DIRISW	MONISW
0	0	1	0	0	0	0	MON1
0	0	1	1	0	0	IN2	IN1
0	1	0	0	$\overline{\text{MUTE4}}$	$\overline{\text{MUTE3}}$	$\overline{\text{MUTE2}}$	$\overline{\text{MUTE1}}$
0	1	0	1	EFM-ENABLE	0	PCA/$\overline{\text{EFM}}$	3T/$\overline{\text{11T}}$
0	1	1	0	Q	P	ATIP	LDIN/$\overline{\text{PROG}}$
0	1	1	1	0	0	SUBP	80SUBQ
1	0	0	0	MA3	MA2	MA1	MA0
All other combinations				Reserved for test purposes			

RESET

When RESET is set, all circuitry is initialized with the exception of the command registers. The default state is cleared.

LPSW

The delay between SUBSYNC and LINKPOS is determined by the state of LPSW. When LPSW is set, the delay is 25 EFM frames. When LPSW is cleared, the delay is 24 EFM frames. The default state is cleared.

−1T

When −1T is set, the width of the EFM signal pulses is reduced by 1T. The default state is cleared.

+N

When +N is set, the width of the minimum-width EFM signal pulses is increased by 60 ns. The default state is cleared.

DIRISW and DIRISW2

DIRISW and DIRISW2 specify the digital interface receiver mode. If DIRISW2 is set, DIRISW must be cleared. The default state for both registers is cleared.

ADCISW

ADCISW specifies the A/D converter interface mode. The default state is cleared.

MONISW

MONISW specifies the monitor interface mode. The default state is cleared.

MON1

MON1 specifies the monitor output source. When MON1 is set, the digital interface receiver signal becomes the source. When MON1 is cleared, the external A/D converter becomes the source. The default state is cleared.

IN1 and IN2

IN1 and IN2 specify the encoded signal source as shown in table 1. The default state for both registers is cleared.

Table 1. IN1 and IN2 select

IN1	IN2	Signal source
LOW	LOW	External A/D converter
x	HIGH	CD-ROM encoder
HIGH	LOW	Digital interface receiver

Note
x = don't care

$\overline{\text{MUTE1}}$

When $\overline{\text{MUTE1}}$ is set, the fade mute function is disabled. The default state is set.

$\overline{\text{MUTE2}}$

When $\overline{\text{MUTE2}}$ is set, the zero-cross mute function is disabled. The default state is set.

$\overline{\text{MUTE3}}$

When $\overline{\text{MUTE3}}$ is cleared, data 42 dB below the maximum level is muted. The default state is set.

$\overline{\text{MUTE4}}$

When $\overline{\text{MUTE4}}$ is set, the unconditional mute is disabled. The default state is cleared.

EFM-ENABLE

When EFM-ENABLE is set, the EFM signal appears on EFM. When EFM-ENABLE is cleared, EFM outputs a continuous LOW-level signal. The default state is cleared.

PCA/$\overline{\text{EFM}}$

When PCA/$\overline{\text{EFM}}$ is cleared, the EFM signal appears on EFM. When PCA/$\overline{\text{EFM}}$ is set, the power calibration signal appears on EFM. The default state is cleared.

3T/$\overline{\text{11T}}$

When 3T/$\overline{\text{11T}}$ is set, the power calibration period is 3T. When 3T/$\overline{\text{11T}}$ is cleared, the power calibration period is 11T. The default state is cleared.

Q

When Q is set, the Q subcodes are input on DI in 80-bit blocks for each subcode frame. When Q is cleared, the Q subcodes are entered on SUBQ as single bits for each EFM frame. The default state is cleared.

P

When P is set, the P subcodes are input on DI in 80-bit blocks for each subcode frame. When P is cleared, the P subcodes are entered on SUBP as single bits for each EFM frame. The default state is cleared.

ATIP

When ATIP is set, the ATIP data is automatically inserted into the subcode data. The default state is cleared.

LDIN/$\overline{\text{PROG}}$

When LDIN/$\overline{\text{PROG}}$ is cleared, the ATIP data is inserted into the AMIN, ASEC and AFRAME subcode positions. When LDIN/$\overline{\text{PROG}}$ is set, the ATIP data is inserted into the MIN, SEC and FRAME positions. The default state is cleared.

SUBP

When P is set, SUBP specifies the P subcode value. The default state is cleared.

80SUBQ

When 80SUBQ is set, the next 80 bits of data on DI are treated as the Q subcode data for the whole subcode frame. The Q subcode data length is 56 bits if ATIP data is being inserted. The data is input least-significant bit first.

MA0 to MA3

MA0 to MA3 specify the monitor address. The default value is 0000.

The monitor address allows access to the data shown in table 2.

Table 2. Monitor data

Monitor address	Monitor data							
	DO0	DO1	DO2	DO3	DO4	DO5	DO6	DO7
0000	0	0	LM11	LM8	0	0	1	RSTSYS

RSTSYS

RSTSYS holds the contents of the RESET register.

LM8

LM8 indicates whether the upper 8 bits of the selected source data have been all LOW or HIGH since the last monitor readout.

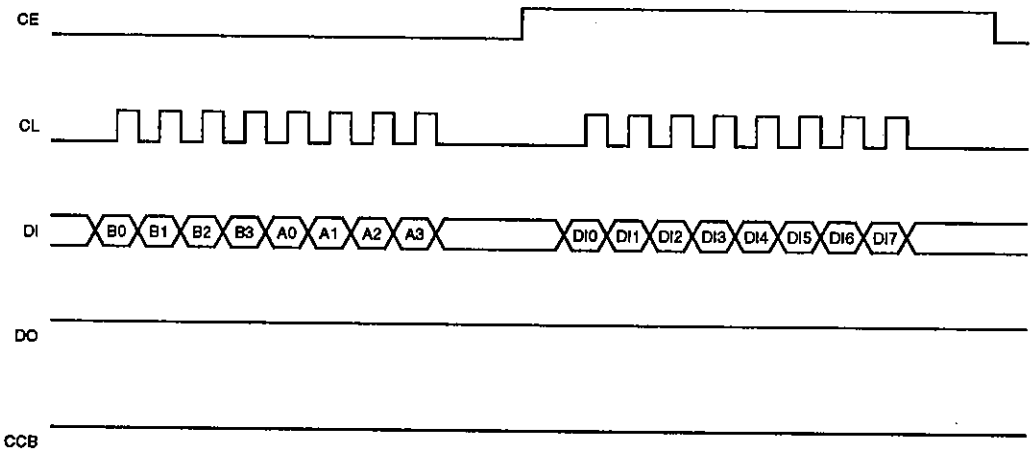
LM11

LM11 indicates whether the upper 11 bits of the selected source data have been all LOW or HIGH since the last monitor readout.

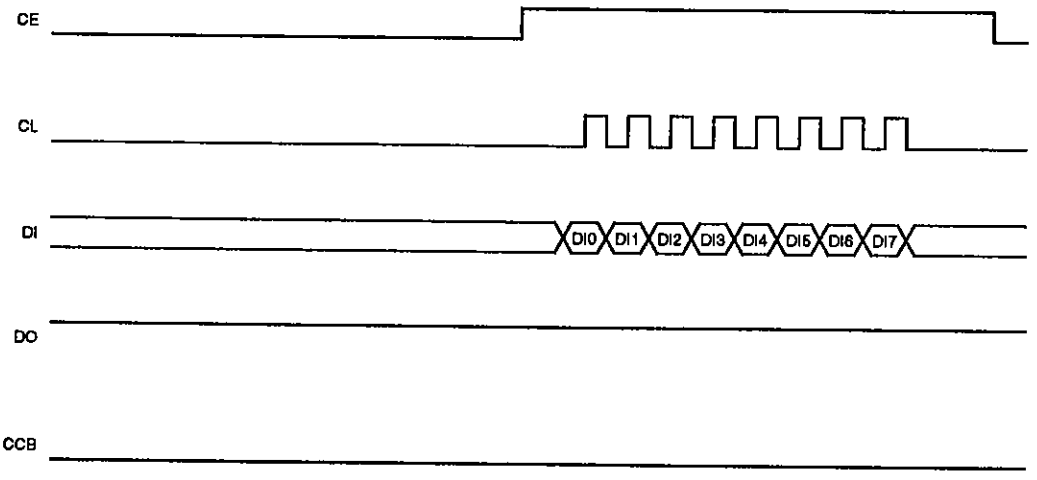
CPU interface waveforms

Command Input waveforms

CCB = HIGH

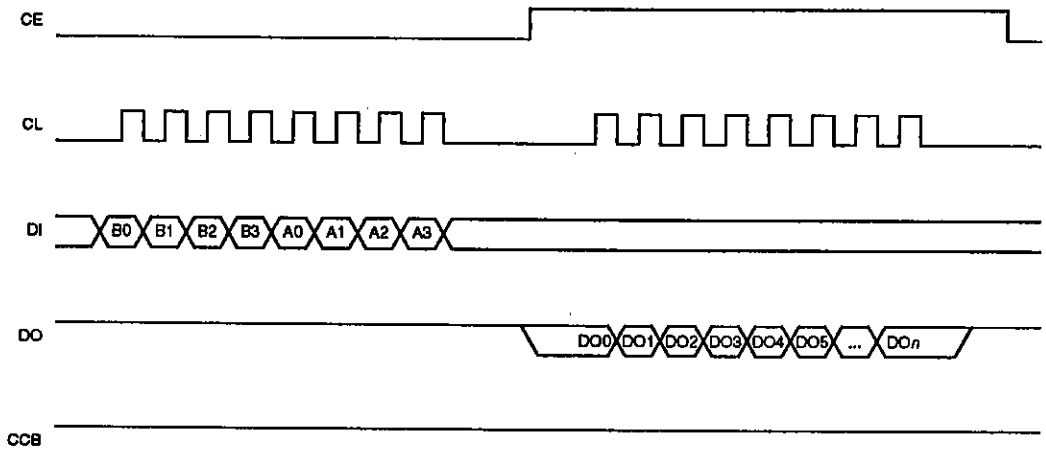


CCB = LOW

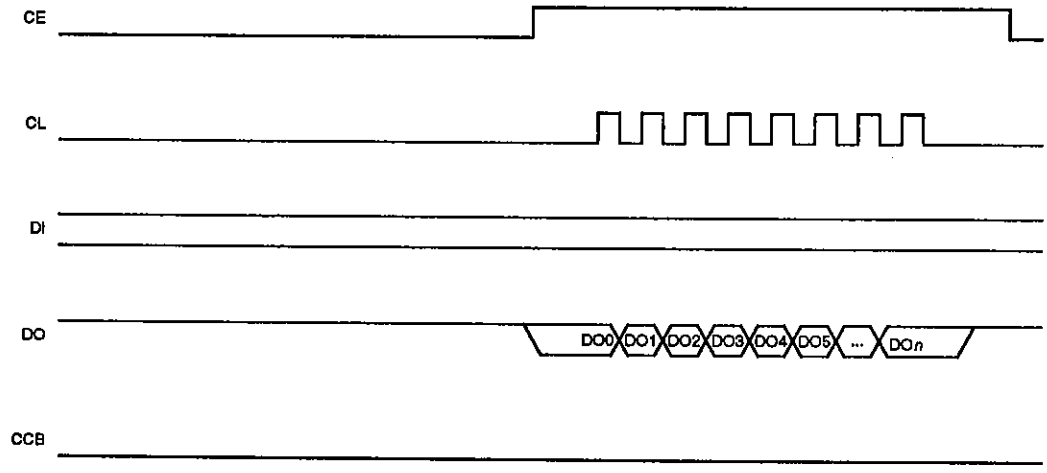


Data output waveforms

CCB = HIGH

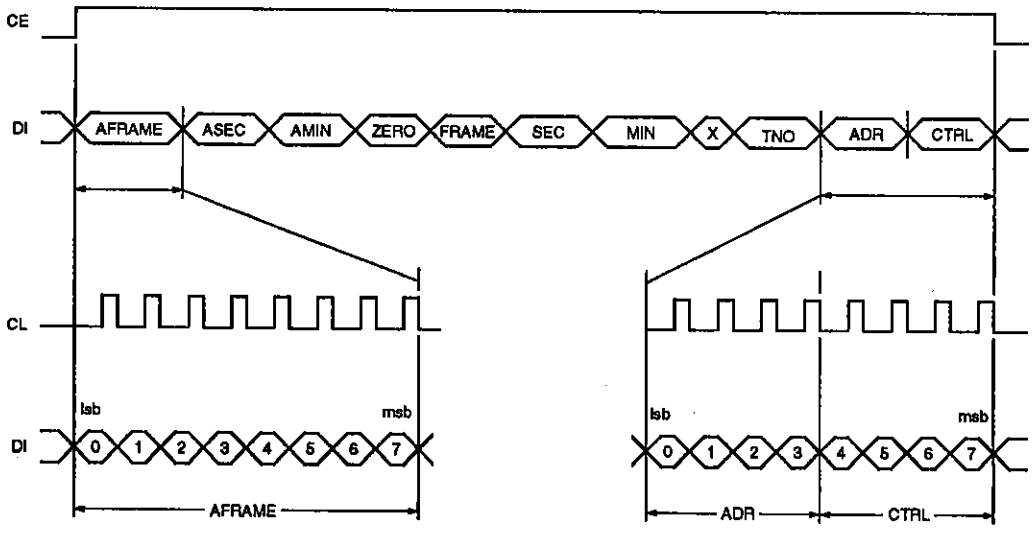


CCB = LOW

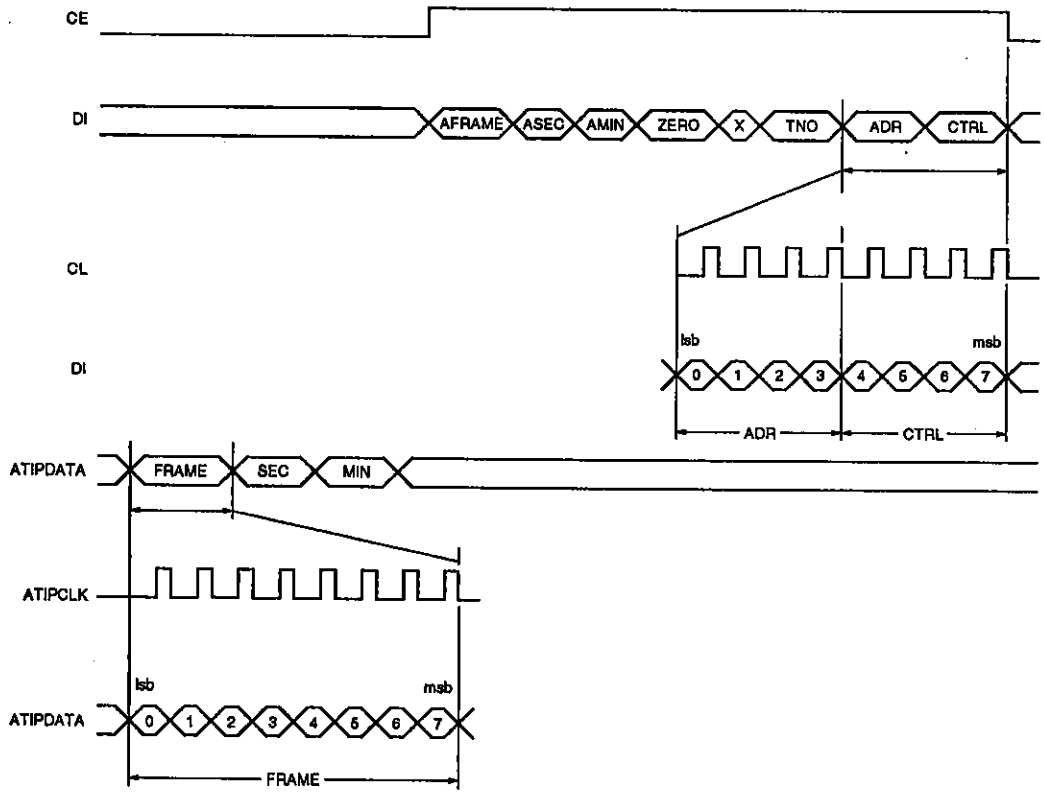


Q subcode data input waveforms

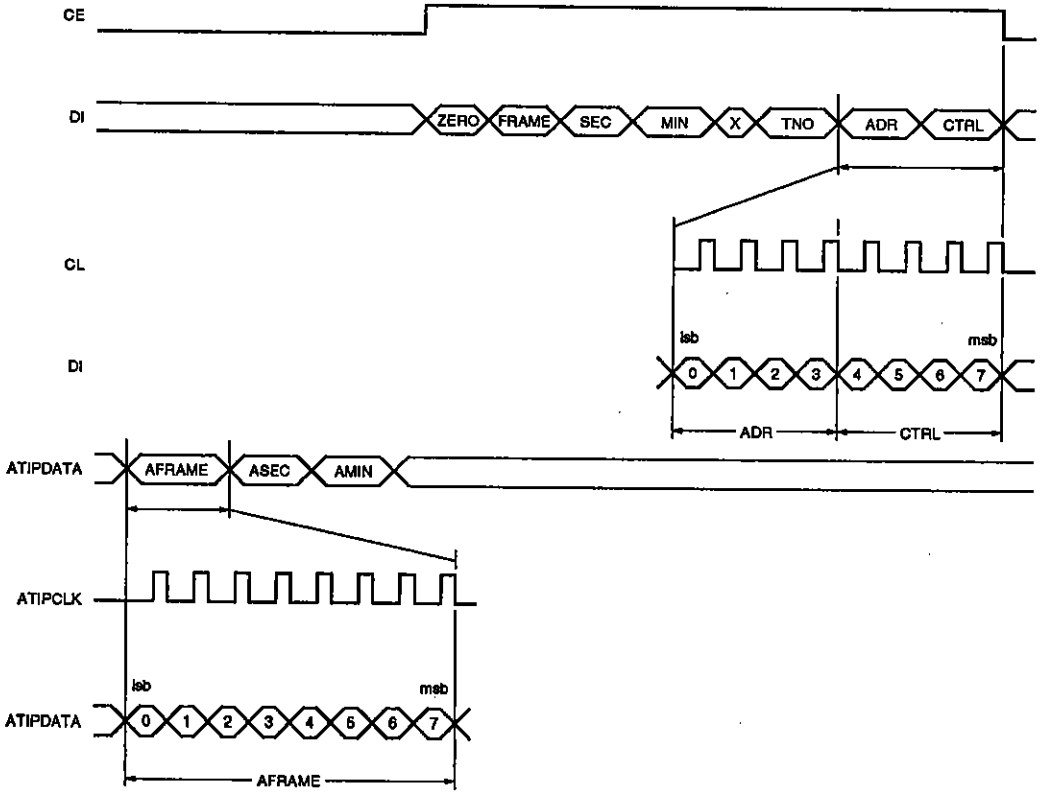
ATIP = LOW



ATIP = LDIN/$\overline{\text{PROG}}$ = HIGH



ATIP = HIGH, LDIN/$\overline{\text{PROG}}$ = LOW

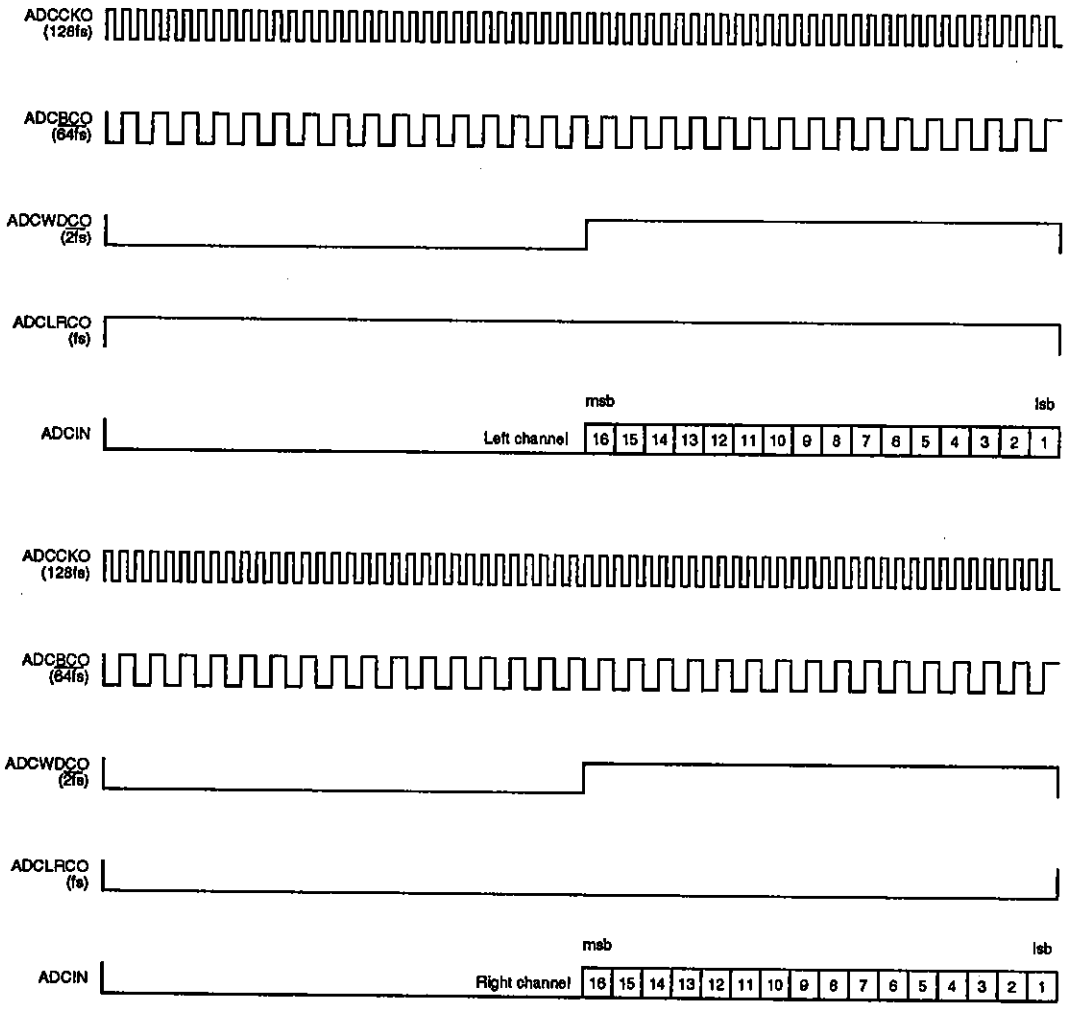


A/D Converter Interface

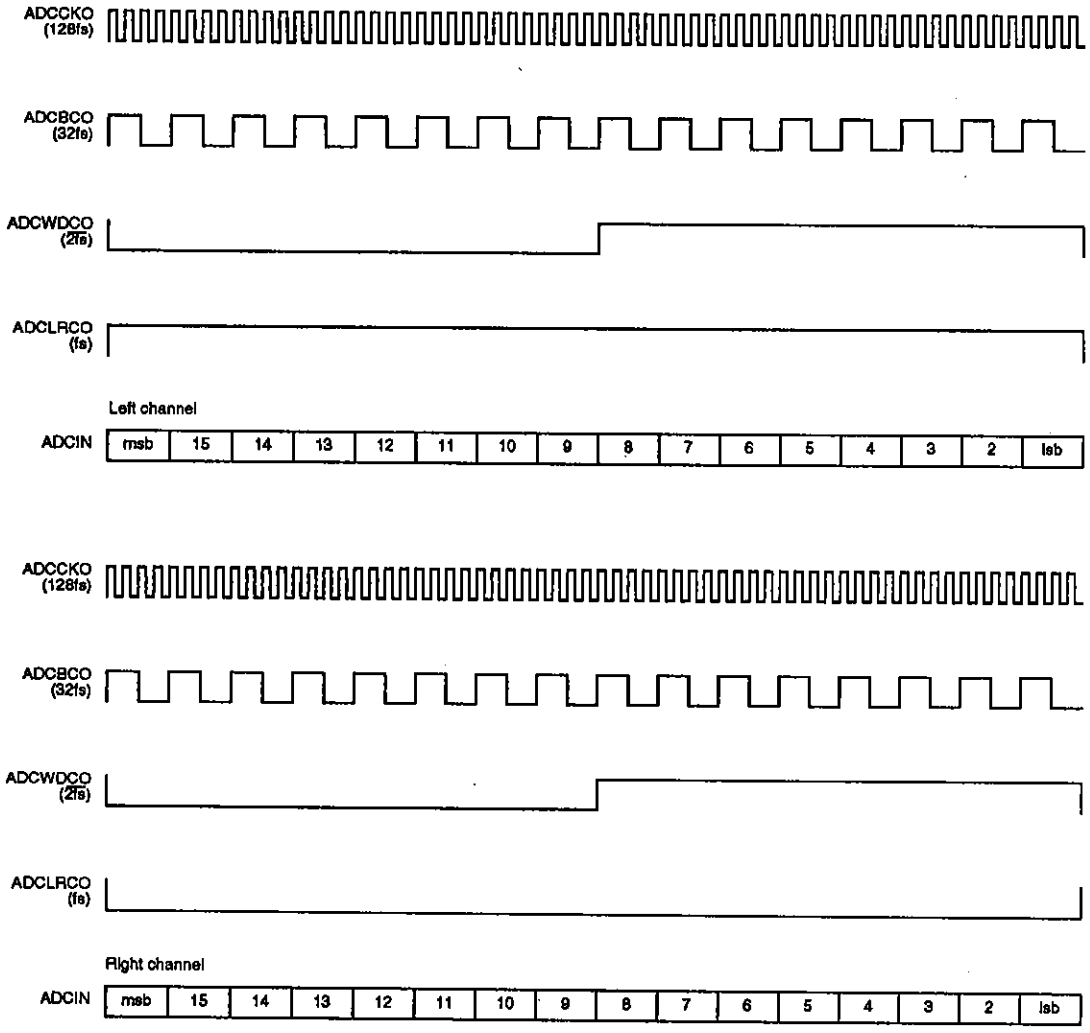
Two A/D converter interfaces are supported. The interface is selected by the state of ADCISW. When ADCISW is cleared, the LC89583 can be connected directly to the LC7886 A/D converter.

A/D converter interface waveforms

ADCISW = LOW



ADCISW = HIGH

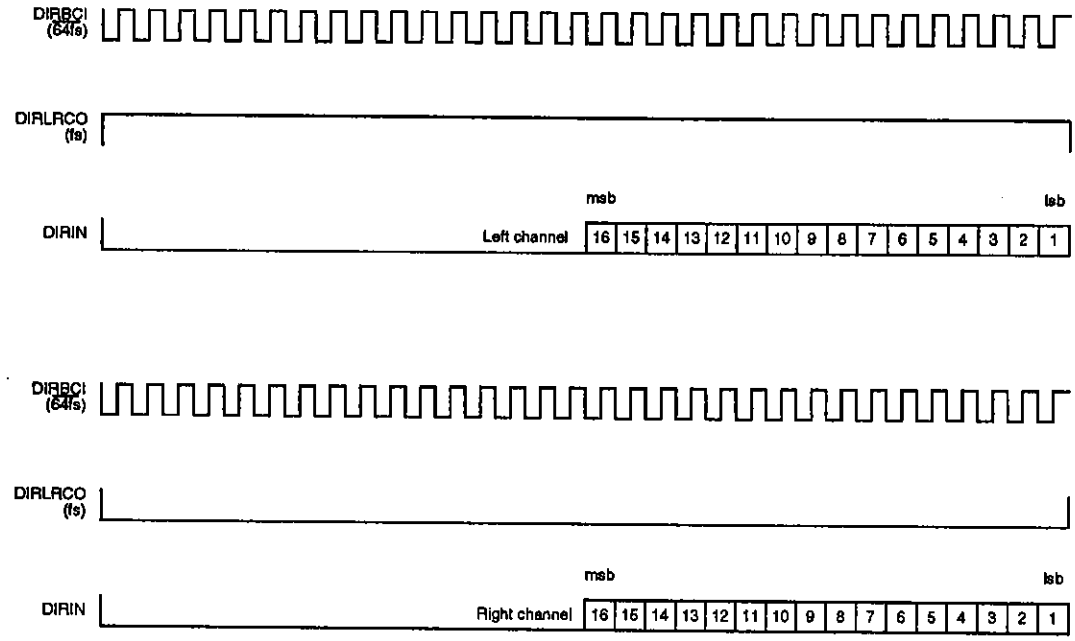

ADCCKO (128fs)
ADCBCO (32fs)
ADCWDCO (2fs)
ADCLRCO (fs)
Left channel
ADCIN
msb 15 14 13 12 11 10 9 8 7 6 5 4 3 2 lsb
ADCCKO (128fs)
ADCBCO (32fs)
ADCWDCO (2fs)
ADCLRCO (fs)
Right channel
ADCIN
msb 15 14 13 12 11 10 9 8 7 6 5 4 3 2 lsb

Digital Interface Receiver (DIR)

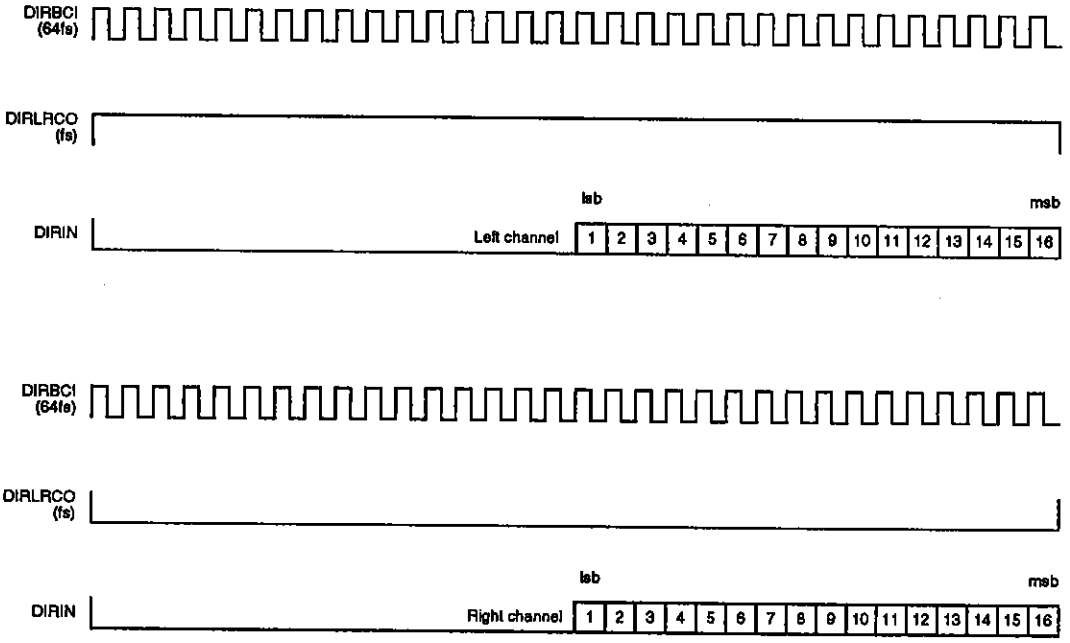
Three DIR modes are supported. The mode is selected by the state of DIRISW and DIRISW2. When DIRISW and DIRISW2 are cleared, the LC89583 can be connected directly to the LC8900K digital interface receiver.

DIR interface waveforms

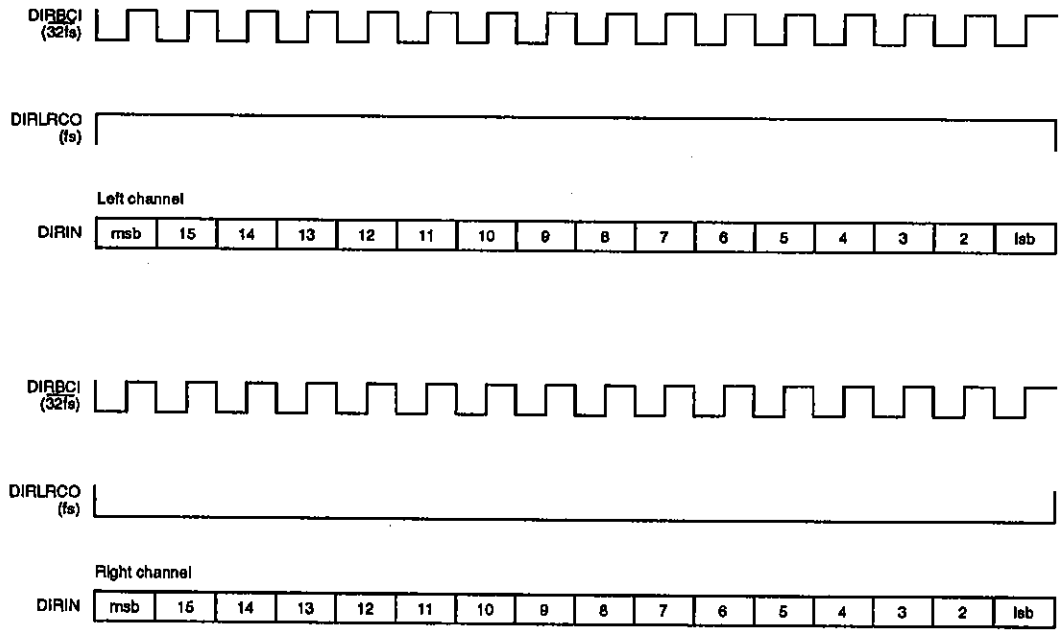
DIRISW = DIRISW2 = LOW



DIRISW = HIGH, DIRISW2 = LOW



DIRISW = LOW, DIRISW2 = HIGH

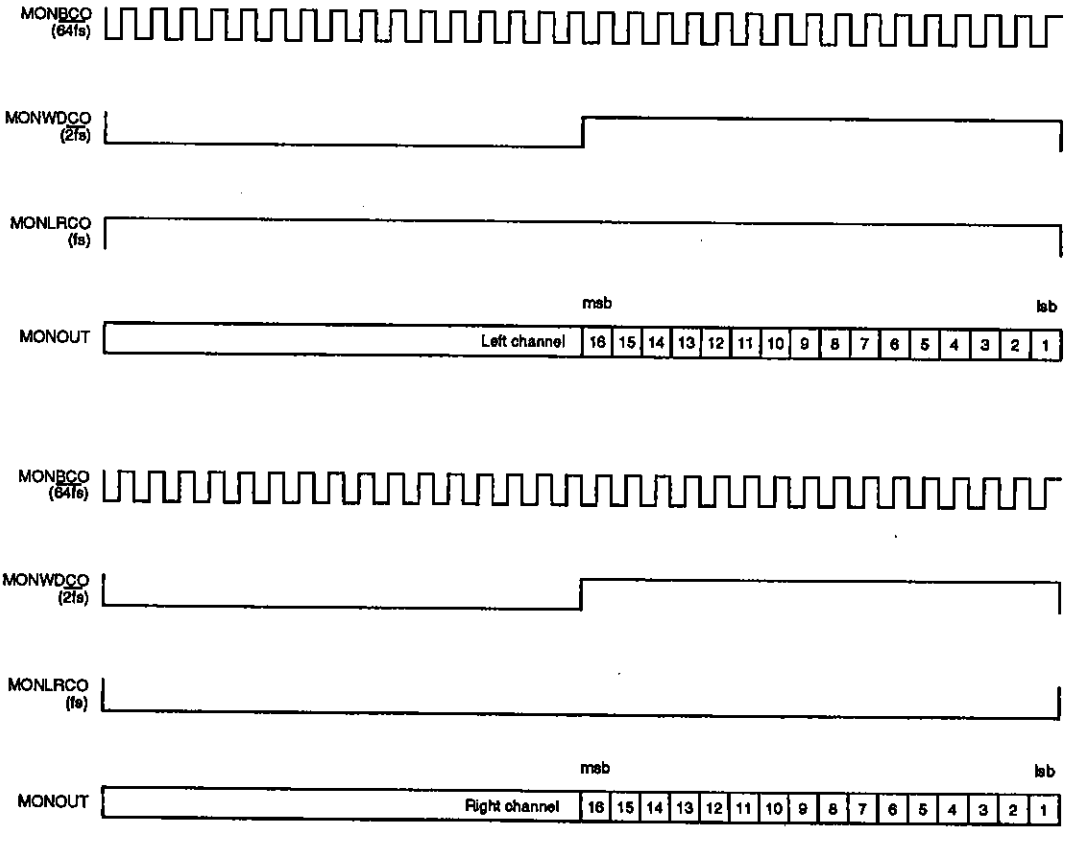


Monitor Interface

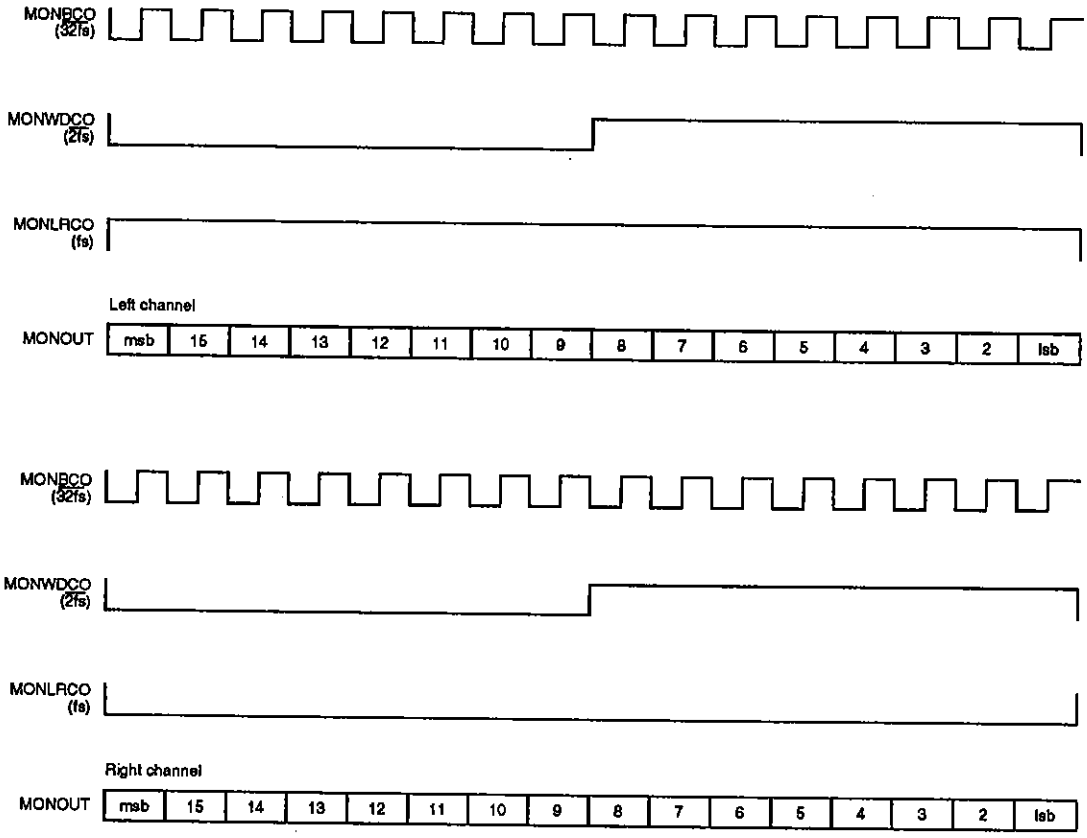
Two monitor interface modes are supported. The mode is selected by the state of MONISW. When MONISW is cleared, the LC89583 can be connected directly to the LC7881 D/A converter.

Monitor Interface waveforms

MONISW = LOW

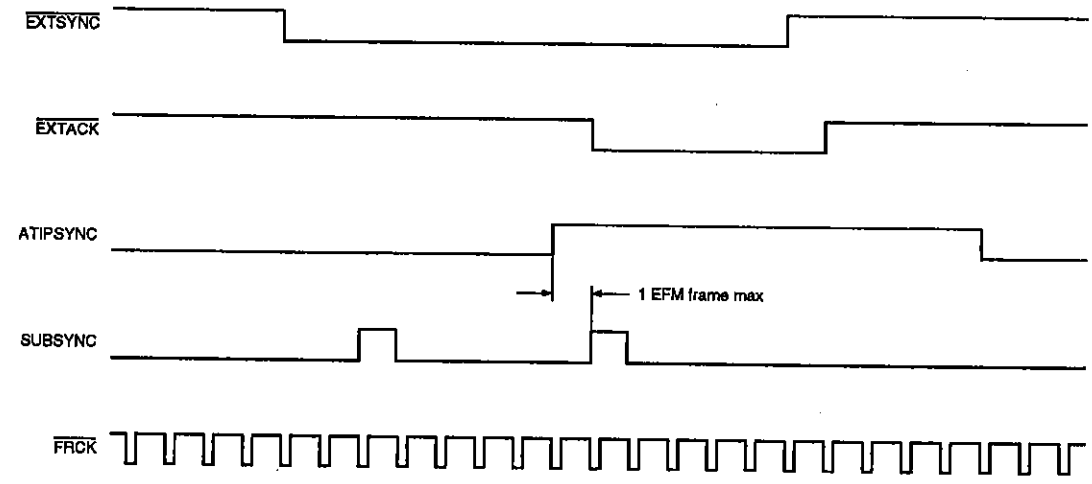


MONISW = HIGH



Synchronizing SUBSYNC with ATIPSYNC

When $\overline{\text{EXTSYNC}}$ is LOW, the LC89583 synchronizes the SUBSYNC output signal with the signal on ATIPSYNC. When ATIPSYNC and $\overline{\text{EXTSYNC}}$ are synchronized, $\overline{\text{EXTACK}}$ goes LOW as shown in the following figure. When $\overline{\text{EXTSYNC}}$ is HIGH, $\overline{\text{EXTACK}}$ remains HIGH.



DESIGN NOTES

- The S0 clock signal from DATAST is output three EFM frames ahead of the signal from SUBSYNC.
- SUBSYNC provides the subframe synchronization signal during each EFM frame.
- When a minimum-width EFM signal (2 or 3T ±1T) is detected, TTT goes HIGH, allowing external hardware to increase the write energy by 10%.
- $\overline{\text{EXTACK}}$ goes LOW when SUBSYNC is synchronized with ATIPSYNC.
- CKSW selects the source of the clock signal output on CKOUT. When CKSW is LOW, XTIN is output on CKOUT. When CKSW is HIGH, DIRCK is output on CKOUT.