Ordering number: EN ※ 5042

CMOS LSI

SANYO

No. ※ 5042

LC8214

Facsimile Controller

Preliminary

Overview

The LC8214 is a facsimile controller comprising a CPU, CPU peripheral circuits, image processor, dot change detector for image data compression and expansion, thermal print head interface, I/O ports and other facsimile functions on a single chip. It can be connected to 9,600bps modem (LC8920, LC89201) or 14.4Kbps modem (LC8921) modem and RAM, ROM, LCD controller and other circuits to form a high-performance, low-cost facsimile system.

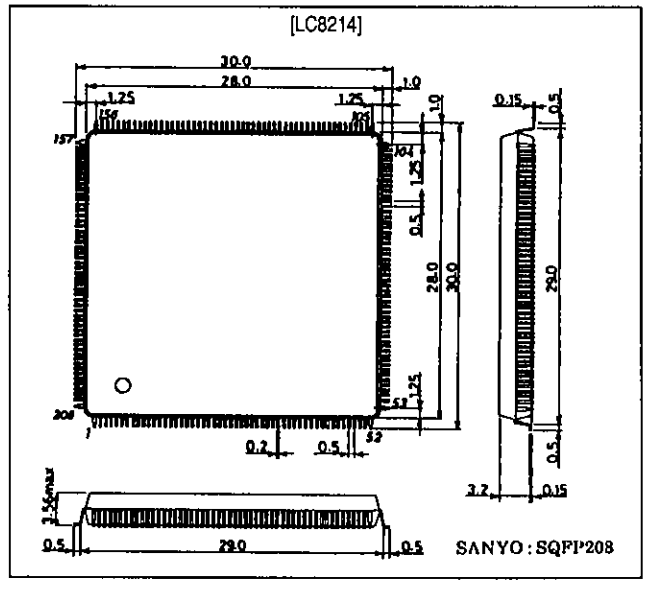
Features

- High-speed 16-bit CPU (65C816), 8MHz cycle
- 16MB program space
- MH/MR/MMR format encoding
- 64-gradation half-tone processing (dither method, error diffusion method)
- Image content separation (character, pictures, screens)
- 8Kpels/line image processing
- Shading correction for all pels
- AGC, 8-bit A/D converter
- Picture element density conversion
- TPH interface (strobe division: 1, 2, and 4 strobe, latchless head)
- Transmit/receive stepping motor interface
- 5-channel 16-bit timer
- 6-channel DMA controller (4MB/s max.)
- 6 to 69 I/O ports
- Single 5V supply
- CMOS process for low-power dissipation

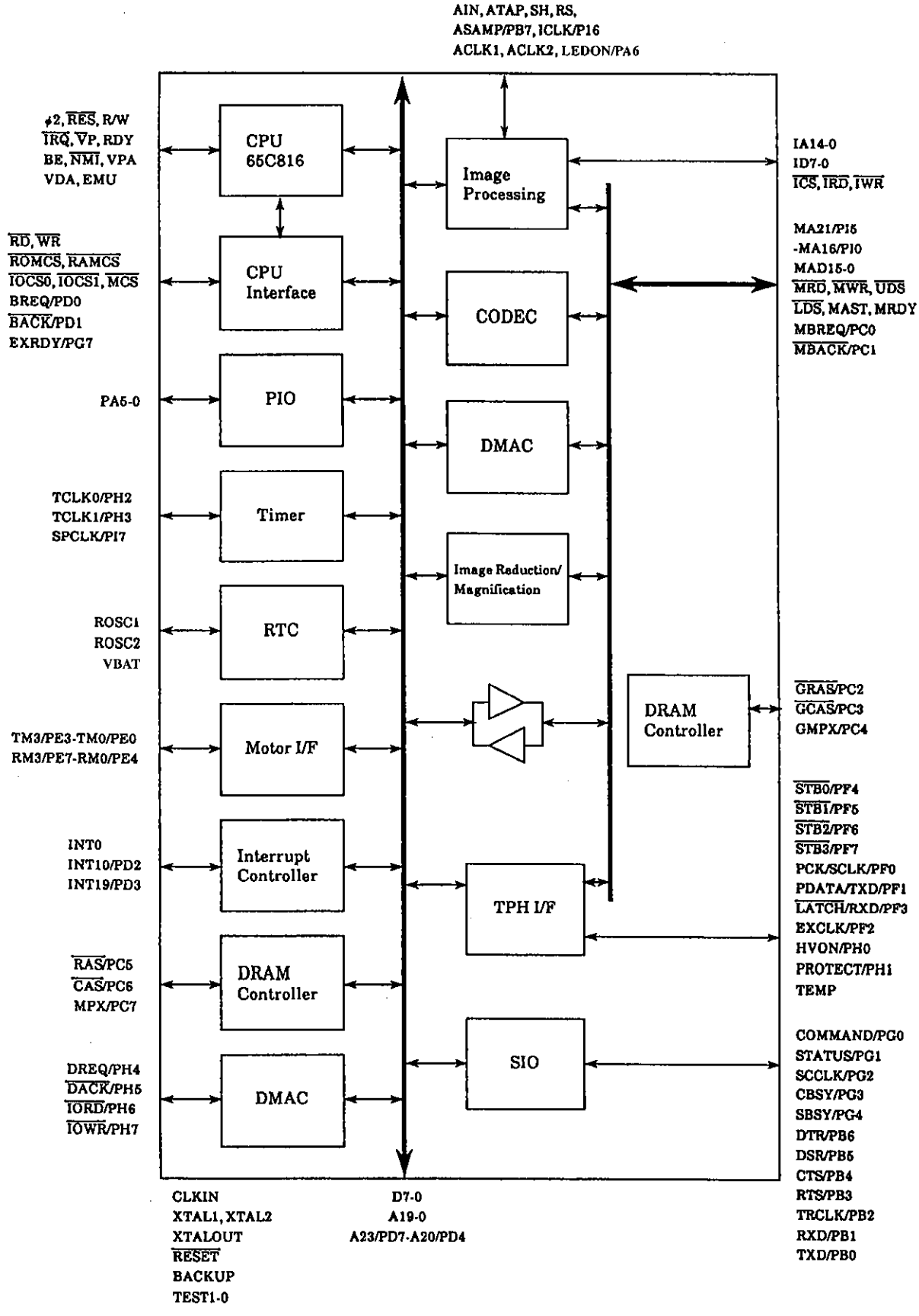
Package Dimensions

Unit: mm

3210-SQFP208



Block Diagram



Pin Assignment

Number	Name	I/O[1]	Function
1	V_{SS}	P	Ground connection pin
2	$\overline{RESET}$	I	Reset signal
3	$\overline{RD}$	O	Read signal from CPU
4	$\overline{WR}$	O	Write signal from CPU
5	$\overline{ROMCS}$	O	Program ROM chip select signal
6	$\overline{RAMCS}$	O	Work RAM chip select signal
7	INT0	I	External interrupt request signals
8	D7	B	Data bus
9	D6	B	
10	D5	B	
11	D4	B	
12	D3	B	
13	D2	B	
14	D1	B	
15	D0	B	
16	V_{DD}	P	Supply pin
17	V_{SS}	P	Ground connection pin
18	$\overline{IOCS0}$	O	External I/O chip select signals
19	$\overline{IOCS1}$	O	
20	$\overline{MCS}$	O	
21	INT19/PD3	B	External interrupt request signals/General-purpose port D
22	INT10/PD2	B	
23	EMU	I	ICE monitor in-operation signal
24	A23/PD7	B	Address bus/General-purpose port D
25	A22/PD6	B	
26	A21/PD5	B	
27	A20/PD4	B	
28	A19	O	Address bus
29	A18	O	
30	A17	O	
31	A16	O	
32	$\overline{RES}$	O	ICE reset signal
33	R/W	I	ICE read/write signal
34	V_{DD}	P	Supply pin
35	V_{SS}	P	Ground connection pin
36	$\phi 2$	O	ICE system clock
37	$\overline{IRQ}$	O	ICE interrupt request signal
38	$\overline{VP}$	B	ICE vector address signal
39	RDY	O	ICE ready signal
40	BE	O	ICE bus enable signal
41	VPA	I	ICE valid program address signal
42	VDA	I	ICE valid data address signal
43	$\overline{NMI}$	I	Non-maskable interrupt request signal

Number	Name	I/O[1]	Function
44	A15	O	Address bus
45	A14	O	
46	A13	O	
47	A12	O	
48	A11	O	
49	A10	O	
50	A9	O	
51	A8	O	
52	V_{DD}	P	Supply pin
53	V_{SS}	P	Ground connection pin
54	A7	O	Address bus
55	A6	O	
56	A5	O	
57	A4	O	
58	A3	O	
59	A2	O	
60	A1	O	
61	A0	O	
62	$\overline{BACK}$/PD1	B	CPU bus acknowledge signal/General-purpose port D
63	BREQ/PD0	B	CPU bus request signal/General-purpose port D
64	$\overline{IOWR}$/PH7	B	External I/O device write signal/General-purpose port H
65	$\overline{IORD}$/PH6	B	External I/O device read signal/General-purpose port H
66	$\overline{DACK}$/PH5	B	External I/O device DMA acknowledge signal/General-purpose port H
67	DREQ/PH4	B	External I/O device DMA request signal/General-purpose port H
68	V_{DD}	P	Supply pin
69	V_{SS}	P	Ground connection pin
70	PROTECT/PH1	B	Head protection abnormality signal input/General-purpose port H
71	HVON/PH0	B	Head voltage ON/OFF control signal/General-purpose port H
72	EXRDY/PA7	B	External ready signal/General-purpose port A
73	LEDON/PA6	B	LED ON control signal/General-purpose port A
74	PA5	B	General-purpose port A
75	PA4	B	
76	PA3	B	
77	PA2	B	
78	PA1	B	
79	PA0	B	
80	TCLK1/PH3	B	Timer external clock inputs/General-purpose port H
81	TCLK0/PH2	B	
82	EXCLK/PF2	B	TPH control external clock/General-purpose port F
83	MPX/PC7	B	DRAM address multiplexed signal/General-purpose port C
84	$\overline{CAS}$/PC6	B	DRAM address strobes/General-purpose port C
85	$\overline{RAS}$/PC5	B	
86	V_{DD}	P	Supply pin
87	V_{SS}	P	Ground connection pin

Number	Name	I/O[1]	Function
88	XTAL1	I	Crystal oscillator connection pins
89	XTAL2	O	
90	XTALOUT	O	Clock output
91	CLKIN	I	System clock input
92	ASAMP/PB7	B	Sampling point monitor signal/General-purpose port B
93	DTR/PB6	B	8251 interface/General-purpose port B
94	DSR/PB5	B	
95	CTS/PB4	B	
96	RTS/PB3	B	
97	TRCLK/PB2	B	
98	RXD/PB1	B	
99	TXD/PB0	B	
100	VBAT	P	Backup supply pin
101	$\overline{\text{BACKUP}}$	I	Power-down signal
102	ROSC1	I	RTC crystal oscillator connection pins
103	ROSC2	O	
104	V_{DD}	P	Supply pin
105	V_{SS}	P	Ground connection pin
106	$\overline{\text{STB3}}$/PF7	B	TPH strobe signals/General-purpose port F
107	$\overline{\text{STB2}}$/PF6	B	
108	$\overline{\text{STB1}}$/PF5	B	
109	$\overline{\text{STB0}}$/PF4	B	
110	$\overline{\text{LATCH}}$/RXD/PF3	B	TPH data latch signal/Serial I/O receive data/General-purpose port F
111	PDATA/TXD/PF1	B	TPH output data/Serial I/O transmit data/General-purpose port F
112	PCK/SCLK/PF0	B	TPH data transmission clock/Serial I/O clock/General-purpose port F
113	IA14	O	Image processor memory address bus
114	IA13	O	
115	IA12	O	
116	IA11	O	
117	IA10	O	
118	IA9	O	
119	IA8	O	
120	V_{DD}	P	Supply pin
121	V_{SS}	P	Ground connection pin
122	IA7	O	Image processor memory address bus
123	IA6	O	
124	IA5	O	
125	IA4	O	
126	IA3	O	
127	IA2	O	
128	IA1	O	
129	IA0	O	
130	$\overline{\text{IRD}}$	O	Image processor memory read signal
131	$\overline{\text{IWR}}$	O	Image processor memory write signal
132	$\overline{\text{ICS}}$	O	Image processor memory chip select

Number	Name	I/O[1]	Function
133	SH	O	Image sensor start pulse
134	RS	O	Image sensor reset pulse
135	ACLK1	O	Image sensor transmission clocks
136	ACLK2	O	
137	ICLK/PI6	B	Image processor external clock/General-purpose port I
138	V_{DD}	P	Supply pin
139	V_{SS}	P	Ground connection pin
140	ID7	B	Image processor memory data bus
141	ID6	B	
142	ID5	B	
143	ID4	B	
144	ID3	B	
145	ID2	B	
146	ID1	B	
147	ID0	B	
148	RM3/PE7	B	Receive motor phase signals/General-purpose port E
149	RM2/PE6	B	
150	RM1/PE5	B	
151	RM0/PE4	B	
152	TM3/PE3	B	Transmit motor phase signals/General-purpose port E
153	TM2/PE2	B	
154	TM1/PE1	B	
155	TM0/PE0	B	
156	V_{DD}	P	Supply pin
157	V_{SS}	P	Ground connection pin
158	AV_{DD}	P	Analog supply pin
159	AIN	I	Analog image signal input
160	TEMP	I	Thermistor input
161	ATAP	I	Built-in A/D converter reference voltage
162	AV_{SS}	P	Analog ground connection
163	GMPX/PC4	B	Image bus DRAM multiplex signal/General-purpose port C
164	$\overline{GCAS}$/PC3	B	Image bus DRAM address strobe/General-purpose port C
165	$\overline{GRAS}$/PC2	B	
166	MA21/PI5	B	Image memory address bus/General-purpose port I
167	MA20/PI4	B	
168	MA19/PI3	B	
169	MA18/PI2	B	
170	MA17/PI1	B	
171	MA16/PI0	B	
172	V_{DD}	P	Supply pin
173	V_{SS}	P	Ground connection pin

Number	Name	I/O[1]	Function
174	MAD15	O	Image memory address bus/Data bus
175	MAD14	O	
176	MAD13	O	
177	MAD12	O	
178	MAD11	O	
179	MAD10	O	
180	MAD9	O	
181	MAD8	O	
182	$\overline{MRD}$	O	Image memory read signal
183	$\overline{MWR}$	O	Image memory write signal
184	$\overline{UDS}$	O	Upper byte data enable
185	$\overline{LDS}$	O	Lower byte data enable
186	MAST	O	Image memory address strobe
187	MRDY	O	Image memory access ready output
188	$\overline{MBACK}$/PC1	B	Image bus acknowledge signal/General-purpose port C
189	MBREQ/PC0	B	Image bus request signal/General-purpose port C
190	V_{DD}	P	Supply pin
191	V_{SS}	P	Ground connection pin
192	MAD7	B	Image memory address bus/Data bus
193	MAD6	B	
194	MAD5	B	
195	MAD4	B	
196	MAD3	B	
197	MAD2	B	
198	MAD1	B	
199	MAD0	B	
200	SPCLK/PI7	B	Speaker clock output/General-purpose port I
201	SBSY/PG4	B	Serial port status busy input/General-purpose port G
202	CBSY/PG3	B	Serial port command busy output/General-purpose port G
203	SCCLK/PG2	B	Serial port transmission clock/General-purpose port G
204	STATUS/PG1	B	Serial port status signal input/General-purpose port G
205	COMMAND/PG0	B	Serial port command signal output/General-purpose port G
206	TEST1	I	Test pins
207	TEST0	I	
208	V_{DD}	P	Supply pin

1. I = input, B = bidirectional, O = output, P = power

Pin Functions

CPU periphery (53 pins)

$\phi 2$	Output	System clock signal to the 65C816 (ICE). Left open for normal operation.
$\overline{RES}$	Output	Reset signal to the 65C816 (ICE). Left open for normal operation.
R/W	Input	Read/write signal from the 65C816 (ICE). Tied low for normal operation.
$\overline{IRQ}$	Output	Interrupt request signal to the 65C816 (ICE). Left open for normal operation.
$\overline{VP}$	Input/output	65C816 (ICE) interrupt vector address read indicator signal. When the internal CPU is operating, the internal CPU $\overline{VP}$ signal is output.
RDY	Output	Ready signal to the 65C816 (ICE). Open-drain output pin. Left open for normal operation.
BE	Output	Bus enable signal to the 65C816 (ICE). Left open for normal operation.

VPA	Input	Valid program address from the 65C816 (ICE) indicator signal. Tied low for normal operation.
VDA	Input	Valid data address from the 65C816 (ICE) indicator signal. Tied low for normal operation.
$\overline{NMI}$	Input	Non-maskable interrupt request signal
EMU	Input	Operation monitor indicator signal from the 65C816 (ICE). When EMU is high, the monitor control signal output can be stopped. Tied low for normal operation.
D7 to D0	Input/output	8-bit data bus
A20/PD4 to A23/PD7	Output	Upper address outputs when 16MB memory space is selected.
	Input/output	Bidirectional general-purpose ports in bit units. After reset, they are set to input ports.
A19 to A0	Output	Address bus
$\overline{RD}$	Output	Read data from external device read signal
$\overline{WR}$	Output	Write data to external device write signal
$\overline{ROMCS}$	Output	External program ROM access chip select signal
$\overline{RAMCS}$	Output	External RAM access chip select signal
$\overline{IOCS0}$	Output	External I/O access chip select signal
$\overline{IOCS1}$	Output	External I/O access chip select signal
$\overline{MCS}$	Output	External I/O access chip select signal
EXRDY/PA7	Input	External ready signal. When this pin is low, the CPU and DRAM controller (CPU bus) must wait.
	Input/output	Bidirectional general-purpose ports in bit units. After reset, they are set to input ports.
BREQ/PD0	Input	Bus hold request signal from the external master device
	Input/output	1-bit bidirectional general-purpose port. After reset, it is set to an input port.
$\overline{BACK}$/PD1	Output	Bus hold acknowledge signal to the external master device.
	Input/output	1-bit bidirectional general-purpose port. After reset, it is set to an input port.
Interrupt controller (3 pins)		
INT0	Input	External interrupt request signal (level 0)
INT10/PD2	Input	External interrupt request signal (level 10)
	Input/output	1-bit bidirectional general-purpose port. After reset, it is set to an input port.
INT19/PD3	Input	External interrupt request signal (level 19)
	Input/output	1-bit bidirectional general-purpose port. After reset, it is set to an input port.
DRAM controller (6 pins)		
$\overline{RAS}$/PC5	Output	CPU bus DRAM row-address strobe signal
	Input/output	1-bit bidirectional general-purpose port. After reset, it is set to an input port.
$\overline{CAS}$/PC6	Output	CPU bus DRAM column-address strobe signal
	Input/output	1-bit bidirectional general-purpose port. After reset, it is set to an input port.
MPX/PC7	Output	CPU bus DRAM address multiplex signal
	Input/output	1-bit bidirectional general-purpose port. After reset, it is set to an input port.
$\overline{GRAS}$/PC2	Output	Image bus DRAM row-address strobe signal
	Input/output	1-bit bidirectional general-purpose port. After reset, it is set to an input port.
$\overline{GCAS}$/PC3	Output	Image bus DRAM column-address strobe signal
	Input/output	1-bit bidirectional general-purpose port. After reset, it is set to an input port.
GMPX/PC4	Output	Image bus DRAM address multiplex signal
	Input/output	1-bit bidirectional general-purpose port. After reset, it is set to an input port.
DMA controller (4 pins)		
DREQ/PH4	Input	External I/O device DMA request signal
	Input/output	1-bit bidirectional general-purpose port. After reset, it is set to an input port.
$\overline{DACK}$/PH5	Output	External I/O device DMA acknowledge signal
	Input/output	1-bit bidirectional general-purpose port. After reset, it is set to an input port.
$\overline{IORD}$/PH6	Output	I/O read signal from DMA controller
	Input/output	1-bit bidirectional general-purpose port. After reset, it is set to an input port.

$\overline{\text{IOWR}}$/PH7	Output	I/O write signal from DMA controller
	Input/output	1-bit bidirectional general-purpose port. After reset, it is set to an input port.
RTC (2 pins)		
ROSC1	Input	RTC crystal oscillator connection pins for a 32.768kHz crystal oscillator element
ROSC2	Output	
Timer (3 pins)		
TCLK0/PH2	Input	Timer 0 external input clock
	Input/output	1-bit bidirectional general-purpose port. After reset, it is set to an input port.
TCLK1/PH3	Input	Timer 1 external input clock
	Input/output	1-bit bidirectional general-purpose port. After reset, it is set to an input port.
SPCLK/PI7	Output	Speaker clock output. A 244Hz to 62.5kHz clock is output, where the frequency is determined by frequency data stored in an internal register.
	Input/output	1-bit bidirectional general-purpose port. After reset, it is set to an input port.
I/O port (6 pins)		
PA5 to PA0	Input/output	Bidirectional general-purpose ports in bit units. After reset, they are set to input ports.
Serial port (11 pins)		
DTR/PB6	Output	8251 data terminal ready signal
	Input/output	1-bit bidirectional general-purpose port. After reset, it is set to an input port.
DSR/PB5	Input	8251 data set ready signal
	Input/output	1-bit bidirectional general-purpose port. After reset, it is set to an input port.
CTS/PB4	Input	8251 clear-to-send signal
	Input/output	1-bit bidirectional general-purpose port. After reset, it is set to an input port.
RTS/PB3	Output	8251 request-to-send signal
	Input/output	1-bit bidirectional general-purpose port. After reset, it is set to an input port.
TRCLK/PB2	Input	8251 clock input
	Input/output	1-bit bidirectional general-purpose port. After reset, it is set to an input port.
RXD/PB1	Input	8251 receive data input
	Input/output	1-bit bidirectional general-purpose port. After reset, it is set to an input port.
TXD/PB0	Output	8251 transmit data output
	Input/output	1-bit bidirectional general-purpose port. After reset, it is set to an input port.
COMMAND/PG0	Output	Serial command signal output
	Input/output	1-bit bidirectional general-purpose port. After reset, it is set to an input port.
STATUS/PG1	Input	Serial status signal input
	Input/output	1-bit bidirectional general-purpose port. After reset, it is set to an input port.
SCCLK/PG2	Input	Serial transfer clock input
	Input/output	1-bit bidirectional general-purpose port. After reset, it is set to an input port.
CBSY/PG3	Output	Command busy output
	Input/output	1-bit bidirectional general-purpose port. After reset, it is set to an input port.
SBSY/PG4	Input	Status busy input
	Input/output	1-bit bidirectional general-purpose port. After reset, it is set to an input port.
Thermal head control (11 pins)		
PCK/SCLK/PF0	Output	Thermal-head serial data transfer clock output
	Input/output	Serial I/O transfer data clock. Output for transmit, and input for receive.
	Input/output	1-bit bidirectional general-purpose port. After reset, it is set to an input port.
PDATA/TXD/PF1	Output	Thermal-head print serial data output
	Output	Serial I/O transmit data output
	Input/output	1-bit bidirectional general-purpose port. After reset, it is set to an input port.

EXCLK/PF2	Input	Transfer clock (PCK) external base clock
	Input/output	1-bit bidirectional general-purpose port. After reset, it is set to an input port.
$\overline{\text{LATCH}}$/RXD/PF3	Output	Thermal-head serial data latch signal
	Input	Serial I/O data receive signal
	Input/output	1-bit bidirectional general-purpose port. After reset, it is set to an input port.
$\overline{\text{STB0}}$/PF4	Output	Thermal-head print strobe signal
	Input/output	1-bit bidirectional general-purpose port. After reset, it is set to an input port.
$\overline{\text{STB1}}$/PF5	Output	Thermal-head print strobe signal
	Input/output	1-bit bidirectional general-purpose port. After reset, it is set to an input port.
$\overline{\text{STB2}}$/PF6	Output	Thermal-head print strobe signal
	Input/output	1-bit bidirectional general-purpose port. After reset, it is set to an input port.
$\overline{\text{STB3}}$/PF7	Output	Thermal-head print strobe signal
	Input/output	1-bit bidirectional general-purpose port. After reset, it is set to an input port.
HVON/PH0	Output	Head supply ON/OFF control signal
	Input/output	1-bit bidirectional general-purpose port. After reset, it is set to an input port.
PROTECT/PH1	Input	Head protection abnormality detector signal input. When PROTECT goes low, HVON and ??? outputs become inactive.
	Input/output	1-bit bidirectional general-purpose port. After reset, it is set to an input port.
TEMP	Input	Thermal-head temperature detector pin. Connected to the thermal-head thermistor output
Motor control (8 pins)		
TM0/PE0 to TM3/PE3	Output	Transmit motor phase signal
	Input/output	Bidirectional general-purpose ports in bit units. After reset, they are set to input ports.
RM0/PE4 to RM3/PE7	Output	Receive motor phase signal
	Input/output	Bidirectional general-purpose ports in bit units. After reset, they are set to input ports.
Image processing (35 pins)		
AIN	Input	Analog image signal input to the internal A/D converter. The minimum input potential should be set as close as possible to AV_{SS}.
ATAP	Input	Internal A/D converter reference voltage pin. This potential changes varies with the internal AGC. A capacitor should be connected to this pin for stability.
ASAMP/PB7	Output	Internal A/D converter sampling point monitor signal
	Input/output	1-bit bidirectional general-purpose port. After reset, it is set to an input port.
SH	Output	Sensor line signal output
RS	Output	CCD reset signal output
ACLK1, ACLK2	Output	Sensor transfer signal outputs
LEDON/PA6	Output	LED ON control signal
	Input/output	1-bit bidirectional general-purpose port. After reset, it is set to an input port.
ICLK/PI6	Input	Image processor external clock input
	Input/output	1-bit bidirectional general-purpose port. After reset, it is set to an input port.
IA14 to IA0	Output	Image processor memory address outputs
ID7 to ID0	Input/output	Image processor memory data bus
$\overline{\text{ICS}}$	Output	Image processor memory chip select
$\overline{\text{IRD}}$	Output	Image processor memory read signal
$\overline{\text{IWR}}$	Output	Image processor memory write signal
Image memory (30 pins)		
MA21/PI5 to MA16/PI0	Output	Image processor memory upper-order address outputs
	Input/output	Bidirectional general-purpose ports in bit units. After reset, they are set to input ports.
MAD15 to MAD0	Input/output	Image memory lower-order address outputs/Data bus
$\overline{\text{MRD}}$	Output	Image memory read signal

$\overline{MWR}$	Output	Image memory write signal
$\overline{UDS}$	Output	Upper-byte data enable
$\overline{LDS}$	Output	Lower-byte data enable
MAST	Output	Image memory address strobe
MRDY	Output	Image memory access ready output
MBREQ/PC0	Input	Image bus request input
	Input/output	1-bit bidirectional general-purpose port. After reset, it is set to an input port.
$\overline{MBACK}$/PC1	Output	Image bus acknowledge ouput
	Input/output	1-bit bidirectional general-purpose port. After reset, it is set to an input port.
System (35 pins)		
XTAL1	Input	Crystal oscillator connection pin for 32MHz crystal oscillator element
XTAL2	Output	Crystal oscillator connection pin for 32MHz crystal oscillator element
XTALOUT	Output	Clock output pin. This clock output has the same frequency as the crystal oscillator.
CLKIN	Input	System clock input. Connected to XTALOUT if using a crystal oscillator.
$\overline{RESET}$	Input	System reset
$\overline{BACKUP}$	Input	Power-down mode select for backup
TEST0, TEST1	Input	Test pins. Tied low for normal operation.
V_{DD}	Power supply	Digital supply pins
V_{SS}	Power supply	Digital ground connection pins
AV_{DD}	Power supply	Analog supply pins
AV_{SS}	Power supply	Analog ground connection pins
V_{BAT}	Power supply	Backup supply pin

Function Outline

CPU Peripheral Circuits

- Generates 80-series CPU compatible CS/RD/WR signals
- Chip select signal outputs for program ROM, SRAM and I/O device connections
- ROM, SRAM and DRAM sizes addressed in 64KB units
- Inserts wait cycles when accessing ROM, SRAM and I/O
- Internal/external DMA controller bus arbitration function

Image Processor

- Number of processed picture elements (pels)
  - 2048pels/line (uses 64K memory, with black and white correction)
  - 4096pels/line (uses 64K memory, with white correction only)
  - 8192pels/line (uses 256K memory, with white correction only)
- 800ns/pel max. processing rate
- 1 external, medium-speed memory
  - 100ns access time at 800ns/pel rate, 60ns access time at 500ns/pel rate
- AGC, 8-bit A/D converter built-in (with delay adjust function)
- Thermal printer head temperature monitor function
- Sensor drive circuit (CCD, various CIS types)
- Digital clamp (dot clamp, even-odd clamp)
- Distortion correction (white, black, all pels)
- γ correction (user-definable curve)
- Image content separation (character, pictures, screens)
- Simple two-value processing (fixed threshold value, density-adjusted threshold value)
- Half-tone processing
  - Systematic dither method (64 gradations), dither threshold value adjustable
  - Error diffusion method (64 gradations)
- Image reduction (thinning out, black fine line hold, white fine line hold)

Codec

- MH/MR/MMR format encoding
- 8/16-bit image bus, 4MB image memory space
- 2-system manuscript alternate processing
- 4Kline (max) block processing
- Line skip mode
- Data transfer between CPU bus and image bus

Picture Element Density Conversion

- Simple thinning, simple OR, 3-term logic
- 3-line window processing
- 1/2 to 2-times conversion in 1/128 steps

TPH Interface

- 4MHz, 2MHz, 1MHz and 500kHz transmission clock frequency
- Switchable rising-edge/falling-edge clock phase
- Strobe division: 1, 2, and 4
- 32μs to 8.16ms strobe width
- Switchable strobe and latch pulse polarity
- Strobe and latch pulse can be generated manually and treated as a general-purpose output port
- Head supply ON/OFF control
- Head protection input pin (PROTECT) setup
  - Mode 1: HVON and STB0 to STB3 are set to inactive state after a continuous LOW-level input of approximately 64ms
  - Mode 2: HVON and STB0 to STB3 are set to inactive state immediately after a LOW-level signal

Motor Interface

- Transmit/receive 2-channel stepping-motor interface
- 4-phase motor (excitation method: 2 phase/1-2 phase/1 phase)
- Forward/reverse selectable control register
- Phase change trigger select
  - Transmit motor
    Register bit ON/OFF
    Dedicated timer trigger
  - Receive motor
    Register bit ON/OFF
    Dedicated timer trigger
- Dedicated timer controlled, 64-step trapezoidal control processing

DMA Controller (CPU Bus)

- 2-channel transmission, memory ↔ I/O
  - Channel 0: External I/O ↔ memory
  - Channel 1: Codec ↔ memory
- 16MB addresses/64K transfer count
- 2.6MB/s max. transfer rate
- Individual DMA request permit/prohibit
- Auto-initialization function
- Fixed precedence order: channel 0 > channel 1

DMA Controller (Image Bus)

- 4-channel transmission, memory ↔ I/O
  - Channel 0: Image processor → memory
  - Channel 1: Memory → TPH interface
  - Channel 2: Memory → picture element density converter
  - Channel 3: Picture element density converter → memory
- 4MB addressable
- 8/16-bit data bus
- 6.4MB/s max. transfer rate
- Line width × line number access (1KB × 4Klines)
- Channel 1 configured for a latchless head
- Individual DMA request permit/prohibit

Timer

- 6 independent 16-bit counters built-in
- 8-bit prescaler built-in for each counter
- 244Hz to 15.6kHz speaker clock generator
- Timer 0 and 1 have selectable external clock inputs

DRAM Controller

- 256K/1M/4Mb DRAM support, up to 120ns access time
- CAS-before-RAS refresh
- Employs early-write mode
- Internal refresh counter: 4ms refresh time for 256K, 8ms for 1M, 16ms for 4M
- Register setting capability for 9 dummy refresh cycle execution
- Auto-refresh mode during backup

Interrupt Controller

- 22-level interrupt control (internal: 19 levels, external: 3 levels)
- Individual level mask processing
- Interrupt vector address output

RTC

- Time function with alarm
- 100-year calendar
- 12-hour/24-hour time display, summer time set capability
- Leap year, short/long month auto-correction
- Selectable binary or BCD data for time, calendar and alarm
- 3 types of interrupts
  - Alarm interrupt
  - Periodic interrupt
  - Update ended interrupt

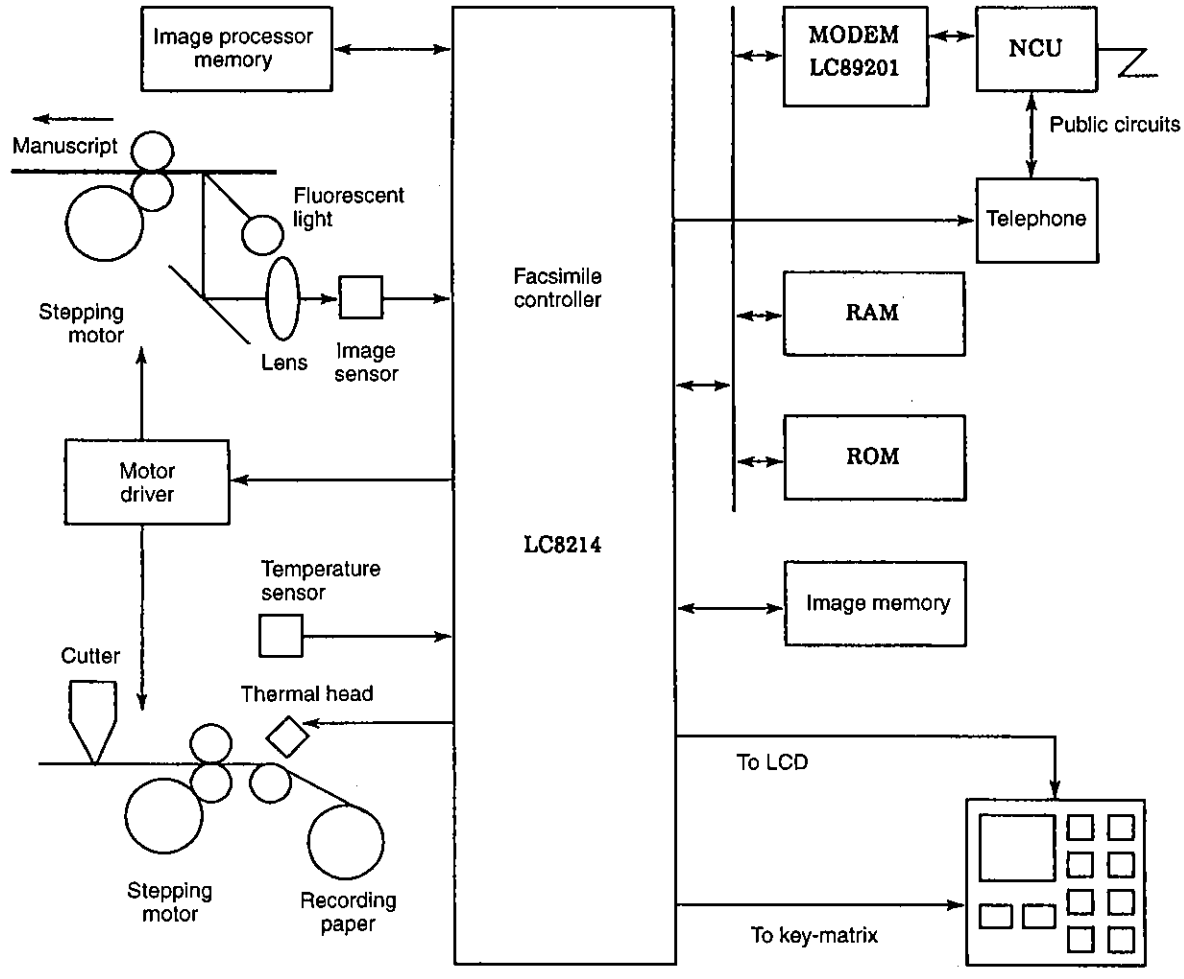
Serial Port

- 3-channel serial port
- 1 channel is 8251 asynchronous mode compatible

General-Purpose Ports

- 6 to 69 input/output ports
- All ports are bidirectional
- Extendable up to 69 ports by switchover to dedicated pins

Sample Application Circuit



Specifications

Absolute Maximum Ratings at V_{SS} = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	Ta = 25°C	–0.3 to +7.0	V
Input/output voltage	V_I, V_O	Ta = 25°C	–0.3 to V_{DD} + 0.3	V
Power dissipation	Pd max	Ta ≤ 70°C	600	mW
Operating temperature	Topr		–30 to +70	°C
Storage temperature	Tstg		–55 to +125	°C
Soldering temperature	Tsol	Manual soldering (3s)	350	°C
		Reflow soldering (10s)	235	°C

Allowable Operating Ranges at Ta = –30 to +70°C, V_{SS} = 0V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}		4.5	–	5.5	V
Input voltage	V_{IN}		0	–	V_{DD}	V

DC Characteristics at Ta = −30 to +70°C, V_{DD} = 4.5 to 5.5V

Parameter	Symbol	Conditions	min	typ	max	Unit
Input HIGH-level voltage	V_{IH1}		2.2	–	–	V
Input LOW-level voltage	V_{iL1}		–	–	0.8	V
Input leakage current	I_L		−25	–	+25	µA
Output HIGH-level voltage	V_{OH}	I_{OH} = −3mA	2.4	–	–	V
Output LOW-level voltage	V_{OL}	I_{OL} = 3mA	–	–	0.4	V
Output leakage current	I_{OZ}	High-impedance output	−100	–	+100	µA
Oscillator frequency	f_{CLK1}	CLKIN	–	–	32	MHz
	f_{CLK2}	ICLK, TCLK0, TCLK1	–	–	32	MHz
	f_{CLK3}	ROSC1, ROSC2	–	32.768	–	kHz
Current dissipation	I_{DD1}	Operating normally	–	–	100	mA
	I_{DD2}	Power-down, V_{DD} = 2V, $\overline{BACKUP}$ = low	–	3	5	µA