Ordering number : EN※4940B

CMOS LSI

No. ※ 4940B

LC89590

CD-R LSI

Preliminary

Functions

- CD-ROM data decoding (including error checking and correction) and encoding functions, subcode reading and writing functions, CD encoding function, ATIP decoding function

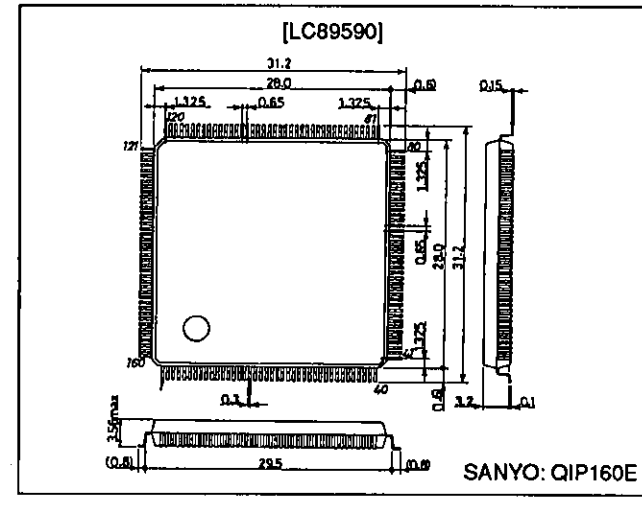
Features

- Double-speed operation at a 17.2872 MHz clock frequency using 70-ns DRAM
- CD-ROM encoding and decoding functions
- ATIP decoding and CRC checking functions
- Subcode data can be written to buffer RAM by connecting to the CD-DSP SUB-CODE pin, thus allowing the sub-CPU to read the subcode values.
- The LC89590 can interleave the subcode data (R to W) and write it along with the CD-ROM data. (CD-DA data)
- Function for adding CRC bits to the subcode Q data
- EFM data modulation function
- The sub-CPU can access the buffer RAM through the LC89590.
- Buffer RAM internal data transfer function
- Four-byte FIFO for sub-CPU to host computer transfers
- Twelve-byte FIFO for host computer to sub-CPU transfers

Package Dimensions

unit: mm

3153A-QFP160E



SANYO Electric Co., Ltd. Semiconductor Business Headquarters

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

Specifications

Absolute Maximum Ratings at V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	Ta = 25°C	–0.3 to +7.0	V
Input and output voltages	V_I V_O	Ta = 25°C	–0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max	Ta ≤ 70°C	350	mW
Operating temperature	Topr		–30 to +70	°C
Storage temperature	Tstg		–55 to +125	°C
Soldering tolerance (pins only)		10 seconds	260	°C

Allowable Operating Ranges at Ta = –30 to +70°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
Input voltage range	V_{IN}		0		V_{DD}	V

DC Characteristics: I/O Levels at Ta = –30 to +70°C, V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Input high-level voltage	$V_{IH}1$	(3), (5)	2.2			V
Input low-level voltage	$V_{IL}1$	(3), (5)			0.8	V
Input high-level voltage	$V_{IH}2$	(2), (4)	2.5			V
Input low-level voltage	$V_{IL}2$	(2), (4)			0.6	V
Input high-level voltage	$V_{IH}3$	(6), (7)	2.2			V
Input low-level voltage	$V_{IL}3$	(6), (7)			0.8	V
Input high-level voltage	$V_{IH}4$	(1)	0.7 V_{DD}			V
Input low-level voltage	$V_{IL}4$	(1)			0.3 V_{DD}	V
Output high-level voltage	$V_{OH}1$	I_{OH} = –2 mA: (4), (5), (6), (9), (10), (11)	V_{DD} – 2.1			V
Output low-level voltage	$V_{OL}1$	I_{OL} = 2 mA: (4), (5), (6), (9), (10), (11)			0.4	V
Output low-level voltage	$V_{OL}2$	I_{OL} = 2 mA: (7)			0.4	V
Output high-level voltage	$V_{OH}3$	I_{OH} = –4 mA: (8)	V_{DD} – 1.5			V
Output low-level voltage	$V_{OL}3$	I_{OL} = 2 mA: (8)			0.4	V
Input leakage current	I_{IL}	V_I = V_{SS}, V_{DD}: (1), (2), (3), (4), (5)	–10		10	µA
Output leakage current	I_{OZ}	When the output is high impedance: (4), (5), (7), (9)	–10		10	µA
Pull-up resistance	R_{UP}	(6), (7)	40	80	160	kΩ

Note: The numbers in parentheses in the table refer to the following applicable output pin sets:

Input

(1) .....XTALCK

(2) .....BICLKIN, BITDATAI, ROUGH, SBSO, SCOR, WFCK, $\overline{CMD}$, $\overline{CS}$, $\overline{ENABLE}$, $\overline{HRD}$, $\overline{HWR}$, $\overline{RD}$, $\overline{RESET}$, $\overline{WR}$

(3) .....BCK, C2PO, CPUCNT, HDTATT, LOCKIN, LRCK, RS, SDATA, SELDRQ, SUA0 to SUA6, $\overline{EXTSYNC}$, $\overline{HDREN}$, TEST, TEST5, TEST6

In/Out

(4) .....PLLOUTIN

(5) .....ATIPSYNC, SVSWITCH

(6) .....D0 to D7, HD0 to HD7, IO0 to IO7, MD0 to MD7

Output

(7) .....$\overline{INT}$

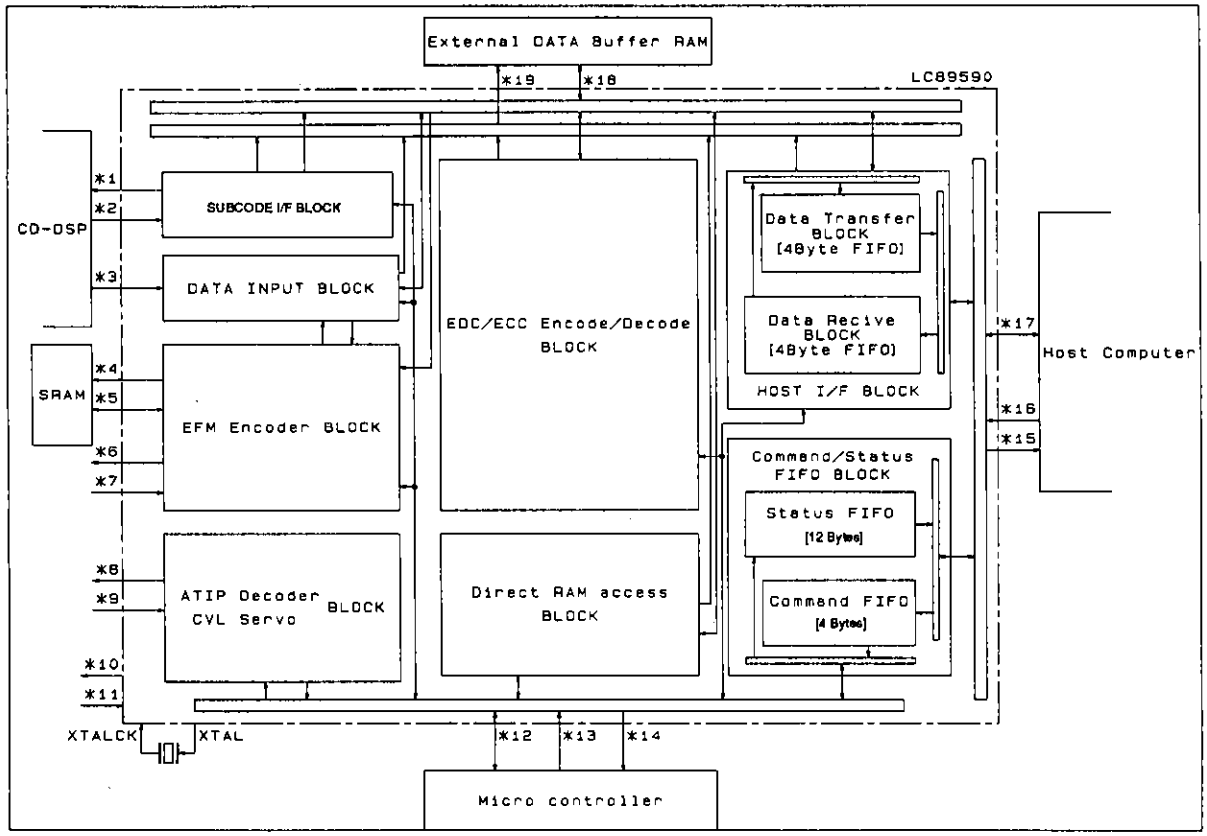
(8) .....XTAL

(9) .....CLV + (MDP), CLV – (MDS)

(10) ....EXCK, $\overline{DREN}$, $\overline{DTEN}$, $\overline{EOP}$, $\overline{RCS}$, $\overline{ROE}$, $\overline{RWE}$, $\overline{STEN}$, $\overline{WAIT}$

(11) ....$\overline{RAS}$, $\overline{CAS}$, DATACKO, DATALRCO, DATAST, DATAWDCO, DATSPCA, EFM, EFMG, EFMS, FRCK, LOCK, OSDATA, PSUBSYNC, SUBSYNC, TTT, $\overline{ERROR}$, $\overline{EXTACK}$, $\overline{SWAIT}$, LINKPOS0, MAD0 to MAD11, MRD, MWR, RA0 to RA10

Block Diagram



A04237

Note: 1. EXCK
2. WFCK, SBSO, SCOR
3. BCK, SDATA, LRCK, C2PO
4. MAD0 to MAD11, MRD, MWR
5. MD0 to MD7
6. SUBSYNC, PSUBSYNC, $\overline{\text{FRCK}}$, DATAST, DATSPCA, EFM, EFMG, EFMS, LINKPOS, TTT, $\overline{\text{EXTACK}}$, OSDATA
7. $\overline{\text{EXTSYNC}}$, ATIPSYNC
8. $\overline{\text{ERROR}}$, ATIPSYNC, LOCK, CLV + (MDP), CLV – (MDS)
9. PLLOUTIN, ROUGH, SVSWITCH, LOCKIN, BICLKIN, BIDATAIN
10. TEST1 to TEST4 (Not connect)
11. TEST5, TEST6 (GND), $\overline{\text{RESET}}$
12. D0 to D7
13. $\overline{\text{CS}}$, RS, $\overline{\text{RD}}$, $\overline{\text{WR}}$, CPUCNT, SUA0 to SUA6, $\overline{\text{SELDRQ}}$
14. $\overline{\text{SWAIT}}$, $\overline{\text{INT}}$
15. $\overline{\text{DREN}}$, $\overline{\text{DTEN}}$, $\overline{\text{STEN}}$, $\overline{\text{EOP}}$, $\overline{\text{WAIT/DRQ}}$
16. $\overline{\text{ENABLE}}$, $\overline{\text{CMD}}$, $\overline{\text{HRD}}$, $\overline{\text{HWR}}$, DTATT, $\overline{\text{HDREN}}$
17. HD0 to HD7
18. IO0 to IO7
19. RA0 to RA10, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{ROE}}$, $\overline{\text{RWE}}$, $\overline{\text{RCS}}$

Pin Functions

Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, NC: No connection pin

Pin No.	Symbol	I/O	Description
1	V_{SS}	P	
2	TEST1	NC	Test inputs Leave pins 2 to 5 open. Pins 6 and 7 must be tied low.
3	TEST2	NC	
4	TEST3	NC	
5	TEST4	NC	
6	TEST5	I	
7	TEST6	I	
8	$\overline{ROE}$	O	Read, write, and select lines for the ROM encoder and decoder buffer RAM.
9	$\overline{RWE}$	O	
10	$\overline{RCS}$	O	
11	V_{DD}	P	
12	IO0	B	Data signal lines for the ROM encoder and decoder buffer RAM. Pull-up resistors are built in.
13	IO1	B	
14	IO2	B	
15	IO3	B	
16	IO4	B	
17	IO5	B	
18	IO6	B	
19	IO7	B	
20	V_{DD}	P	
21	V_{SS}	P	
22	$\overline{RAS}$	O	DRAM $\overline{RAS}$ signal output
23	V_{SS}	P	
24	$\overline{CAS}$	O	DRAM $\overline{CAS}$ signal output
25	V_{DD}	P	
26	RA0	O	Address signal outputs to the ROM encoder and decoder buffer RAM.
27	RA1	O	
28	RA2	O	
29	RA3	O	
30	RA4	O	
31	RA5	O	
32	TEST	I	Test input. Must be tied low.
33	RA6	O	Address signal outputs to the ROM encoder and decoder buffer RAM.
34	RA7	O	
35	RA8	O	
36	RA9	O	
37	RA10	O	
38	$\overline{RESET}$	I	Chip reset input
39	SUA0	I	Command register selection address
40	V_{DD}	P	
41	V_{SS}	P	
42	SUA1	I	Command register selection address
43	SUA2	I	
44	SUA3	I	
45	SUA4	I	
46	SUA5	I	
47	SUA6	I	
48	V_{SS}	P	

Continued on next page.

Continued from preceding page.

Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, NC: No connection pin

Pin No.	Symbol	I/O	Description
49	D0	B	Microprocessor data signal lines Pull-up resistors are built in.
50	D1	B	
51	D2	B	
52	D3	B	
53	D4	B	
54	D5	B	
55	D6	B	
56	D7	B	
57	$\overline{\text{SELDRQ}}$	I	Mode selection for transfers to the host (WAIT control, DRQ control)
58	$\overline{\text{RD}}$	I	Microprocessor data read signal input
59	$\overline{\text{WR}}$	I	Microprocessor data write signal input
60	V_{DD}	P	
61	V_{SS}	P	
62	$\overline{\text{CS}}$	I	Chip select signal input from the microprocessor
63	RS	I	Register select signal
64	$\overline{\text{SWAIT}}$	O	Sub-CPU wait signal
65	$\overline{\text{INT}}$	O	Interrupt request signal output to the microprocessor
66	$\overline{\text{ENABLE}}$	I	Chip select signal input from the host
67	$\overline{\text{CMD}}$	I	Command/data selection signal input from the host
68	$\overline{\text{HWR}}$	I	Host data write signal input
69	$\overline{\text{HRD}}$	I	Host data read signal input
70	CPUCNT	I	Indirect/direct addressing selection signal input
71	HD0	B	Host data signals Pull-up resistors are built in.
72	HD1	B	
73	HD2	B	
74	HD3	B	
75	HD4	B	
76	HD5	B	
77	HD6	B	
78	HD7	B	
79	$\overline{\text{WAIT}}$	O	Wait signal output to the host. Can be switched to output the DRQ signal.
80	V_{DD}	P	
81	V_{SS}	P	
82	$\overline{\text{DTEN}}$	O	Data enable signal output
83	$\overline{\text{STEN}}$	O	Status enable signal output
84	$\overline{\text{EOP}}$	O	End of process signal output. Used during DMA data transfers.
85	$\overline{\text{DREN}}$	O	Data receive enable signal output
86	DTATT	I	ROM data/subcode data switching input
87	$\overline{\text{HDREN}}$	I	Transfer enable signal input from host
88	EXCK	O	Subcode I/O
89	WFCK	I	
90	SBSO	I	
91	SCOR	I	
92	V_{DD}	P	
93	$\overline{\text{ERROR}}$	O	ATIP parity error detection output
94	LOCK	O	CLV servo lock monitor
95	LOCKIN	I	CD decoder lock signal input
96	BICLKIN	I	Biphase data transfer clock input
97	BIDATAI	I	Biphase data input
98	CLV + (MDP)	O	CLV servo signal output
99	CLV – (MDS)	O	CLV servo signal output
100	V_{DD}	P	
101	V_{SS}	P	
102	PLLOUTIN	B	Wobble signal carrier wave clock input

Continued on next page.

Continued from preceding page.

Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, NC: No connection pin

Pin No.	Symbol	I/O	Description
103	ROUGH	I	Wobble signal input for rough CLV servo
104	SVSWITCH	B	CLV servo reference clock selection input
105	SDATA	I	Serial data input
106	BCK	I	Serial data input clock
107	LRCK	I	44.1 kHz strobe signal input
108	C2PO	I	C2 pointer input
109	V_{SS}	P	
110	XTALCK	I	Crystal oscillator circuit input (17.2872 MHz)
111	XTAL	O	Crystal oscillator circuit output
112	V_{SS}	P	
113	V_{SS}	P	
114	MWR	O	EFM encoder SRAM write signal
115	MRD	O	EFM encoder SRAM read signal
116	MAD0	O	EFM encoder SRAM address signal outputs
117	MAD1	O	
118	MAD2	O	
119	MAD3	O	
120	V_{DD}	P	
121	V_{SS}	P	
122	MAD4	O	EFM encoder SRAM address signal outputs
123	MAD5	O	
124	MAD6	O	
125	MAD7	O	
126	MAD8	O	
127	V_{DD}	P	
128	MAD9	O	EFM encoder SRAM address signal outputs
129	MAD10	O	
130	MAD11	O	
131	MD0	B	EFM encoder SRAM data signals
132	MD1	B	
133	MD2	B	
134	V_{SS}	P	
135	MD3	B	EFM encoder SRAM data signals
136	MD4	B	
137	MD5	B	
138	MD6	B	
139	MD7	B	
140	V_{DD}	P	
141	V_{SS}	P	
142	$\overline{\text{EXTSYNC}}$	I	ATIP synchronization enable signal input
143	$\overline{\text{EXTACK}}$	O	ATIP synchronization acknowledge signal output
144	ATIPSYNC	B	ATIP synchronization signal I/O
145	PSUBSYNC	O	Pseudo-subcode synchronization output
146	EFMG	O	EFM output gate signal
147	LINKPOS	O	Link position signal output
148	EFMS	O	Outputs the logical AND of the EFM and EFMG signals.
149	EFM	O	EFM signal output
150	TTT	O	3T detection signal output

Continued on next page.

Continued from preceding page.

Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, NC: No connection pin

Pin No.	Symbol	I/O	Description
151	V_{SS}	P	
152	DATACKO	O	4.3218 MHz oscillator output
153	DATALRCO	O	44.1 kHz oscillator output
154	DATAWDCO	O	88.2 kHz oscillator output
155	OSDATA	O	ROM encoded data serial output
156	$\overline{FRCK}$	O	EFM frame synchronizing signal output
157	DATAST	O	Data start monitor signal output
158	DATSPCA	O	Data/PCA monitor signal output
159	SUBSYNC	O	Subcode synchronizing signal output
160	V_{DD}	P	