Ordering number : EN5114

No. 5114

SANYO

LC89973M

PAL CCD Delay Line

Overview

The LC89973M is a CCD delay line for PAL television systems. It incorporates a comb filter for chrominance signal and a 1H delay line for luminance signal.

Structure

- NMOS + CCD

Structure

- NMOS + CCD

Functions

- Two CCD shift registers (for chrominance and luminance signals)
- CCD drive circuits
- CCD stage count switching circuit
- CCD signal adder
- Auto-bias circuit
- Sync tip clamping circuit (luminance signal)
- Center-bias circuit (chrominance signal)
- Sample-and-hold circuit
- PLL 3 × frequency multiplier
- fsc clock output circuit
- RD voltage generator

Features

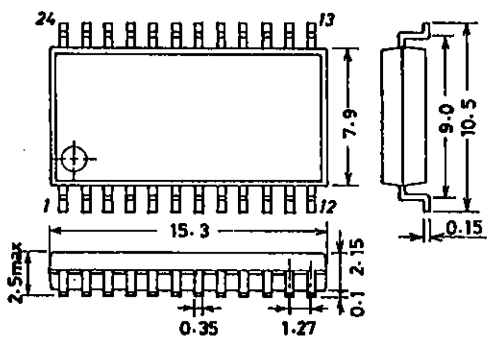
- 5 V single-voltage power supply
- Built-in PLL 3 × frequency multiplier circuit allows 3 fsc operation from an fsc (4.43 MHz) input.
- Control pin switchable to handle PAL/GBI and 4.43 MHz NTSC systems.
- Built-in chrominance signal crosstalk exclusion comb filter features high precision comb characteristics in an adjustment-free circuit.
- Built-in peripheral circuits allow applications to be constructed with a minimum number of external components.
- Positive-phase signal input/positive-phase signal output (luminance signal)

Package Dimensions

unit: mm

3045B-MFP24

[LC89973M]



SANYO: MFP24

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		–0.3 to +6.0	V
Allowable power dissipation	Pd max		600	mW
Operating temperature	Topr		–10 to +70	°C
Storage temperature	Tstg		–55 to +150	°C

Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}		4.75	5.00	5.25	V
Clock input amplitude	V_{CLK}		300	500	1000	mVp-p
Clock frequency	F_{CLK}	Sine wave	—	4.43361875	—	MHz
Clock signal input amplitude	$V_{IN\text{-}C}$		—	350	500	mVp-p
Luminance signal input amplitude	$V_{IN\text{-}Y}$		—	400	572	mVp-p

Electrical Characteristics at V_{DD} = 5.0 V, Ta = 25°C, F_{CLK} = 4.43361875 MHz, V_{CLK} = 500 mVp-p

Parameter	Symbol	Switch states			Conditions	min	typ	max	Unit
		SW1	SW2	SW3					
Supply current	$I_{DD\text{-}1}$	a	a	b	1	40	50	60	mA
	$I_{DD\text{-}2}$	b	a	b					
Chrominance System Characteristics (with no Y-IN input)									
Pin voltage (input)	$V_{INC\text{-}1}$	a	a	b	2	2.0	2.4	2.8	V
	$V_{INC\text{-}2}$	b	a	b					
Pin voltage (output)	$V_{OUYC\text{-}1}$	a	a	b		1.2	1.6	2.0	V
	$V_{OUTC\text{-}2}$	b	a	b					
Voltage gain	$G_{VC\text{-}1}$	a	a	b	3	–2	0	+2	dB
	$G_{VC\text{-}2}$	b	a	b					
Comb depth	$C_{D\text{-}1}$	a	a	b	4	—	–40	–35	dB
	$C_{D\text{-}2}$	b	a	b					
Linearity	$L_{NC\text{-}1}$	a	a	b	5	–0.3	0.0	+0.3	dB
	$L_{NC\text{-}2}$	b	a	b					
Clock leakage (3 fsc)	$L_{CK3C\text{-}1}$	a	a	b	6	—	10	50	mVrms
	$L_{CK3C\text{-}2}$	b	a	b					
Clock leakage (fsc)	$L_{CK1C\text{-}1}$	a	a	b		—	0.8	1.5	mVrms
	$L_{CK1C\text{-}2}$	b	a	b					
Noise	$N_{C\text{-}1}$	a	a	b	7	—	0.5	2.0	mVrms
	$N_{C\text{-}2}$	b	a	b					
Output impedance	$Z_{OC\text{-}1}$	a	a	a, b	8	200	350	500	Ω
	$Z_{OC\text{-}2}$	b	a	a, b					
0 H delay time	$T_{DC\text{-}1}$	a	a	b	9	—	245	—	ns
	$T_{DC\text{-}2}$	b	a	b					

Continued on next page.

Continued from preceding page.

Parameter	Symbol	Switch states			Conditions	min	typ	max	Unit
		SW1	SW2	SW3					
Luminance System Characteristics (with no C-IN1 or C-IN2 input)									
Pin voltage (input)	V_{INY-1}	a	a	b	10	1.7	2.1	2.5	V
	V_{INY-2}	b	a	b					
Pin voltage (output)	V_{OUTY-1}	a	a	b		0.8	1.2	1.6	V
	V_{OUTY-2}	b	a	b					
Voltage gain	G_{VY-1}	a	a	b	11	–2	0	+2	dB
	G_{VY-2}	b	a	b					
Frequency responce	G_{FY-1}	a	b	b	12	–2	0	+2	dB
	G_{FY-2}	b	b	b					
Differential gain	D_{GY-1}	a	a	b	13	0	5	7	%
	D_{GY-2}	b	a	b					
Differential phase	D_{PY-1}	a	a	b		0	5	7	deg
	D_{PY-2}	b	a	b					
Linearity	L_{SY-1}	a	a	b	14	37	40	43	%
	L_{SY-2}	b	a	b					
Clock leakage (3 fsc)	L_{CK3Y-1}	a	a	b	15	—	10	50	mVrms
	L_{CK3Y-2}	b	a	b					
Clock leakage (fsc)	L_{CK1Y-1}	a	a	b		—	0.8	1.5	mVrms
	L_{CK1Y-2}	b	a	b					
Noise	N_{Y-1}	a	a	b	16	—	0.5	2.0	mVrms
	N_{Y-2}	b	a	b					
Output impedance	Z_{OY-1}	a	a	c, b	17	250	400	550	Ω
	Z_{OY-2}	b	a	c, b					
Delay time	T_{DY-1}	a	a	b	18	—	63.84	—	µs
	T_{DY-2}	b	a	b		—		—	

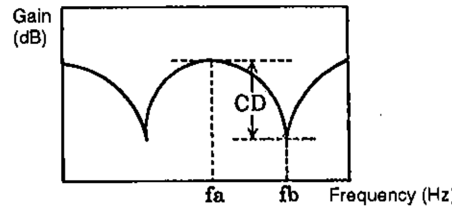
Test Conditions

1. Supply current with no signal input.
2. C-OUT voltage (center bias voltage) with no signal input.
3. Measure the C-OUT output with 350 mVp-p sine wave signals input to C-IN1 and C-IN2.

$$GVC = 20 \log \frac{\text{C-OUT output [mVp-p]}}{350\ \text{[mVp-p]}}\ \text{[dB]}$$

Test frequencies
GVC-1 4.429662 MHz (PAL/GBI)
GVC-2 4.425749 MHz (4.43 NTSC)

4. Measure the comb depth from the C-OUT output with a 350 mVp-p sine wave signal of frequency fa input to C-IN1 and C-IN2 and with a frequency of fb input.



$$CD = 20 \log \frac{\text{C-OUT output with fb input [mVp-p]}}{\text{C-OUT output with fa input [mVp-p]}} \text{ [dB]}$$

Test frequencies

	fa	fb
CD-1	4.429662 MHz	4.425756 MHz (PAL/GBI)
CD-2	4.425749 MHz	4.417930 MHz (4.43 NTSC)

5. Measure the C-OUT output with a 200 mVp-p sine wave signal input to C-IN1 and C-IN2 and with 500 mVp-p sine wave signal input and calculate the difference in the gains.

$$LNC = 20 \log \left(\frac{\text{Output for a 500 mVp-p input [mVp-p]}}{\text{500 [mVp-p]}} \Big/ \frac{\text{Output for a 200 mVp-p input [mVp-p]}}{\text{200 [mVp-p]}} \right) \text{ [dB]}$$

Test frequencies
LNC-1 4.429662 MHz (PAL/GBI)
LNC-2 4.425749 MHz (4.43 NTSC)

6. Measure the 3 fsc (13.3 MHz) and fsc (4.43 MHz) components in the C-OUT output with no input.

7. Measure the noise in the C-OUT output with no input.
Measure the noise with a noise meter set up with a 200 kHz high-pass filter and a 5 MHz low-pass filter.

8. Let V1 be the C-OUT output with a 350 mVp-p sine wave input to C-IN1 and C-IN2 and SW3 set to a, and let V2 be the C-OUT output with SW3 set to b.

$$ZOC = \frac{\text{V2 [mVp-p]} - \text{V1 [mVp-p]}}{\text{V1 [mVp-p]}} \times 500 \text{ [}\Omega\text{]}$$

Test frequencies
ZOC-1 4.429662 MHz (PAL/GBI)
ZOC-2 4.425749 MHz (4.43 NTSC)

9. The C-OUT output delay time with respect to inputs to C-IN1. (the CCD 2.5 bit delay)

10. Y-OUT voltage (clamp voltage) with no signal input.

11. Measure the Y-OUT output with a 200 kHz 400 mVp-p sine wave input to Y-IN.

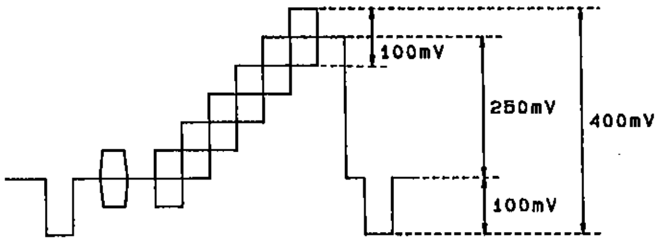
$$GVY = 20 \log \frac{\text{Y-OUT output [mVp-p]}}{\text{400 [mVp-p]}} \text{ [dB]}$$

12. Measure the Y-OUT output with a 200 kHz 200 mVp-p sine wave input to Y-IN and with a 3.3 MHz 200 mVp-p sine wave input.

$$GFY = 20 \log \frac{\text{Y-OUT output with a 3.3 MHz input [mVp-p]}}{\text{Y-OUT output with a 200 kHz input [mVp-p]}} \text{ [dB]}$$

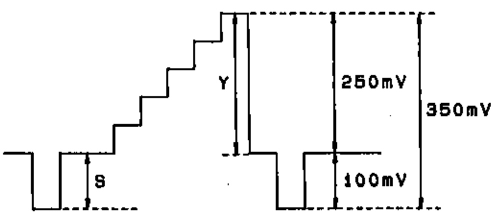
Note that V_{bias} should be adjusted so that the circuit is biased to the clamp level plus 250 mV.

13. Input a five-level step waveform (see the figure below) to Y-IN and measure the differential gain and differential phase in the Y-OUT output with a vector scope.



A03853

14. Input a five-level step waveform (see the figure below) to Y-IN and measure the luminance level (Y) and the sync level (S) in the Y-OUT output.



$$LS = \frac{S\ [mV]}{Y\ [mV]} \times 100\ [\%]$$

A03854

15. Measure the 3 fsc (13.3 MHz) and fsc (4.43 MHz) components in the Y-OUT output with no input.

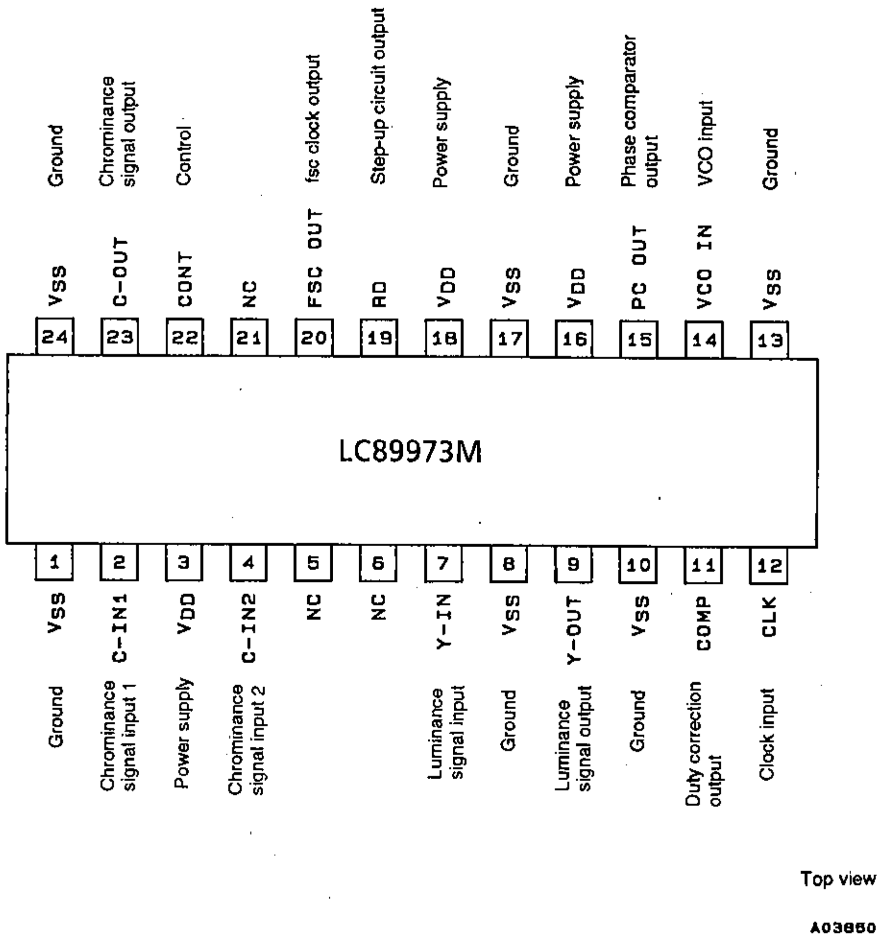
16. Measure the noise in the Y-OUT output with no input.
Measure the noise with a noise meter set up with a 200 kHz high-pass filter, a 5 MHz low-pass filter, and a 4.43 MHz trap filter.

17. Let V1 be the Y-OUT output with a 200 kHz 400 mVp-p sine wave input and SW3 set to c, and let V2 be the C-OUT output with SW3 set to b.

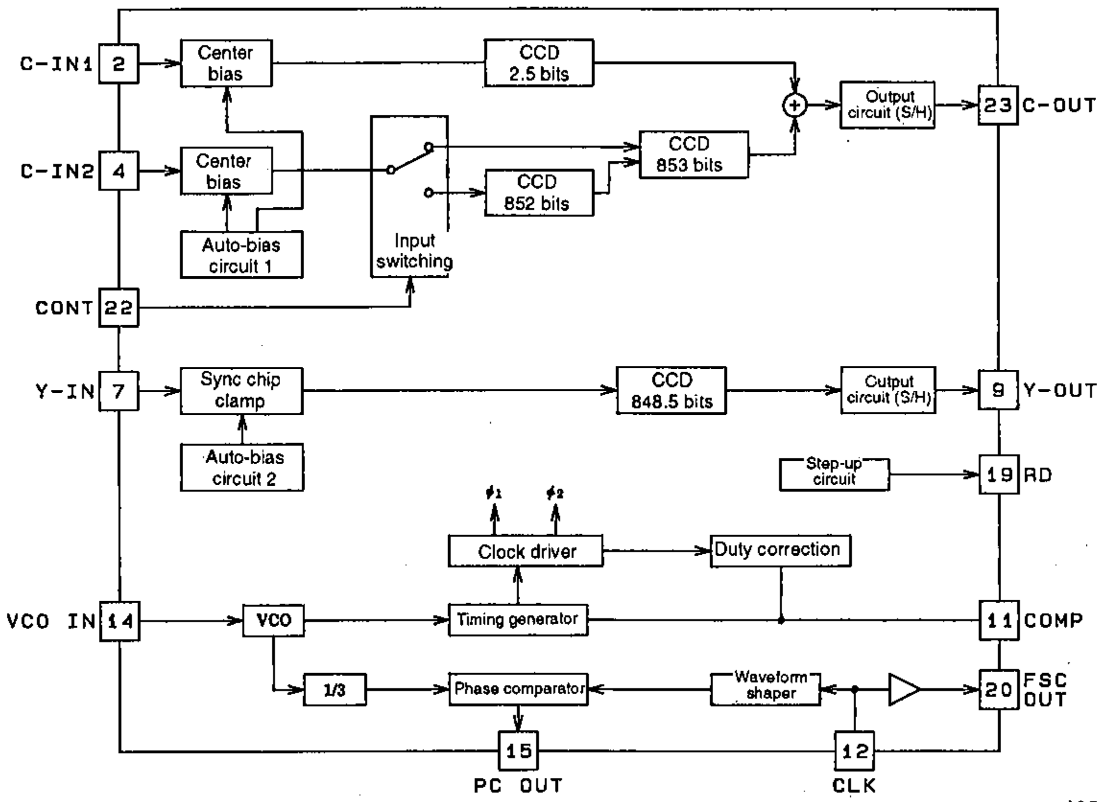
$$ZOY = \frac{V2\ [mVp\text{-}p] - V1\ [mVp\text{-}p]}{V1\ [mVp\text{-}p]} \times 500\ [\Omega]$$

18. The Y-OUT delay time with respect to Y-IN

Pin Assignment



Block Diagram



A03851

Control Pin Function

CONT	Mode (representative example)	Chrominance signal delay (CCD bits)	Luminance signal delay (CCD bits)
Low	PAL/GBI	2 H (1705) + 0 H (2.5)	1 H (848.5)
High	4.43 NTSC	1 H (853) + 0 H (2.5)	1 H (848.5)

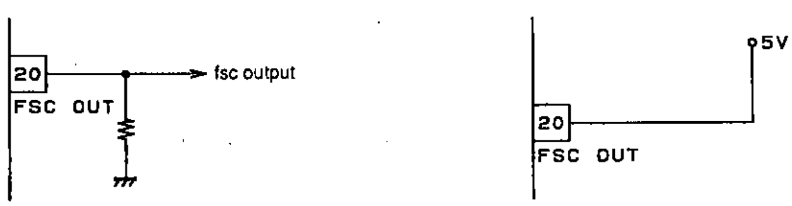
Switching Voltage Levels

Low/high	Symbol	min	typ	max	Unit
Low	V_L	–0.3	0.0	+0.5	V
High	V_H	2.0	5.0	6.0	V

Note: Since the control pin has a built-in pull-down resistor, the pin will be set to the low state if left open.

FSC OUT Pin Function

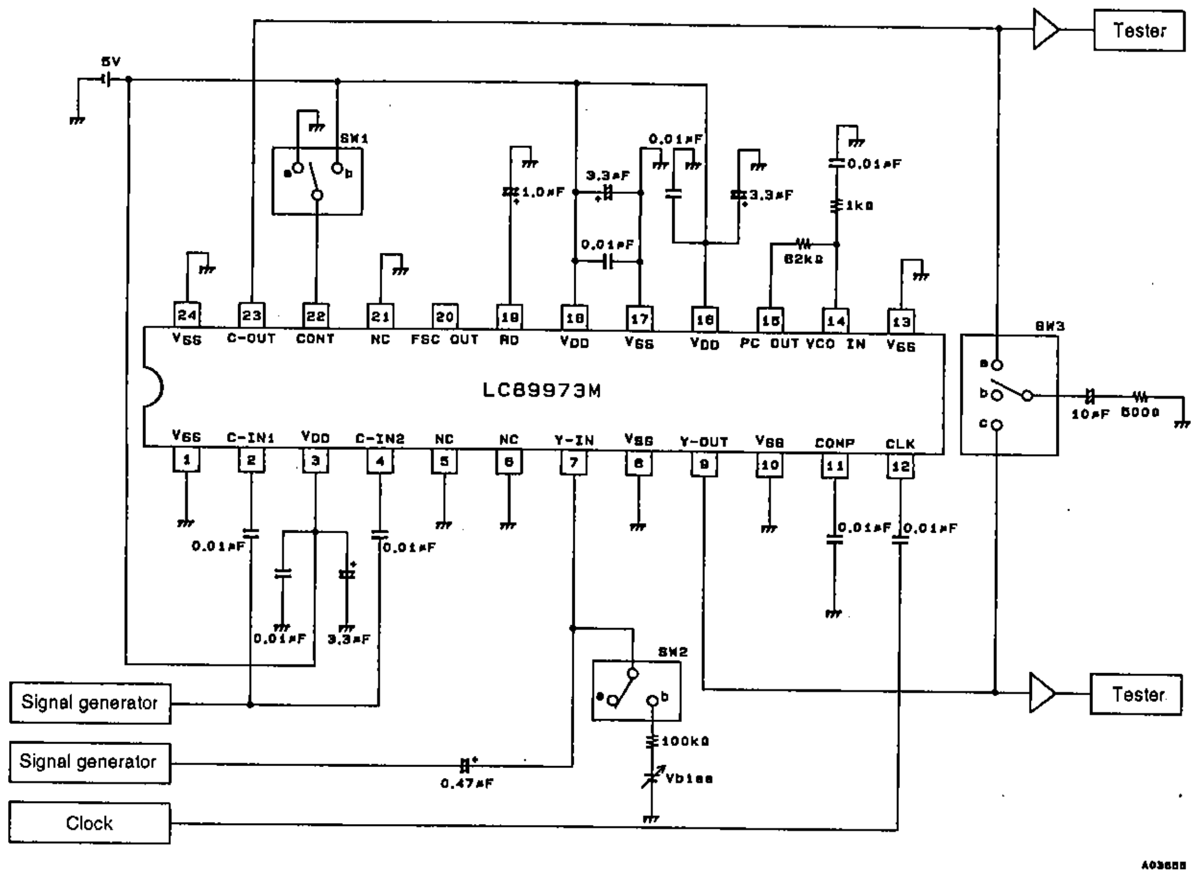
This pin provides a buffer output for the clock signal input to the CLK pin.



A03852

Note: Since this pin has a built-in pull-up resistor, the pin voltage will go to the supply voltage and output will cease if left open.

Test Circuit



No products described or contained herein are intended for use in surgical implants, life-support systems, aerospace equipment, nuclear power control systems, vehicles, disaster/crime-prevention equipment and the like, the failure of which may directly or indirectly cause injury, death or property loss.

- Anyone purchasing any products described or contained herein for an above-mentioned use shall:
  ① Accept full responsibility and indemnify and defend SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors and all their officers and employees, jointly and severally, against any and all claims and litigation and all damages, cost and expenses associated with such use:
  ② Not impose any responsibility for any fault or negligence which may be cited in any such claim or litigation on SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors or any of their officers and employees jointly or severally.

- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of June, 1995. Specifications and information herein are subject to change without notice.