

SANYO

No.2810A

LM7005**Electronic AV Tuner-Use Electronic Tuning
PLL Frequency Synthesizer****Features**

The LM7005 is an N-channel MOS LSI used as an AV tuner-use electronic tuning PLL frequency synthesizer converting a wide range of frequency bands from UHF to LW.

(1) Programmable divider

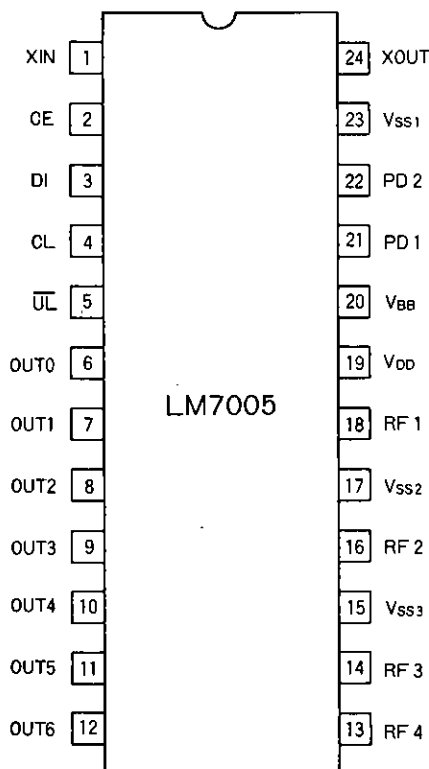
- RF 1 pin : 1/2 prescaler + 1/16 or 1/17 swallow counter + main counter
400MHz to 900MHz (18bits)
- RF 2 pin : 1/16 or 1/17 swallow counter + main counter
30MHz to 450MHz (18bits)
- RF 3 pin : 1/16 or 1/17 swallow counter + main counter
30MHz to 150MHz (18bits)
- RF 4 pin : Direct input to main counter
0.5MHz to 35MHz (14bits)

(2) Reference frequency

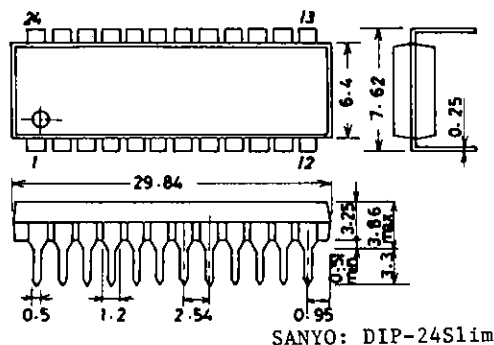
- Programmable divider (14bits)
220Hz to 450kHz at Fundamental Crystal (X'tal) oscillation frequency : 7.2MHz

(3) Unlock detection pin available**(4) Deadlock clear circuit available****(5) Output ports : 7 pins**

N-ch open drain output type

(6) Package : DIP24S (Slim)**Pin Assignment****Package Dimensions 3084**

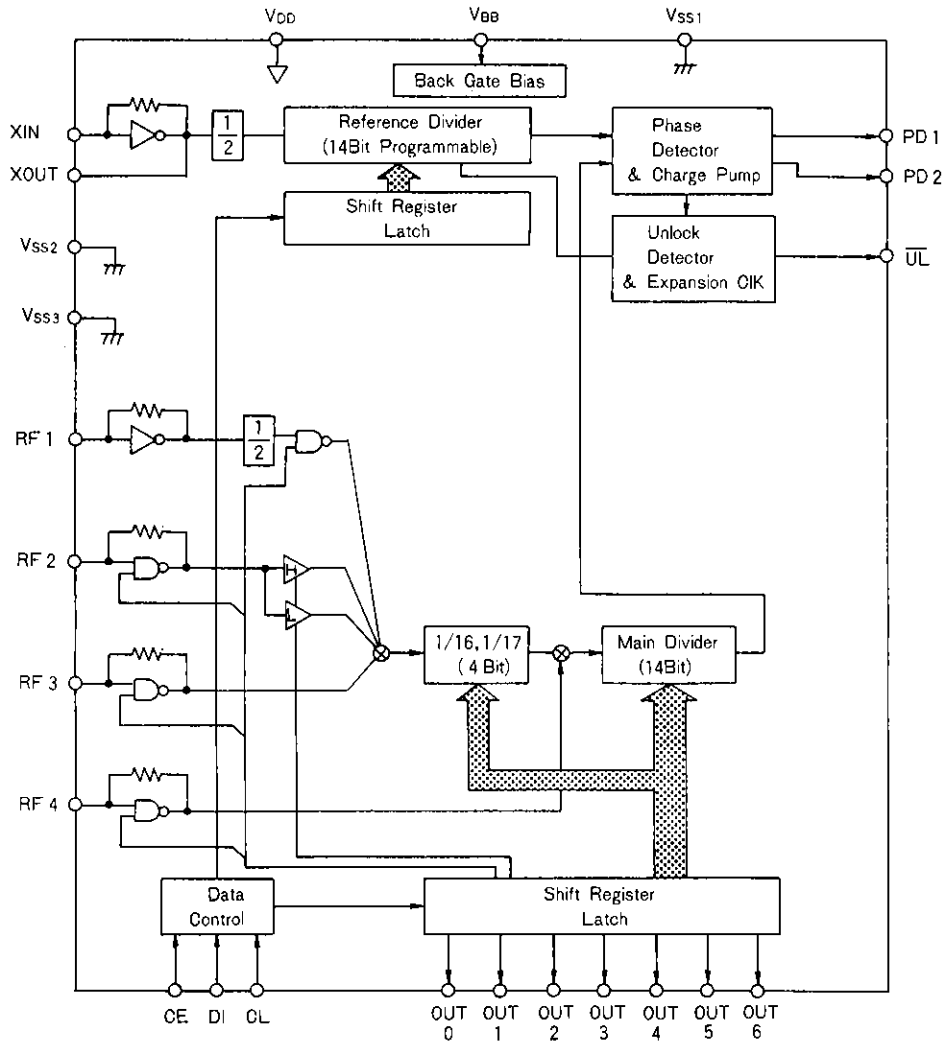
(unit: mm)




SANYO: DIP-24S11m

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Block Diagram



( : Input frequency selection)

Pin symbol

XIN, XOUT	: X'tal OSC
RF1 to RF4	: Local oscillation signal input
CE, DI, CL	: Serial data input
OUT0 to OUT6	: Output ports
UL	: Unlock signal output
PD1, PD2	: Charge pump output
VBB	: Back gate bias input
VDD	: Supply voltage
VSS1, VSS2, VSS3	: Ground

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Absolute Maximum Ratings at $T_a = 25^\circ\text{C}, V_{SS} = 0\text{V}$

				unit
Maximum Supply Voltage	$V_{DD \text{ max}}$	V_{DD}	-0.3 to 6.0	V
Back Gate Bias Input	V_{BB}	V_{BB}	-4.0 to -2.0	V
Input Voltage	$V_{IN(1)}$	CE,CL,DI	-0.3 to 6.0	V
	$V_{IN(2)}$	Input pins other than $V_{IN(1)}$	-0.3 to $V_{DD} + 0.3$	V
Output Voltage	V_{OUT}	OUT0 to OUT6, \overline{UL}	-0.3 to 15	V
Output Current	$I_{OL \text{ max}}$	OUT0 to OUT6, \overline{UL}	3.0	mA
Allowable Power Dissipation	$P_d \text{ max}$	$T_a \leq 85^\circ\text{C}$	430	mW
Operating Temperature	T_{opr}		-40 to +85	$^\circ\text{C}$
Storage Temperature	T_{stg}		-55 to +125	$^\circ\text{C}$

Allowable Operating Conditions at $T_a = -40$ to $+85^\circ\text{C}, V_{SS} = 0\text{V}$

			min	typ	max	unit
Supply Voltage	V_{DD}	V_{DD}	4.5		5.5	V
'H'-Level Input Voltage	V_{IH}	CE,CL,DI	2.2		5.5	V
'L'-Level Input Voltage	V_{IL}	CE,CL,DI	0		0.7	V
Output Voltage	V_{OUT}	OUT0 to OUT6, \overline{UL}	0		13	V
Input Frequency	$f_{IN(1)}$	XIN	1.0		16	MHz
						Capacitor coupled sine wave input :
	$f_{IN(2)}$	RF1	400		900	MHz
						sine wave input : SP = *
	$f_{IN(3)}$	RF2	100		450	MHz
						sine wave input : SP = 1
	$f_{IN(4)}$	RF2	30		150	MHz
					sine wave input : SP = 0	
$f_{IN(5)}$	RF3	30		150	MHz	
					Capacitor coupled sine wave input : SP = *	
$f_{IN(6)}$	RF4	0.5		35	MHz	
					Capacitor coupled sine wave input : SP = *	
Guaranteed Crystal Oscillation Resonator	X'tal	XIN-XOUT	3.0	7.2	8.0	MHz
Input Amplitude	$V_{IN(1)}$	XIN	0.5		1.5	Vrms
						Capacitor coupled sine wave input
	$V_{IN(2)}$	RF1	0.1		1.5	Vrms
						Capacitor coupled sine wave input
	$V_{IN(3)}$	RF2	0.1		1.5	Vrms
					Capacitor coupled sine wave input	
$V_{IN(4)}$	RF3	0.1		1.5	Vrms	
					Capacitor coupled sine wave input	
$V_{IN(5)}$	RF4	0.1		1.5	Vrms	
					Capacitor coupled sine wave input	

Note : SP is one of the control data bits, which is used for selecting a desired input frequency band.

(* Don't care)

Electrical Characteristics under recommended operating conditions

			min	typ	max	unit
On-chip Feedback Resistor	$R_f(1)$	XIN		1.0		$\text{M}\Omega$
	$R_f(2)$	RF1		500		$\text{k}\Omega$
	$R_f(3)$	RF2		500		$\text{k}\Omega$
	$R_f(4)$	RF3		500		$\text{k}\Omega$
	$R_f(5)$	RF4		500		$\text{k}\Omega$
'H'-Level Input Current	$I_{IH(1)}$	CE,CL,DI			5.0	μA
	$I_{IH(2)}$	XIN			20	μA
	$I_{IH(3)}$	RF1,2,3,4			40	μA
'L'-Level Input Current	$I_{IL(1)}$	CE,CL,DI			5.0	μA
	$I_{IL(2)}$	XIN			20	μA
	$I_{IL(3)}$	RF1,2,3,4			40	μA

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				min	typ	max	unit
'H'-Level Output Voltage	V_{OH}	PD1,PD2	$I_O = 0.1mA$	$0.6V_{DD}$			V
'L'-Level Output Voltage	$V_{OL(1)}$	PD1,PD2	$I_O = 0.1mA$			0.3	V
	$V_{OL(2)}$	OUT0 to OUT6, \overline{UL}	$I_O = 2mA$			1.0	V
Output OFF Leak Current	I_{OFF}	OUT0 to OUT6, \overline{UL}	$V_O = 13V$			5.0	μA
'H'-Level Tri-State OFF Leak Current	I_{OFFH}	PD1,PD2	$V_O = V_{DD}$		0.01	10.0	nA
'L'-Level Tri-State OFF Leak Current	I_{OFFL}	PD1,PD2	$V_O = V_{SS}$		0.01	10.0	nA
Input Capacitance	C_{IN}	RF1			2.5		pF
Supply Current	I_{DD}				55	80	mA

$f_{IN(2)} = 900MHz,$
 $V_{IN(2)} = 100mV_{rms},$
 $X'tal = 7.2MHz,$
 other input pins = $V_{SS},$
 output pins = open

[1] Pin Description

Symbol	Pin No.	Contents	Functional Description	I/O Type
XIN XOUT	1 24	X'tal OSC	Crystal oscillation frequency input pin. Connected with the crystal oscillation resonator with an oscillation frequency of 7.2MHz.	Input Output
RF1	18	Local oscillation signal frequency input	<ul style="list-style-type: none"> · Serial data input pin : This input pin is selected when bits DV0 and DV1 are set to 0. The serial input data to this pin is transmitted to a programmable divider circuit. · The input frequency range is between 400MHz and 900MHz (100mVrms : Minimum). · The input signal is transmitted to the swallow counter via the internal prescaler. · The settable division ratio is between 256 and 262143. Please note that the actual division ratio will be twice the value set because the internal prescaler is provided. 	Input
RF2	16	Local oscillation signal frequency input	<ul style="list-style-type: none"> · Serial data input pin : This pin is selected when control data bits DV0 and DV1 are set to 1 and 0, respectively. The input serial data to this pin is transmitted to a programmable divider circuit. · Serial input data with control data bit SP = 1 : <ul style="list-style-type: none"> · The input frequency range is between 100 MHz and 450MHz (100mVrms : Minimum). · The input signal frequency to this pin is directly transmitted to the swallow counter, not via the 1/2 internal prescaler. · The settable division ratio can be between 256 and 262143. · Serial input data with control data bit SP = 0 : <ul style="list-style-type: none"> · The input signal frequency is between 30MHz and 150MHz (100mVrms : Minimum). · The input signal frequency is directly transmitted to the swallow counter, not via the 1/2 internal prescaler. · The settable division ratio can be between 256 and 262143. 	Input

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Symbol	Pin No.	Contents	Functional Description	I/O Type
RF3	14	Local oscillation signal frequency input	<ul style="list-style-type: none"> Serial data input pin : This pin is selected when control data bits DV0 and DV1 are set to 0 and 1, respectively. The serial input data to this pin is transmitted to a programmable divider circuit. The input frequency range is between 30MHz and 150MHz (100mVrms : Minimum). The input signal frequency is directly transmitted to the swallow counter, not via the 1/2 internal prescaler. The settable division ratio can be between 256 and 626143. 	Input
RF4	13	Local oscillation signal frequency input	<ul style="list-style-type: none"> Serial data input pin : This is selected when control data bits DV0 and DV1 are set to 1. The input serial data to this pin is transmitted to a programmable divider circuit. The input frequency range is between 0.5MHz and 35MHz. The input signal frequency is directly transmitted to the 14-bit main divider. The settable division ratio is between 16 and 16383. 	Input
PD1	21	Phase comparator	<ul style="list-style-type: none"> Charge pump output from the PLL circuit : H-level output - - - Reference frequency (fref) < fosc/N. L-level output - - - Reference frequency (fref) > fosc/N. Floating state - - - Reference frequency (fref) = fosc/N. Note : fosc/N = local oscillation signal frequency divided by N. 	Output (Tri-state)
PD2	22	Charge pump output		
\overline{UL}	5	Unlock detection output	<ul style="list-style-type: none"> Used for PLL lock/unlock state output. <ul style="list-style-type: none"> PLL in lock state : Open-circuited. PLL in unlock state : Low For more information, refer to the unlock detection circuit. 	Output [N-ch open drain circuit type]
CE	2	Chip enable signal input	<ul style="list-style-type: none"> Set this pin to the H-level state to input serial data to the LM7005. 	Input ※
CL	4	Clock pulse input	<ul style="list-style-type: none"> Provide synchronization timings for inputting serial data into the LM7005. 	Input ※
DI	3	Serial data input	<ul style="list-style-type: none"> Pin for inputting serial data to the LM7005. To set the initial value in the LM7005, the total number of 56 bits must be used. 	Input ※
OUT0 OUT1 OUT2 OUT3 OUT4 OUT5 OUT6	6 7 8 9 10 11 12	Output port	<ul style="list-style-type: none"> Output ports used for outputting the 7-bit serial data from the controller to an external circuit. This synthesizer receives 7-bit serial data O0 to O6 from the controller and then latches it into the shift register. That 7-bit serial data is then output in parallel to an external device from these 7 ports. Data logic "1" : Open-circuited Data logic "0" : Low Withstand voltage level : 13V 	Output [N-ch open drain circuit type]

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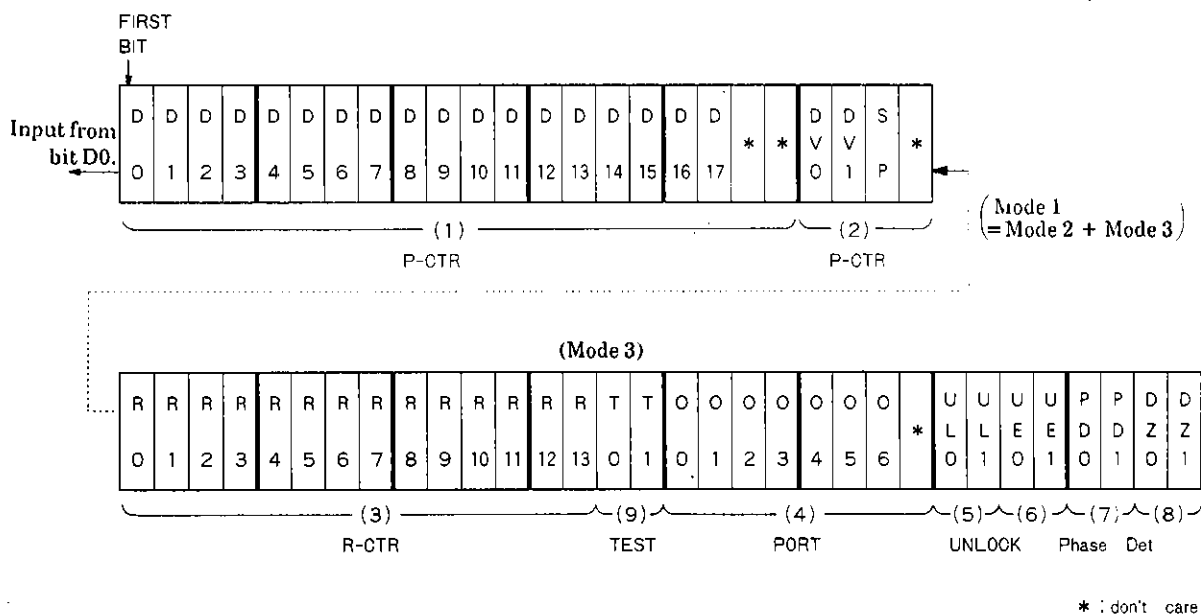
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Symbol	Pin No.	Contents	Functional Description	I/O Type
V _{BB}	20	Back gate bias input	· Pin for back gate bias input (The capacitor of 0.01 μF is needed between this pin and the ground.)	—
V _{DD}	19	Supply voltage	· Supply voltage pin. (Supply voltage : 4.5V to 5.5V)	—
V _{SS1}	23	Ground	· Ground pin	—
V _{SS2}	17	Ground	· Ground pin for high frequency signal : For RF1 pin	—
V _{SS3}	15	Ground	· Ground pin for high frequency signal : For RF2/3/4 pin	—

※ H-level input voltage for pins CE, CL and DI : 2.2V to 5.5V (V_{IH}). L-level input voltage for pins CE, CL and DI : 0V to 0.7V (V_{IL}). These voltage levels are independent of the supply voltage (V_{DD}).

[2] Control data (serial data) configuration



The serial data for controlling the LM7005 consists of 56 bits. After the power on, all the 56 bits must be input to the LM7005 for initialization.

Mode 1 : The LSI test mode selection data (T0 and T1) must be set to 0.

Mode 2 : The 24 bits from D0 to * must be used.

Mode 3 : The 32 bits from R0 to DZ1 must be used.

○ : Input required, — : Input not required.

	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)
Mode 1	○	○	○	○	○	○	○	○	○
Mode 2	○	○	—	—	—	—	—	—	—
Mode 3	—	—	○	○	○	○	○	○	○

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[3] Control data bit description

No.	Data	Description	Associated data bits																																				
(1)	Programmable divider control data D0 to D17 : Specify a desired division ratio	<p>The control data (D0 to D17) must be input to the LM7005 for setting a desired division ratio in the programmable divider circuit. This control data is a binary value. Bit D17 is the most significant bit (MSB) of the control data. The least significant bit (LSB) of this control data depends on bits DV0 and DV1 as shown in the table below.</p> <table border="1"> <thead> <tr> <th>DV0</th> <th>DV1</th> <th>Pin</th> <th>LSB</th> <th>Settable division ratio</th> <th>Actual division ratio</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>RF1</td> <td>D0</td> <td>256 to 262143</td> <td>Division ratio set × 2</td> </tr> <tr> <td>1</td> <td>0</td> <td>RF2</td> <td>D0</td> <td>256 to 262143</td> <td>Division ratio set</td> </tr> <tr> <td>0</td> <td>1</td> <td>RF3</td> <td>D0</td> <td>256 to 262143</td> <td>Division ratio set</td> </tr> <tr> <td>1</td> <td>1</td> <td>RF4</td> <td>D4</td> <td>16 to 16383</td> <td>Division ratio set</td> </tr> </tbody> </table> <p>If LSB = D4 (RF4), bits D0 to D3 can be set to either 0 or 1.</p>	DV0	DV1	Pin	LSB	Settable division ratio	Actual division ratio	0	0	RF1	D0	256 to 262143	Division ratio set × 2	1	0	RF2	D0	256 to 262143	Division ratio set	0	1	RF3	D0	256 to 262143	Division ratio set	1	1	RF4	D4	16 to 16383	Division ratio set	DV0 DV1 SP						
DV0	DV1	Pin	LSB	Settable division ratio	Actual division ratio																																		
0	0	RF1	D0	256 to 262143	Division ratio set × 2																																		
1	0	RF2	D0	256 to 262143	Division ratio set																																		
0	1	RF3	D0	256 to 262143	Division ratio set																																		
1	1	RF4	D4	16 to 16383	Division ratio set																																		
(2)	DV0 and DV1 : Divider selection data SP : Select a desired input frequency band	<p>Bits DV0 and DV1 are used to select a desired local oscillation signal input pin from RF1 to RF4. Bit SP has meaning if RF2 pin has been selected. This bit is used to select a desired input frequency range. * : Do not care.</p> <table border="1"> <thead> <tr> <th>DV0</th> <th>DV1</th> <th>Pin</th> <th>SP</th> <th>H/L</th> <th>Settable division ratio</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>RF1</td> <td>*</td> <td>-</td> <td>400MHz to 900MHz</td> </tr> <tr> <td>1</td> <td>0</td> <td>RF2</td> <td>1</td> <td>H</td> <td>100MHz to 450MHz</td> </tr> <tr> <td></td> <td></td> <td></td> <td>0</td> <td>L</td> <td>30MHz to 150MHz</td> </tr> <tr> <td>0</td> <td>1</td> <td>RF3</td> <td>*</td> <td>-</td> <td>30MHz to 150MHz</td> </tr> <tr> <td>1</td> <td>1</td> <td>RF4</td> <td>*</td> <td>-</td> <td>0.5MHz to 35MHz</td> </tr> </tbody> </table>	DV0	DV1	Pin	SP	H/L	Settable division ratio	0	0	RF1	*	-	400MHz to 900MHz	1	0	RF2	1	H	100MHz to 450MHz				0	L	30MHz to 150MHz	0	1	RF3	*	-	30MHz to 150MHz	1	1	RF4	*	-	0.5MHz to 35MHz	D0 to D17
DV0	DV1	Pin	SP	H/L	Settable division ratio																																		
0	0	RF1	*	-	400MHz to 900MHz																																		
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0	1	RF3	*	-	30MHz to 150MHz																																		
1	1	RF4	*	-	0.5MHz to 35MHz																																		
(3)	R0 to R13 : Select a desired reference frequency	<p>Bits R0 to R13 are used to set a desired division ratio in the reference divider circuit. The control data (R0 to R13) is a binary value. The least significant bit (LSB) of this control data is R0. Settable division ratio : 8 to 16383. Actual division ratio = division ratio set × 2 Reference frequency = Crystal oscillation frequency : XIN / actual division ratio</p>	UL0 UL1 UE0 UE1																																				
(4)	O0 to O6 : Specify output port data	<p>Bits O0 to O6 are used to determine the output data to an external device from ports OUT0 to OUT6. The control data (O0 to O6) is input to the LM7005 from the controller and then latched into the shift register. The content of the shift register is output to an external device from output ports OUT0 to OUT6. Each output port consists of an N-ch open drain output circuit and enters the following state :</p> <ul style="list-style-type: none"> · Data logic "1" : Open-circuited · Data logic "0" : Low 	-																																				

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No.	Data	Description	Associated data bits																																			
(5) (6)	UL0 and UL1, and UE0 and UE1 : Unlock detection data bits	<ul style="list-style-type: none"> Data bits (UL0 and UL1) are used for detecting a pulse width of a phase error signal from the phase comparator to the pulse width detection circuit. Data bits (UE0 and UE1) are used to specify a desired expansion time data for output unlock signal from the LM7005 to an external circuit. <table border="1" data-bbox="549 517 1254 701"> <thead> <tr> <th>UL0</th> <th>UL1</th> <th>Phase error signal detection width</th> <th>Division ratio for reference divider</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Direct</td> <td>8 or more</td> </tr> <tr> <td>1</td> <td>0</td> <td>$\pm 4/f_{x'tal}$ or longer</td> <td>8 or more</td> </tr> <tr> <td>0</td> <td>1</td> <td>$\pm 16/f_{x'tal}$ or longer</td> <td>24 or more</td> </tr> <tr> <td>1</td> <td>1</td> <td>$\pm 64/f_{x'tal}$ or longer</td> <td>96 or more</td> </tr> </tbody> </table> <p style="text-align: center;">($f_{x'tal}$: Crystal oscillation frequency)</p> <table border="1" data-bbox="544 779 1259 925"> <thead> <tr> <th>UE0</th> <th>UE1</th> <th>Expansion time = N cycles of a selected reference frequency</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>8 cycles</td> </tr> <tr> <td>1</td> <td>0</td> <td>64 cycles</td> </tr> <tr> <td>0</td> <td>1</td> <td>128 cycles</td> </tr> <tr> <td>1</td> <td>1</td> <td>512 cycles</td> </tr> </tbody> </table> <ul style="list-style-type: none"> For more information, please refer to the unlock detection circuit to be later discussed. 	UL0	UL1	Phase error signal detection width	Division ratio for reference divider	0	0	Direct	8 or more	1	0	$\pm 4/f_{x'tal}$ or longer	8 or more	0	1	$\pm 16/f_{x'tal}$ or longer	24 or more	1	1	$\pm 64/f_{x'tal}$ or longer	96 or more	UE0	UE1	Expansion time = N cycles of a selected reference frequency	0	0	8 cycles	1	0	64 cycles	0	1	128 cycles	1	1	512 cycles	R0 to R13
UL0	UL1	Phase error signal detection width	Division ratio for reference divider																																			
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0	0	8 cycles																																				
1	0	64 cycles																																				
0	1	128 cycles																																				
1	1	512 cycles																																				
(7)	PD0 and PD1 : Charge pump output control data	<ul style="list-style-type: none"> These two bits are used to control the charge pump outputs (PD1 and PD0). When the PLL is forced into a deadlock state, these data bits are used to control the charge pump outputs and then allows the PLL to exit from the deadlock state. <table border="1" data-bbox="691 1211 1090 1361"> <thead> <tr> <th>PD0</th> <th>PD1</th> <th>Charge pump output</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Normal operation</td> </tr> <tr> <td>1</td> <td>0</td> <td>High</td> </tr> <tr> <td>0</td> <td>1</td> <td>Low</td> </tr> <tr> <td>1</td> <td>1</td> <td>Floating</td> </tr> </tbody> </table>	PD0	PD1	Charge pump output	0	0	Normal operation	1	0	High	0	1	Low	1	1	Floating	-																				
PD0	PD1	Charge pump output																																				
0	0	Normal operation																																				
1	0	High																																				
0	1	Low																																				
1	1	Floating																																				
(8)	DZ0 and DZ1 : Dead zone control data	<ul style="list-style-type: none"> These two data bits are used to select a desired dead zone for the phase detector from the following four options. DZC > DZB > DZA <table border="1" data-bbox="691 1547 1090 1697"> <thead> <tr> <th>DZ0</th> <th>DZ1</th> <th>Dead zone</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>DZA</td> </tr> <tr> <td>1</td> <td>0</td> <td>DZB</td> </tr> <tr> <td>0</td> <td>1</td> <td>DZC</td> </tr> <tr> <td>1</td> <td>1</td> <td>Input inhibited</td> </tr> </tbody> </table>	DZ0	DZ1	Dead zone	0	0	DZA	1	0	DZB	0	1	DZC	1	1	Input inhibited	-																				
DZ0	DZ1	Dead zone																																				
0	0	DZA																																				
1	0	DZB																																				
0	1	DZC																																				
1	1	Input inhibited																																				
(9)	T0 and T1 : LSI test data	<ul style="list-style-type: none"> These two data bits are used to select a desired test mode. They have nothing to do with the user operation. Normally, these bits are set to 0. Note that these data bits must be always set to "0" right after power is supplied. 	-																																			

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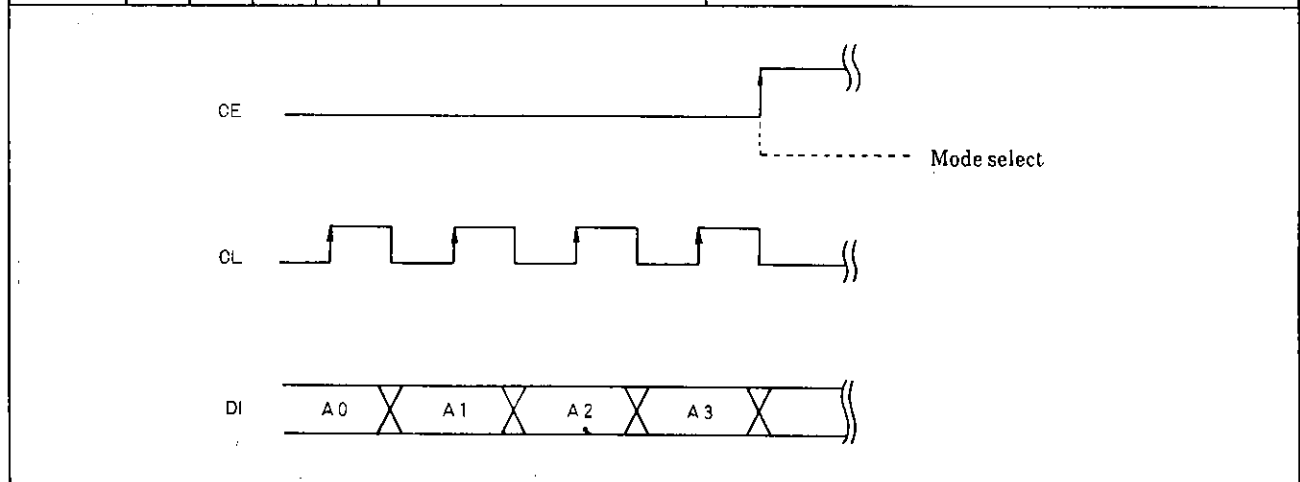
[4] Control data (serial data) entry

There are three control data entry modes available on the LM7005. Control data can be input to this LSI after one of the three entry modes has been selected.

The one of the three entry modes can be selected by four data bits (A0 to A3) input to the DI pin before the CE pin level becomes High. Note that these four bits are input to the LSI on the rising edge of the clock pulses input to the CL pin.

The timing chart is given under the table below.

Mode	A0	A1	A2	A3	Function Description	Operations Description
1	1	0	0	0	All the control data bits need to be input.	· This mode allows all the 56 control data bits to be input to the LM7005. This mode must be used for initializing the LSI immediately after power is applied.
2	0	1	0	0	Only the control data bits for controlling the programmable divider need to be input.	· This mode allows only the 24 control data bits (D0 to SP, *) to be input to the LM7005. The other bits than the 32 bits remain unchanged.
3	1	1	0	0	Only the control data bits for controlling the reference divider need to be input.	· This mode allows only the 32 control data bits (R0 to DZ1) to be input to the LM7005. The other bits than the 24 bits remain unchanged.
	0 to 0	0 to 0	1 to 0	0 to 0	Invalid	· This is an invalid mode. No control data can not be input to the LSI.



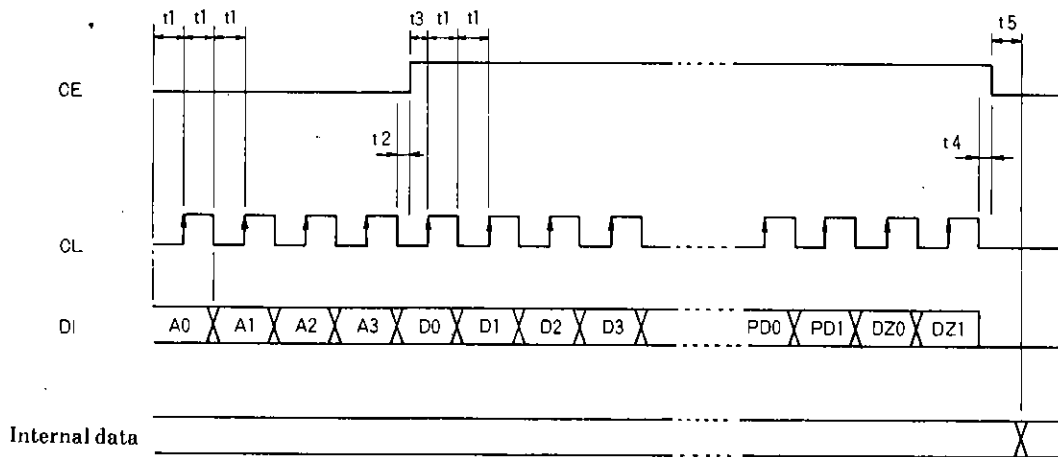
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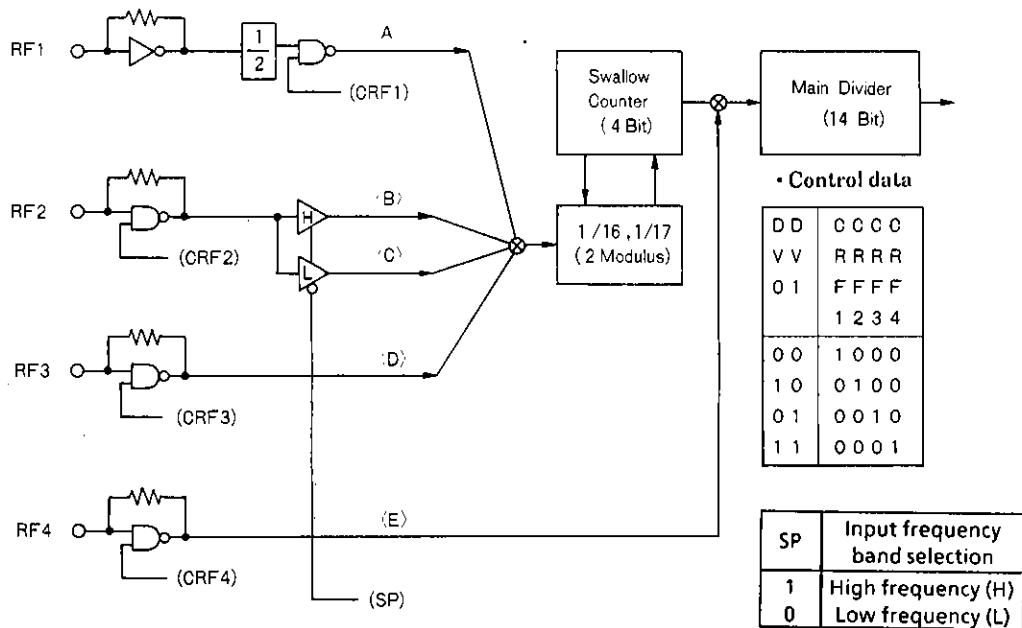
[5] Serial control data input timing



$t1 > 5/fx'ta1$ (0.7μs) $t2 > 0$ $t3 > 5/fx'ta1$ (0.7μs)
 $t4 > 0$ $t5 > 5/fx'ta1$ (0.7μs) ※ $fx'ta1$: Crystal oscillation frequency
 The constants in parentheses apply to the case where $fx'ta1 = 7.2\text{MHz}$.

- Mode 1: This mode allows the user to input 60 bits to the DI pin : 4 mode selection data bits + 56 control data bits
- Mode 2: This mode allows the user to input 28 bits to the DI pin : 4 mode selection data bits + 24 control data bits
- Mode 3: This mode allows the user to input 36 bits to the DI pin : 4 mode selection data bits + 32 control data bits

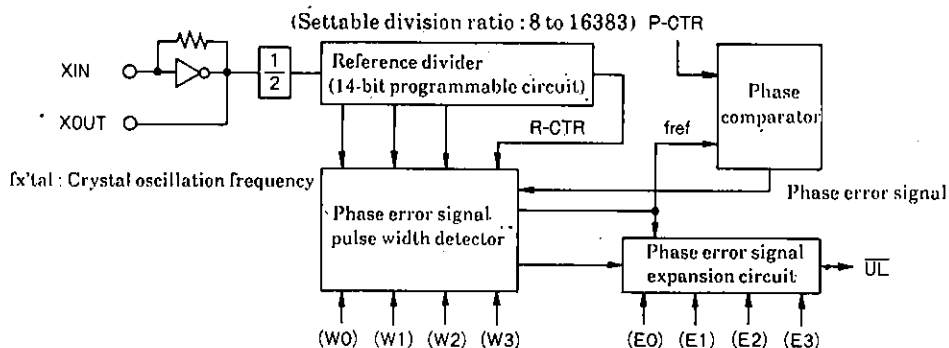
[6] Programmable divider circuit configuration



Pin	DV0	DV1	Settable division ratio	Actual division ratio	SP	Channel	Input frequency range	Frequency band
RF1	0	0	256 to 262134	Division ratio set × 2	*	(A)	400MHz to 900MHz	UHF
PF2	1	0	Same as above	Division ratio set	1	(B)	100MHz to 450MHz	VHF
					0	(C)	30MHz to 150MHz	FM
RF3	0	1	Same as above	Division ratio set	*	(D)	30MHz to 150MHz	FM
RF4	1	1	16 to 16383	Division ratio set	*	(E)	0.5MHz to 35MHz	SW,MW,LW

DV0, DV1 and SP: Control data bits and * indicates that any bit value will be accepted.

[7] Unlock detector circuit configuration



UL0	UL1		Phase error detector	Division ratio set for reference divider	Detection pulse width at $f_{x'tal} = 7.2\text{MHz}$
0	0	W0	(Direct output) *	8 or greater	—
1	0	W1	$\pm 4/f_{x'tal}$ or longer	8 or greater	$\pm 0.56\mu\text{s}$ or greater
0	1	W2	$\pm 16/f_{x'tal}$ or longer	24 or greater	$\pm 2.23\mu\text{s}$ or greater
1	1	W3	$\pm 64/f_{x'tal}$ or longer	96 or greater	$\pm 8.89\mu\text{s}$ or greater

UL0	UL1		Expansion time period = N cycles of f_{ref} (reference frequency)	Reference frequency : $f_{ref} = 100\text{kHz}$
0	0	E0	8 cycles	0.08ms
1	0	E1	64 cycles	0.64ms
0	1	E2	128 cycles	1.28ms
1	1	E3	512 cycles	5.12ms

UL0, UL2, UE0 and UE1 : Control data bits and * indicates that phase error signal pulse width will not be expanded.

- Phase error signal detection width is closely related to a division ratio set in the reference divider. Please keep it in mind.
- Phase error signal detection width and expansion time period are determined by a crystal oscillation resonator frequency and a selected reference frequency. Please keep it in mind.

Example : Crystal oscillation resonator --- 7.2MHz. Reference frequency --- 100kHz

- ① Division ratio set in the reference divider : $7.2\text{MHz} \div 100\text{kHz} \div 2 = 36$
- ② Phase error signal detection width : $UL0=0, UL=1 \rightarrow W2$ --- $\pm 2.23\mu\text{s}$ or greater. Note that W3 cannot be selected.
- ③ Expansion time period : $UE0=UE1=1 \rightarrow E3$ --- 5.12msec.

