Ordering number : EN4127

CMOS LSI

No. 4127

LC8954

Error Correction and AD PCM Playback LSI for CD-I Applications

Overview

The LC8954 is an error correction and AD PCM decoder LSI for CD-I applications, and integrates in a single chip selected functions from the Sanyo LC8951, LC8955 and LC8953 products. Of the hardware required for CD-I applications, the LC8954 integrates all of the CD player output peripheral circuits in a single chip.

Functions

The LC8954 can be roughly divided into three blocks.

- Error correction block
  - — This block corrects the errors in the CD-ROM data output from the CD player block.
  - — The CD-ROM data output from the CD player block is temporarily buffered in the LC8954 external SRAM. Error correction is performed automatically after one sector has been buffered. After error correction, a CPU interrupt is issued. The CPU checks that the error correction completed normally, and transfers data from the SRAM using the LC8954. Real time performance is achieved by pipelining the buffering, error correction, and data transfer operations.
  - — Nominally error corrected (but actually not corrected) AD PCM data is transferred at the discretion of the CPU to the audio block.
  - — Control of the buffering, error correction, and other functions is performed by register settings.
- AD PCM decoder block
  - — Error corrected AD PCM data is transferred to the AD PCM decoder block (audio block) at the discretion of the CPU. Actually, data is read from the LC8954 external SRAM error correction area and written to the audio area. Then, the audio block begins playback by reading data from the audio area.
  - — The LC8954 supports automatic playback of levels A, B, and C and stereo/mono signals based on subheader data.
  - — Expanded data is input to the audio processor circuit, and output to the D/A converter according to the gain value set in the LC8954 registers.
  - — The LC8954 can be directly connected to the Sanyo LC78835 and LC78835M (8× oversampling digital filter + D/A converter). CD-DA output from the audio pins is also supported by internal register settings.
- 68000 interface block
  - — The LC8954 can be connected directly to a 68000 CPU.
  - — The data output from the error correction block is output after being converted from an 8-bit to a 16-bit format. Similarly, the sound map written to the AD PCM block is written after being converted from a 16-bit to an 8-bit format.
  - — The two pins ACK and RDY are provided for the interface to the DMA controller. Data can be transferred in single address mode, burst mode, or cycle stealing mode.

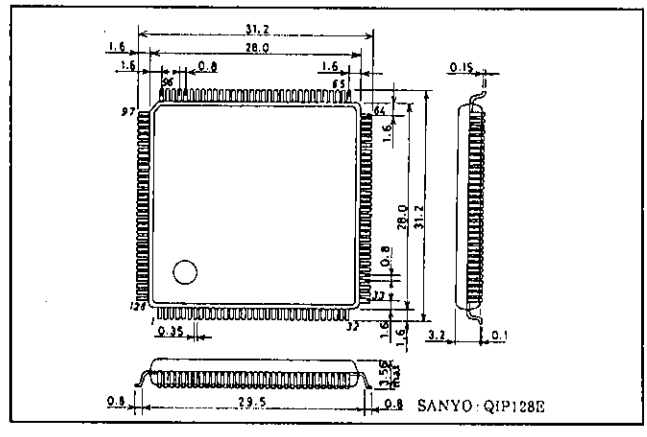
Features

- Can be directly connected to a 68000 CPU.
- Built-in DMA controller interface
- Built-in APU circuit that supports independent gain settings in four channels
- Can be directly connected to the Sanyo LC78835 and LC78835M (digital filter and D/A converter)
- Features from the LC8951 and LC8955 are inherited by the LC8954.
- Subcode interface on-chip
- External SRAM access from sub-CPU
- CMOS single voltage power supply: 5 V
- By combining features from the LC8951, LC8955, and portions of theLC8953 into one chip, the peripheral section of a CD player within a CD-I system can be constructed with just one chip.

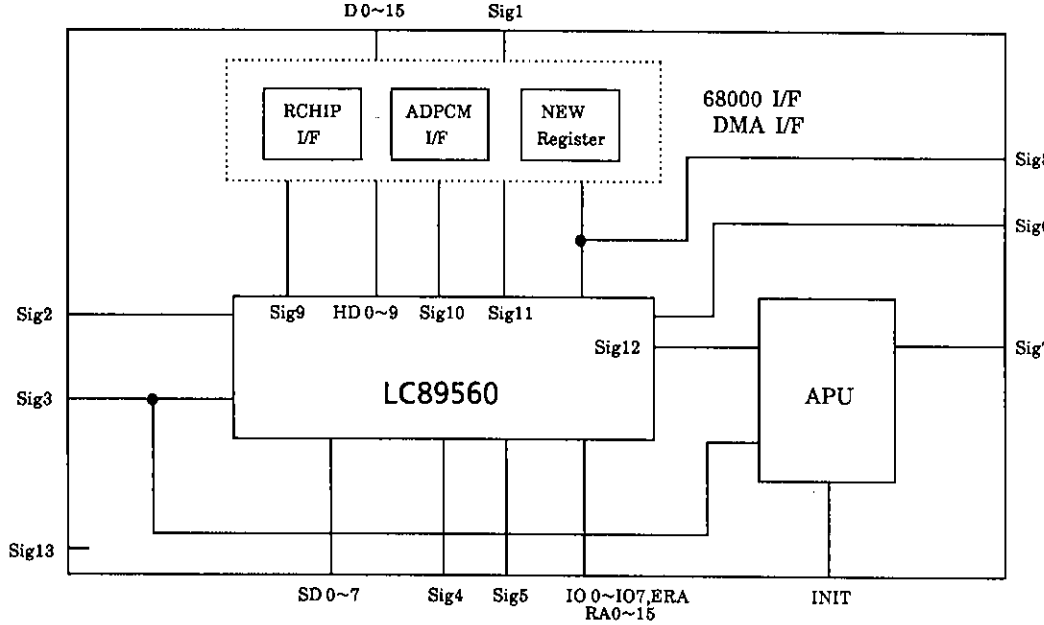
Package Dimensions

unit: mm

3182-QIP128E



Block Diagram



Sig1: ZCSCDIC, A1 to 5, ZAS, ZUDS, ZLDS, R/W, ZHINT0, ZHINT1, ZDTACK, CPUCLK, CDPORT0, CDPORT1, ZDRQ0, ZDRQ1, ZACK0, ZACK1, ZRDY0, ZRDY1, ZDONE
Sig2: MCK, WFCK, EXCK, SBSO, SCOR, C2PO, CEMPHAS, ADPCLK
Sig3: LRCK, SDATA, BCK
Sig4: SUA0 to 5, ZSWAIT, ZINT, RS, ZRD, ZWR, ZCS, SCPUCNT
Sig5: ZROE, ZRWE
Sig6: MBITSPL, MSPLFRQ, MSTEMON, MEMPHAS, SOC1, DACCK
Sig7: OLRCK, ODATA, OBCLK
Sig8: BUFFULL, DATAEMP, UNDFLOW
Sig9: ZWAIT, ZSTEN, ZDTEN, ZHWR, ZHRD, ZCMD
Sig10: SA0, SA1, ZAPCS, BUSY
Sig11: NEW READ WRITE SIGNAL
Sig12: INLRCK, INBCK, INDATA
Sig13: EXTAL, XTAL, TEST0 to 2, ZRESET

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		−0.3 to +7.0	V
Maximum input and output voltages	V_I V_O max		−0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max	Ta ≤ 70°C	600	mW
Operating temperature	Topr		−30 to +70	°C
Storage temperature	Tstg		−55 to +125	°C
Solder withstand temperature		For 10 seconds, and with only the pins immersed	260	°C

Allowable Operating Ranges at Ta = −30 to +70°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}		4.5	5.0	5.5	V
Input voltage range	V_{IN}		0		V_{DD}	V

Electrical Characteristics

DC Characteristics at Ta = –30 to +70°C, V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high level voltage	$V_{IH}1$	TTL level: all input pins other than (1), (2), and EXTAL	2.2			V
Input low level voltage	$V_{IL}1$	TTL level: all input pins other than (1), (2), and EXTAL			0.8	V
Input high level voltage	$V_{IH}2$	TTL level, Schmitt: (1)	2.5			V
Input low level voltage	$V_{IL}2$	TTL level, Schmitt: (1)			0.6	V
Input high level voltage	$V_{IH}3$	TTL level, built-in pull-up resistor: (2)	2.5			V
Input low level voltage	$V_{IL}3$	TTL level, built-in pull-up resistor: (2)			0.6	V
Output high level voltage	$V_{OH}1$	I_{OH} = –3 mA: All output pins other than (3), (4) and XTAL	3.5			V
Output low level voltage	$V_{OL}1$	I_{OH} = 3 mA: All output pins other than (3), (4) and XTAL			0.4	V
Output high level voltage	$V_{OH}2$	I_{OH} = –6 mA: (3)	2.4			V
Output low level voltage	$V_{OL}2$	I_{OL} = 6 mA: (3)			0.4	V
Output low level voltage	$V_{OL}3$	I_{OL} = 3 mA, open drain, built-in pull-up resistor: (4)			0.4	V
Input leakage current	I_L	V_I = V_{SS}, V_{DD}: All input pins other than (2)	–25		+25	µA
Output leakage current	I_{OZ}	When in high impedance output mode: CDPORT0, CDPORT1, and D0 to D15	–100		+100	µA
Pull-up resistance	R_{UP}	(2), (4)	10	20	40	kΩ

Note: (1) WFCK, SBSO, SCOR, ZRESET, ZUDS, ZLDS, ZAS, R/W, ZACK0, ZACK1, ZRD, ZWR, ZCS
(2) SD0 to 7, IO0 to 7, ERA, ZDONE
(3) ZDTACK, D0 to 15
(4) ZINT, ZDONE, ZHINT0, ZHINT1

Pin Assignment

Type: I: Input pin, O: Output pin, B: Bi-directional pin, P: Power supply pin

Pin No.	Pin	Type	Function
1	V_{DD}	P	
2	MSTEMON	O	Audio block monitor
3	MEMPHAS	O	
4	MBITSPL	O	
5	MSPLFRQ	O	
6	OLRCK	O	D/A converter output
7	ODATA	O	
8	OBCLK	O	
9	SOC1	O	Output corresponding to the LC78835 or LC78835M
10	DACCK	O	16.9344 MHz (level A or B) or 8.4672 MHz (level C) output
11	RA0	O	RAM address outputs
12	RA1	O	
13	RA2	O	
14	RA3	O	
15	RA4	O	
16	RA5	O	
17	V_{SS}	P	
18	RA6	O	RAM address outputs
19	RA7	O	
20	RA8	O	
21	RA9	O	
22	RA10	O	
23	RA11	O	
24	RA12	O	
25	ADPCLK	I	AD PCM block clock input

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Type: I: Input pin, O: Output pin, B: Bi-directional pin, P: Power supply pin

Pin No.	Pin	Type	Function
26	RA13	O	RAM address outputs
27	RA14	O	
28	RA15	O	
29	ZRWE	O	RAM write enable
30	ZROE	O	RAM read enable
31	IO0	B	Data buffer RAM data I/O
32	IO1	B	
33	V_{SS}	P	
34	IO2	B	Data buffer RAM data I/O
35	IO3	B	
36	IO4	B	
37	IO5	B	
38	IO6	B	
39	IO7	B	
40	ERA	B	Data buffer RAM erasure flag I/O
41	EXTAL	I	Crystal oscillator connection
42	XTAL	O	
43	TEST0	I	Test pins: Normally tied low
44	TEST1	I	
45	TEST2	I	
46	MCK	O	CD-DSP connection
47	LRCK	I	
48	SDATA	I	
49	V_{DD}	P	
50	BCK	I	CD-DSP connection
51	C2PO	I	
52	WFCK	I	Subcode I/O
53	EXCK	O	
54	SBSO	I	
55	SCOR	I	
56	CEMPHAS	I	Connects to the CD-DSP EMPHASIS pin
57	SD0	B	Sub-CPU data signal pins: Built-in pull-up resistors
58	SD1	B	
59	SD2	B	
60	SD3	B	
61	SD4	B	
62	SD5	B	
63	SD6	B	
64	SD7	B	
65	V_{DD}	P	
66	ZRESET	I	Reset pin: Hold low for at least 1 μs
67	SCPUCNT	I	Sub-CPU I/F selection
68	SUA0	I	Sub-CPU register selection address
69	SUA1	I	
70	SUA2	I	
71	SUA3	I	
72	SUA4	I	
73	SUA5	I	
74	ZSWAIT	O	Sub-CPU wait signal
75	ZINT	O	Sub-CPU interrupt signal
76	RS (ALE)	I	Internal register set
77	ZRD	I	Sub-CPU read
78	ZWR	I	Sub-CPU write
79	ZCS	I	Sub-CPU chip select
80	D0	B	Host CPU data bus

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Type: I: Input pin, O: Output pin, B: Bi-directional pin, P: Power supply pin

Pin No.	Pin	Type	Function
81	V_{SS}	P	
82	D1	B	Host CPU data bus
83	D2	B	
84	D3	B	
85	D4	B	
86	V_{SS}	P	
87	V_{DD}	P	
88	D5	B	Host CPU data bus
89	D6	B	
90	D7	B	
91	D8	B	
92	V_{SS}	P	
93	D9	B	Host CPU data bus
94	D10	B	
95	D11	B	
96	D12	B	
97	V_{SS}	P	
98	D13	B	Host CPU data bus
99	D14	B	
100	D15	B	
101	ZHINT0	O	Host CPU interrupt
102	ZUDS	I	High-order data strobe input
103	ZLDS	I	Low-order data strobe input
104	ZAS	I	Address strobe signal
105	ZCSCDIC	I	Chip select from the host CPU
106	A1	I	Host CPU address
107	A2	I	
108	A3	I	
109	A4	I	
110	A5	I	
111	R/W	I	Read/write input
112	ZDTACK	B	Data acknowledge signal
113	V_{DD}	P	
114	CPUCLK	I	CPU clock input
115	CDPORT0	B	General-purpose I/O signals
116	CDPORT1	B	
117	ZHINT1	O	Host CPU interrupt
118	ZDONE	B	DMA transfer pin: Open drain with built-in pull-up resistors
119	ZACK0	I	For DMA transfer pins
120	ZACK1	I	
121	ZRDY0	O	
122	ZRDY1	O	
123	ZDRQ0	O	
124	ZDRQ1	O	
125	BUFFULL	O	SRAM status
126	DATAEMP	O	
127	UNDFLOW	O	
128	INIT	I	Gain control register initialization input