



STK400-090

AF Power Amplifier (Split Power Supply) (50W+50W+50W min, THD = 0.4%)

Overview

The STK400-090 is a thick-film audio power amplifier IC belonging to a series in which all devices are pin compatible. This allows a single PCB design to be used to construct amplifiers of various output capacity simply by changing hybrid ICs. Also, this series is part of a new, larger series that comprises mutually similar devices with the same pin compatibility. This makes possible the development of a 2-channel amplifier from a 3-channel amplifier using the same PCB. In addition, this new series features $6/3\Omega$ drive in order to support the low impedance of modern speakers.

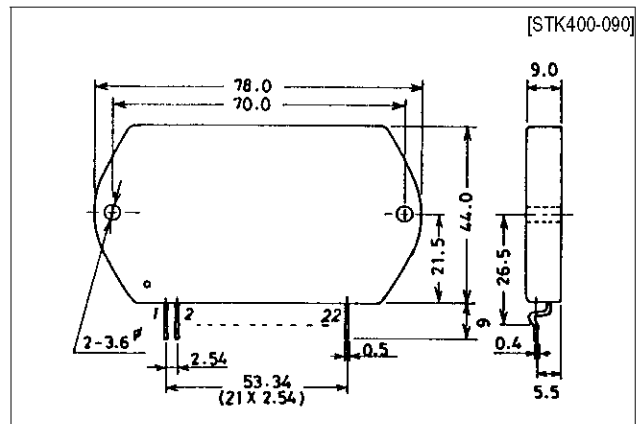
Features

- Pin compatible
STK400-000 series (3-channel/single package)
↓
STK401-000 series (2-channel/single package)
- Output load impedance $R_L = 6/3\Omega$ supported
- New pin configuration
Pin configuration has been grouped into individual blocks of inputs, outputs and supply lines, minimizing the adverse effects of pattern layout on operating characteristics.
- Few external components
In comparison with existing series, external bootstrap resistors and capacitors can be eliminated.

Package Dimensions

unit: mm

4086A



Specifications

Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC \text{ max}}$		± 47	V
Thermal resistance	θ_{j-c}	Per power transistor	1.7	$^\circ\text{C/W}$
Junction temperature	T_j		150	$^\circ\text{C}$
Operating substrate temperature	T_c		125	$^\circ\text{C}$
Storage temperature	T_{stg}		-30 to $+125$	$^\circ\text{C}$
Available time for load short-circuit	t_s	$V_{CC} = \pm 32\text{V}$, $R_L = 6\Omega$, $f = 50\text{Hz}$, $P_O = 50\text{W}$	1	s

Operating Characteristics at $T_a = 25^\circ\text{C}$, $R_L = 6\Omega$ (noninductive load), $R_g = 600\Omega$, $V_G = 40\text{dB}$

Parameter	Symbol	Conditions	min	typ	max	Unit
Quiescent current	I_{CCO}	$V_{CC} = \pm 39\text{V}$	30	90	150	mA
Output power	$P_{O(1)}$	$V_{CC} = \pm 32\text{V}$, $f = 20\text{Hz}$ to 20kHz , $\text{THD} = 0.4\%$	50	55	-	W
	$P_{O(2)}$	$V_{CC} = \pm 26\text{V}$, $f = 1\text{kHz}$, $\text{THD} = 1.0\%$, $R_L = 3\Omega$	50	55	-	W
Total harmonic distortion	THD(1)	$V_{CC} = \pm 32\text{V}$, $f = 20\text{Hz}$ to 20kHz , $P_O = 1.0\text{W}$	-	-	0.4	%
	THD(2)	$V_{CC} = \pm 32\text{V}$, $f = 1\text{kHz}$, $P_O = 5.0\text{W}$	-	0.01	-	%
Frequency response	f_L, f_H	$V_{CC} = \pm 32\text{V}$, $P_O = 1.0\text{W}$, $^{+0}_{-3}\text{dB}$	-	20 to 50k	-	Hz
Input impedance	r_i	$V_{CC} = \pm 32\text{V}$, $f = 1\text{kHz}$, $P_O = 1.0\text{W}$	-	55	-	$k\Omega$
Output noise voltage	V_{NO}	$V_{CC} = \pm 39\text{V}$, $R_g = 10k\Omega$	-	-	1.2	mVrms
Neutral voltage	V_N	$V_{CC} = \pm 39\text{V}$	-70	0	+70	mV

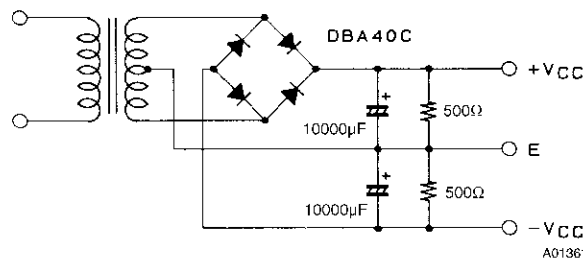
Notes.

All tests are measured using a constant-voltage supply unless otherwise specified.

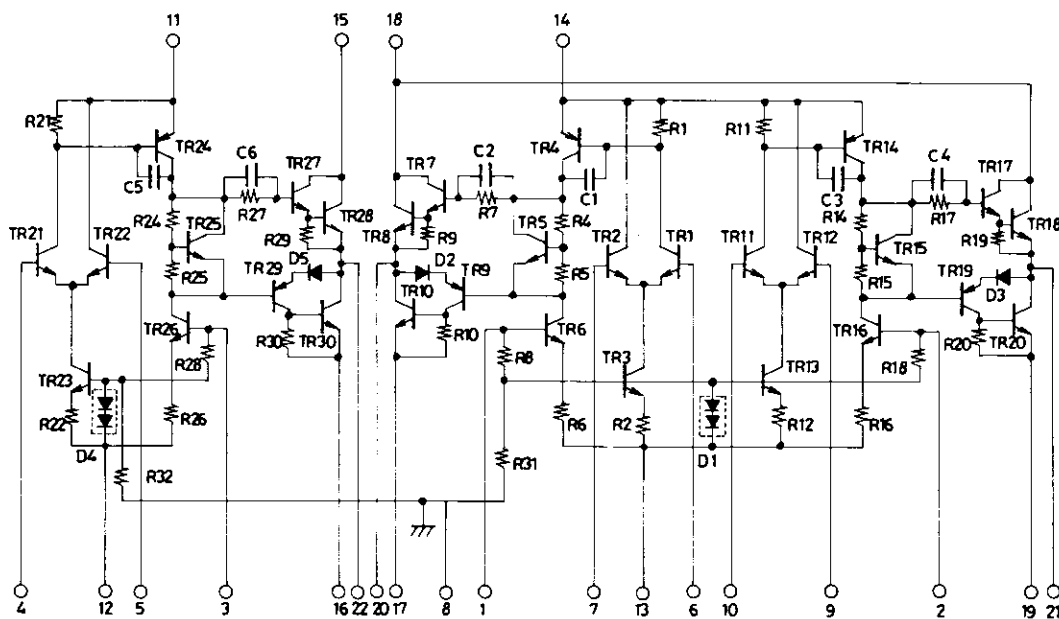
Available time for load short-circuit and output noise voltage are measured using the transformer supply specified below.

The output noise voltage is the peak value of an average-reading meter with an rms value scale (VTVM). A regulated AC supply (50Hz) should be used to eliminate the effects of AC primary line flicker noise.

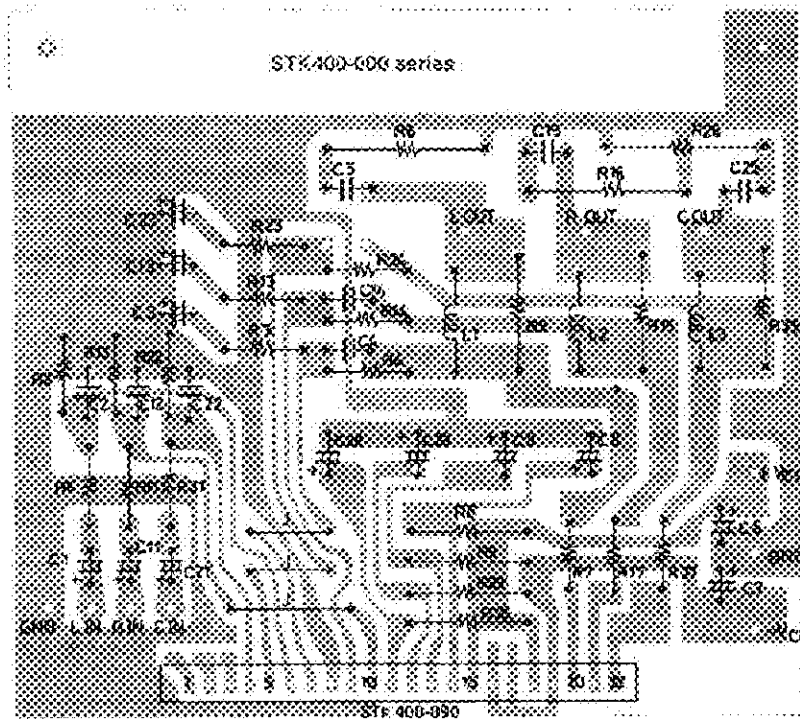
Specified Transformer Supply (MG-200 or Equivalent)



Equivalent Circuit

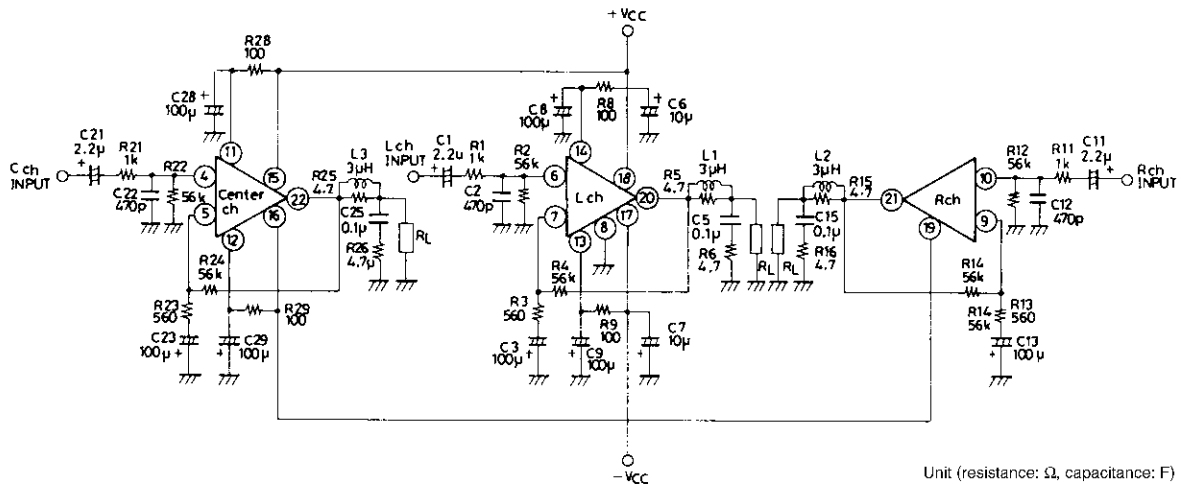


Sample PCB Layout for 2-Channel or 3-Channel Amplifiers



Copper (Cu) foil surface
 Pin 1 of STK401-000 series devices corresponds to pin 6 of STK400-000 series devices.

Sample Application Circuit



External Component Description

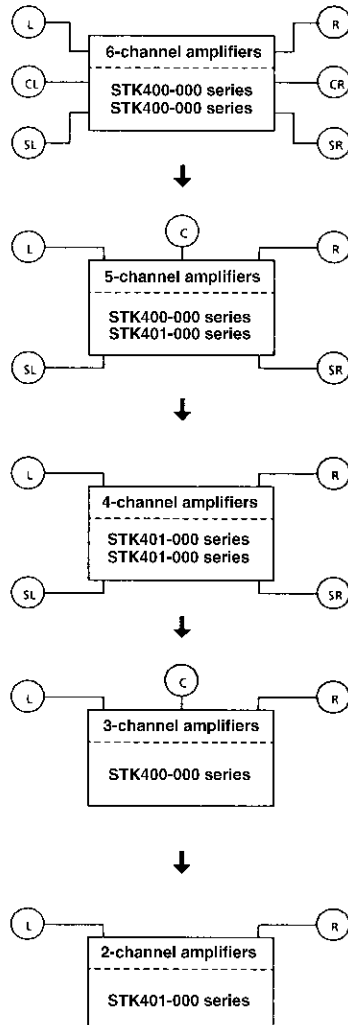
C1, C11, C21	<p>Input coupling capacitors. For DC blocking. Since capacitor reactance becomes larger at lower frequencies, the output noise can be adversely affected by signal source resistance-dependent 1/f noise. In this case, a lower reactance value should be chosen. In order to remove pop noise at power-on, larger values of capacitance should be chosen for C1 and C11, which determine the input time constant, and smaller values for C3, C13 and C23 in the NF circuit.</p>
C2, C12, C22	<p>Input filter capacitors. These, together with R1, R11 and R21, form filters to reduce high-frequency noise.</p>
C3, C13, C23	<p>NF capacitors. These determine the low-side cut-off frequency.</p> $f_L = \frac{1}{2\pi \times C3(C13, C23) \times R3(R13, R23)}$ <p>Large values should be chosen for C3, C13 and C23 to maintain voltage gain at low frequencies. However, because this would tend to increase the shock noise at power-on, values larger than absolutely necessary should be avoided.</p>
C5, C15, C25	<p>Oscillation prevention capacitors. Mylar capacitors are recommended for their excellent thermal and frequency characteristics.</p>
C6, C7	<p>Oscillation prevention capacitors. These should be inserted as close as possible to the IC supply pins to reduce supply impedance and hence provide stable IC operation. Electrolytic capacitors are recommended.</p>
C8, C9, C28, C29	<p>Decoupling capacitors. These, together with R8, R9, R28 and R29, form time constant circuits that remove shock noise and ripple voltage from the supply, preventing any noise being coupled to the inputs.</p>
R1, R11, R21	<p>Input filter resistors.</p>
R2, R12, R22	<p>Input bias resistors. These are used to bias the input pins at zero potential. The input impedance is largely determined by this resistance.</p>
R3, R13, R23 R4, R14, R24	<p>Voltage-gain VG setting resistors. VG = 40dB is recommended using R3, R13, R23 = 560Ω, and R4, R14, R24 = 56kΩ. Gain adjustments are best made using R3, R13 and R23. If gain adjustments are made using R4, R14 and R24, then set R2, R12, R22 = R4, R14, R24 to maintain V_N balance stability.</p>
R5, R15, R25	<p>Oscillation prevention resistors.</p>
R6, R16, R26	<p>Oscillation prevention resistors. The power dissipated in these resistors is dependent on the frequency, as given below.</p> $P_{R6(R16, R26)} = \left(\frac{V_{CC \max} / \sqrt{2}}{1 / 2\pi f \times C5(C15, C25) + R6(R16, R26)} \right)^2 \times R6(R16, R26)$ <p>where f is the output signal frequency upper limit.</p>
R8, R9, R28, R29	<p>Ripple filter resistors. P_O max, ripple rejection and supply power-on shock noise are all affected by this resistance. These resistors should be chosen taking into consideration both the function they perform as predriver transistor limiting resistors during load short circuits and the peak current that flows through them when charging C8, C9, C28 and C29.</p>
L1, L2, L3	<p>Oscillation prevention coils. These correct the phase difference caused by capacitive loads and increase stability against oscillation.</p>

Series Configuration

3-channel amplifier type Nos.	Rated output	2-channel amplifier type Nos.	Rated output	THD [%] f = 20Hz to 20kHz	Supply voltage [V] ¹			
					V _{CC max1}	V _{CC max2}	V _{CC1}	V _{CC2}
STK400-010	10W × 3	STK401-010	10W × 2	0.4	-	±26	±17	±14
STK400-020	15W × 3	STK401-020	15W × 2		-	±29	±20	±16
STK400-030	20W × 3	STK401-030	20W × 2		-	±34	±23	±19
STK400-040	25W × 3	STK401-040	25W × 2		-	±36	±25	±21
STK400-050	30W × 3	STK401-050	30W × 2		-	±39	±26	±22
STK400-060	35W × 3	STK401-060	35W × 2		-	±41	±28	±23
STK400-070	40W × 3	STK401-070	40W × 2		-	±44	±30	±24
STK400-080	45W × 3	STK401-080	45W × 2		-	±45	±31	±25
STK400-090	50W × 3	STK401-090	50W × 2		-	±47	±32	±26
STK400-100	60W × 3	STK401-100	60W × 2		-	±51	±35	±27
STK400-110	70W × 3	STK401-110	70W × 2		±56.0	-	±38	-
-	-	STK401-120	80W × 2		±61.0	-	±42	-
-	-	STK401-130	100W × 2		±65.0	-	±45	-
-	-	STK401-140	120W × 2		±74.0	-	±51	-

1. V_{CC max1} (R_L = 6Ω), V_{CC max2} (R_L = 3 to 6Ω), V_{CC1} (R_L = 6Ω), V_{CC2} (R_L = 3Ω)

Sample Designs using a Common PCB



Similarly, when STK400-090 $V_{CC} = \pm 26V$ and $R_L = 3\Omega$, from Figure 2:

$$P_d = 76W \text{ (for } 1/10 P_{O \text{ max}} = 5W)$$

$$\text{From expression (1)'}: \theta_{c-a} < (125 - 50)/76 < 0.98$$

$$\text{From expression (2)'}: \theta_{c-a} < (150 - 50)/76 - 1.7/6 < 1.03$$

Therefore, to satisfy both expressions, the required heat-sink must have a thermal resistance less than $0.98^\circ C/W$.

This heatsink design example is based on a constant-voltage supply, and should be verified within your specific set environment.

Figure 1. $P_d - P_O$

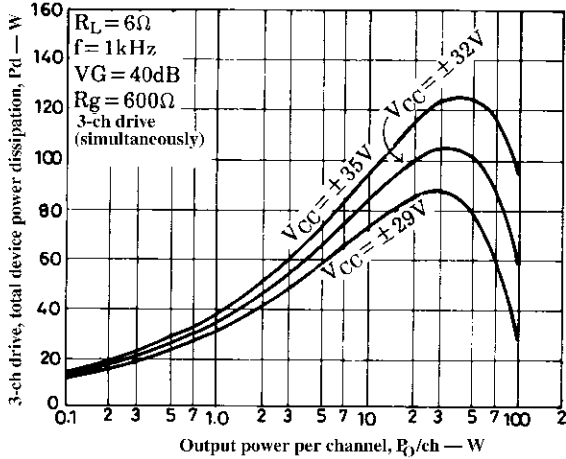
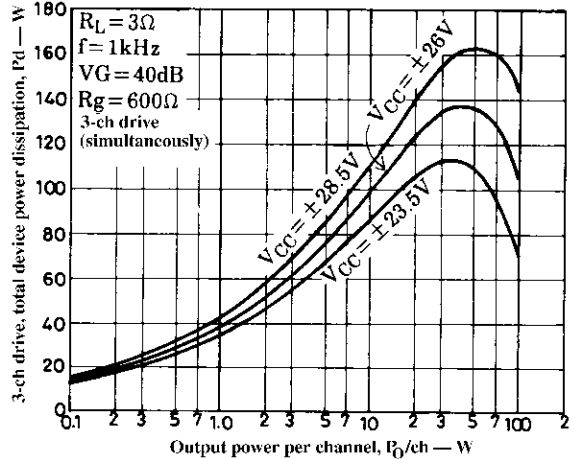
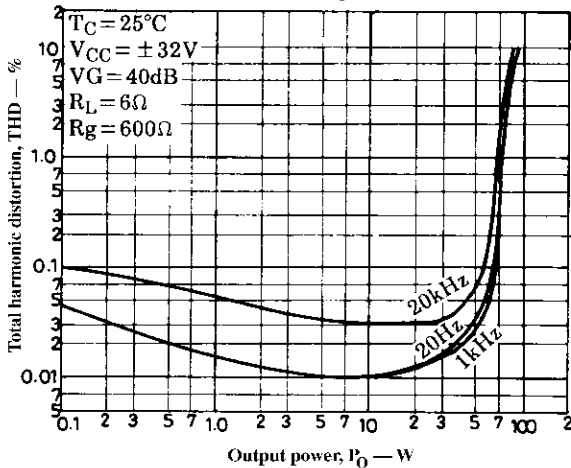


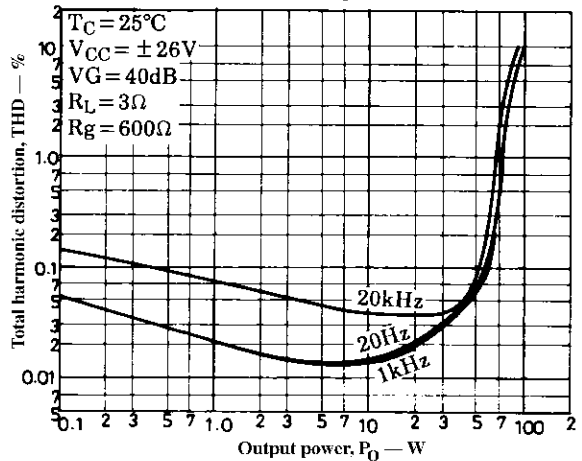
Figure 2. $P_d - P_O$



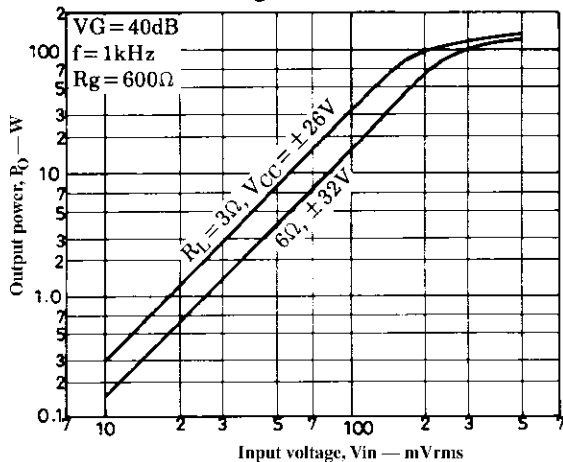
THD - P_O



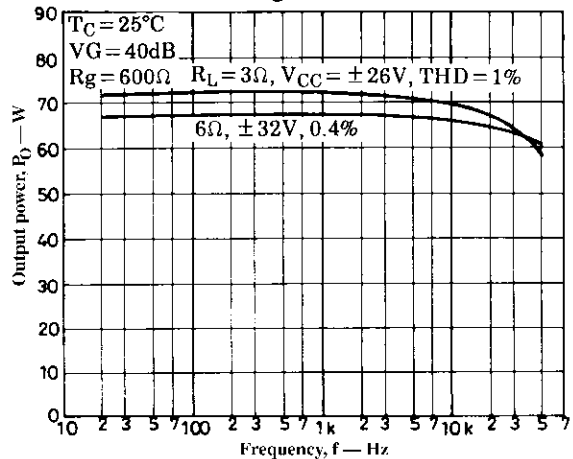
THD - P_O

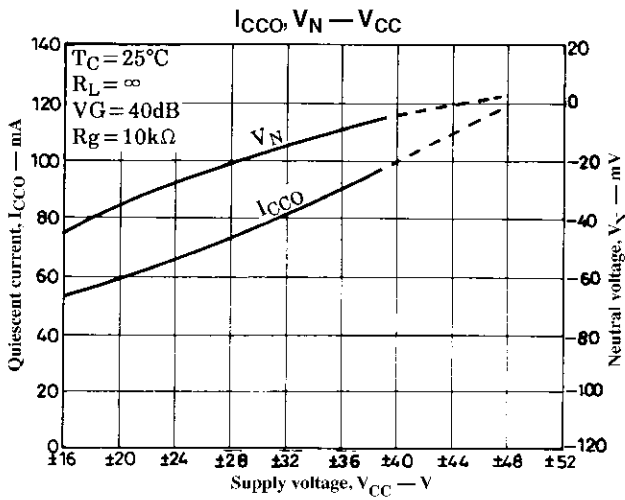
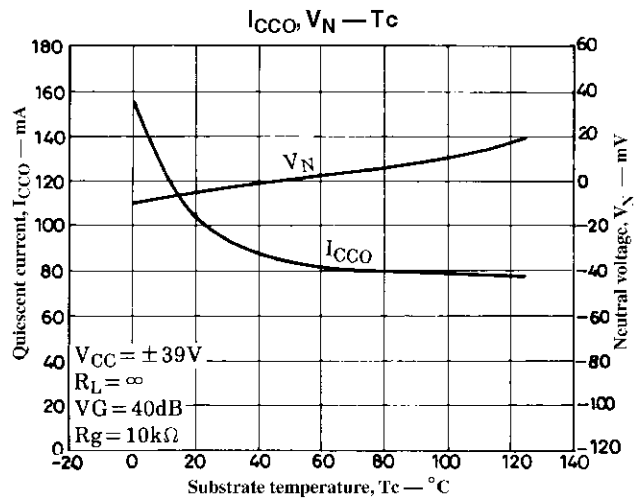
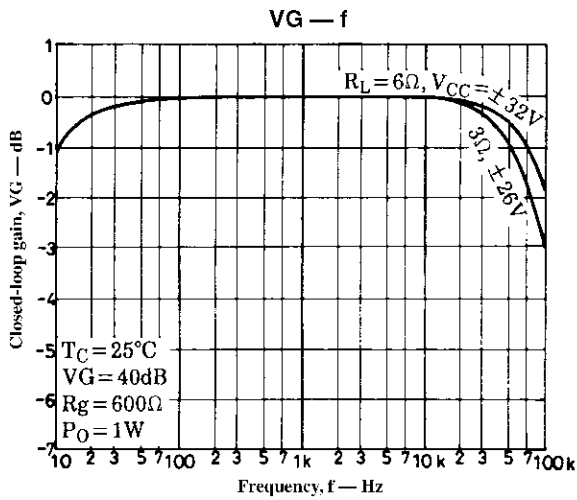
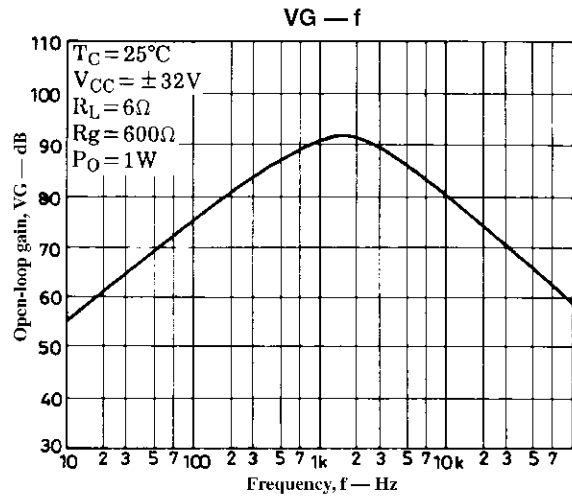
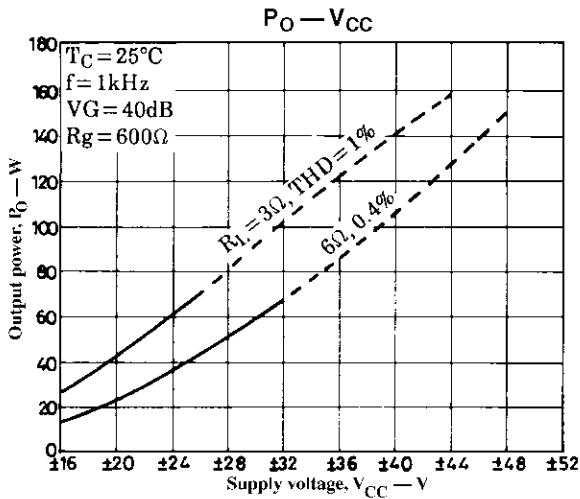


$P_O - V_{in}$



$P_O - f$





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