Ordering number: EN2778C

CMOS LSI

LC7930N, 7930NW

LCD Drivers

Overview

The LC7930N, 7930NW are CMOS LSIs which incorporate 20-bit shift register, latch, and two sets of 20 LCD drivers. They also have two switching pins: one of them (channel 2) can be used as a scan-line driver (back plate) and the other (channel 1) as a segment driver. They are optimal for LCD interface with microcontroller (4 or 8 bits) or dot matrix controller circuit incorporating character generator.

Features

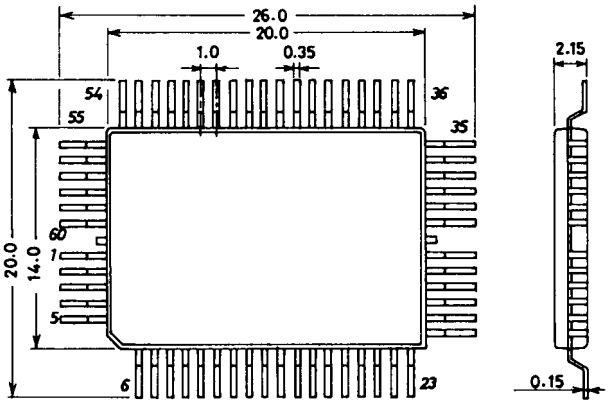
- Two channels of 20 output segment drivers
- The configuration of 20 output segment drivers + 20 scanning terminal drivers available
- A series data to connect with the microcontroller and three control signals
- Able to be connected in series for large display
- Built-in bidirectional shift register can be shifted in the direction that makes wiring easy
- Operating supply voltage/ Operating temperature: V_{DD} = 4.5 to 5.5 V / Topr = –20 to +75°C
- Operating current drain : I_{DD} = 1.0 mA max (Logic = 400 kHz, LCD = 1 kHz)
- Package : Pin 60 Flat LC7930N : QIP60
  Pin 64 Flat LC7930NW : SQFP64

Package Dimensions

unit : mm

3055A-QFP60C

[LC7930N]

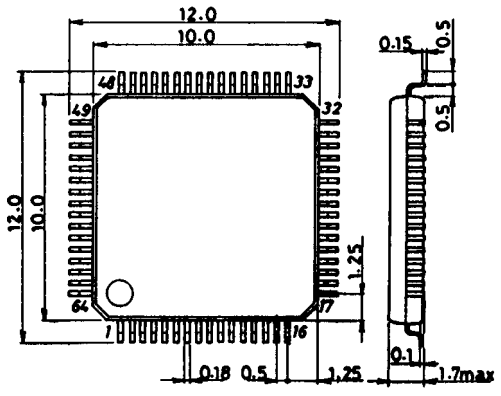


SANYO : QIP60C

unit : mm

3190-SQFP64

[LC7930NW]



SANYO : SQFP64

Specifications

Absolute Maximum Ratings at Ta = 25 ± 2°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		–0.3 to +7.0	V
	V_{EE} max		V_{DD}–13.5 to V_{DD}+0.3	V
Maximum input voltage	V_I max		–0.3 to V_{DD}+0.3	V
		V1, V2, V3, V4, V5, V6	V_{EE} to V_{DD}+0.3	V
Maximum output voltage	V_O max		–0.3 to V_{DD}+0.3	V
		Output transistor OFF, Y1 to Y40	V_{EE} to V_{DD}+0.3	V
Allowable power dissipation	Pd max		100	mW
Operating temperature	Topr		–20 to +75	°C
Storage temperature	Tstg		–55 to +125	°C

Note : Don't soak the whole of IC into the tank filled with melted solder for soldering

Allowable Operating Conditions at Ta = –20 to +75°C, V_{SS} = 0 V, V_{EE} = –4 to –6 V

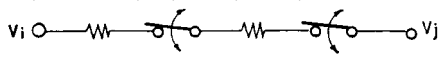
Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}	V_{DD}	4.5		5.5	V
High-level input voltage	V_{IH}	Note (1)	0.7V_{DD}		V_{DD}	V
Low-level input voltage	V_{IL}	Note (1)	V_{SS}		0.3V_{DD}	V
Shift frequency	f_{CL}	CLK_{SR}			400	kHz
High-level clock width	t_{CWH}	CLK_{SR}, CLK_{LA}	800			ns
Low-level clock width	t_{CWL}	CLK_{SR}	800			ns
Data setup time	t_{SU}	LDATA1, LDATA2, RDATA1, RDATA2	300			ns
Clock setup time	t_{SL}	CLK_{SR}, CLK_{LA} $CLK_{SR} \rightarrow CLK_{LA}$	500			ns
	t_{LS}	CLK_{SR}, CLK_{LA} $CLK_{LA} \rightarrow CLK_{SR}$	500			ns
Clock transition time	t_{ct}	CLK_{SR}, CLK_{LA}			200	ns
Data retention time	t_{DH}	LDATA1, LDATA2, RDATA1, RDATA2	300			ns

Electirical Characteristics at Ta = –20 to +75°C, V_{DD} = +5 V ± 10%, V_{SS} = 0 V, V_{EE} = –4 to –6 V

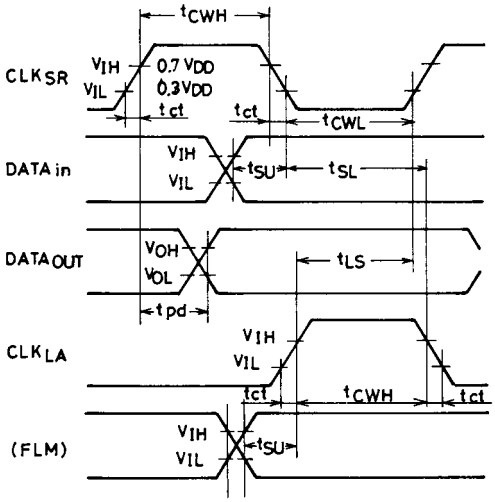
Parameter	Symbol	Conditions		min	typ	max	Unit
Input leakage current	I_{IH}	Note (1)	Vin = V_{DD}			5	µA
	I_{IL}	Note (1)	Vin = V_{SS}	–5			µA
High-level output voltage	V_{OH}	LDATA1, LDATA2, RDATA1, RDATA2	I_{OH} = –0.4 mA	V_{DD}–0.4			V
Low-level output voltage	V_{OL}	LDATA1, LDATA2, RDATA1, RDATA2	I_{OL} = 0.4 mA			0.4	V
Vi to Yj voltage down	V_{d1}	Y1 to Y40 Note (2)	Ion = 100 µA, single output			1.1	V
	V_{d2}	Y1 to Y40 Note (2)	Ion = 50 µA, all outputs			1.5	V
Vi quiescent current	I_{VH}	V1 to V6	Open output pins Vin = V_{DD}			10	µA
	I_{VL}	V1 to V6	Open output pins Vin = V_{EE}	–10			µA
Supply current	I_{DD}	V_{DD}	Open output pins CLK_{SR} = 400 kHz			1.0	mA
	I_{EE}	V_{EE}	Open output pins M = 1 kHz			10	µA
Output propagation delay time	t_{PD}	LDATA1, LDATA2, RDATA1, RDATA2	C_L = 15 pF			500	ns

Note (1): Applied to the pins; CLK_{SR}, CLK_{LA}, LDATA1, RDATA1, LDATA2, RDATA2, M, L/R1, L/R2, CH2-BP

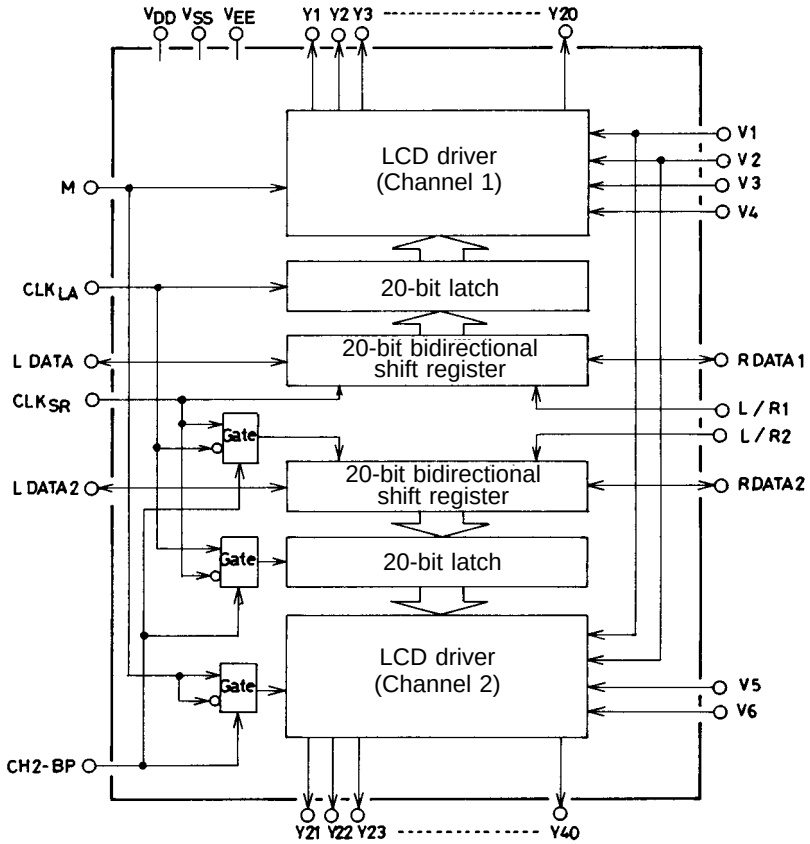
(2): The equivalent circuit between Vi to Yj (i = 1 to 6, j = 1 to 40)



Switching Waveforms



Internal Equivalent Circuit



Pin Assignment

[LC7930N]

Number	Name	Input/Output	Number	Name	Input/Output	Number	Name	Input/Output
1	Y30	Output	21	Y14	Output	41	RDATA1	Input/Output
2	Y31	Output	22	Y13	Output	42	LDATA2	Input/Output
3	Y32	Output	23	Y12	Output	43	RDATA2	Input/Output
4	Y33	Output	24	Y9	Output	44	N.C.	—
5	Y34	Output	25	Y10	Output	45	M	Input
6	Y29	Output	26	Y11	Output	46	L/R1	Input
7	Y28	Output	27	Y8	Output	47	L/R2	Input
8	Y27	Output	28	Y7	Output	48	CH2-BP	Input
9	Y26	Output	29	V_{DD}	—	49	V1	Input
10	Y25	Output	30	Y6	Output	50	V2	Input
11	Y24	Output	31	Y5	Output	51	V3	Input
12	Y23	Output	32	Y4	Output	52	V4	Input
13	Y22	Output	33	Y3	Output	53	V5	Input
14	Y21	Output	34	Y2	Output	54	V6	Input
15	Y20	Output	35	Y1	Output	55	Y40	Output
16	Y19	Output	36	V_{EE}	—	56	Y39	Output
17	Y18	Output	37	CLK_{LA}	Input	57	Y38	Output
18	Y17	Output	38	CLK_{SR}	Input	58	Y37	Output
19	Y16	Output	39	V_{SS}	—	59	Y36	Output
20	Y15	Output	40	LDATA1	Input/Output	60	Y35	Output

[LC7930NW]

Number	Name	Input/Output	Number	Name	Input/Output	Number	Name	Input/Output
1	V5	Input	23	Y6	Output	45	Y26	Output
2	V4	Input	24	V_{DD}	—	46	Y27	Output
3	V3	Input	25	Y7	Output	47	Y28	Output
4	V2	Input	26	Y8	Output	48	Y29	Output
5	V1	Input	27	Y11	Output	49	N.C.	—
6	CH2-BP	Input	28	Y10	Output	50	Y34	Output
7	L/R2	Input	29	Y9	Output	51	Y33	Output
8	L/R1	Input	30	Y12	Output	52	Y32	Output
9	M	Input	31	Y13	Output	53	Y31	Output
10	RDATA2	Input/Output	32	N.C.	—	54	Y30	Output
11	LDATA2	Input/OUtput	33	Y14	Output	55	N.C.	—
12	RDATA1	Input/Output	34	Y15	Output	56	N.C.	—
13	LDATA1	Input/Output	35	Y16	Output	57	Y35	Output
14	V_{SS}	—	36	Y17	Output	58	Y36	Output
15	CLK_{SR}	Input	37	Y18	Output	59	Y37	Output
16	CLK_{LA}	Input	38	Y19	Output	60	Y38	Output
17	V_{EE}	—	39	Y20	Output	61	Y39	Output
18	Y1	Output	40	Y21	Output	62	Y40	Output
19	Y2	Output	41	Y22	Output	63	V6	Input
20	Y3	Output	42	Y23	Output	64	N.C.	—
21	Y4	Output	43	Y24	Output			
22	Y5	Output	44	Y25	Output			

Pin Descriptions

<table>
<tr><th>Pin Name</th><th>Function</th></tr>
<tr><td>V_{DD}
V_{SS}
V_{EE}</td><td>Logic circuitry power supply (+5 V ±10%)
0 V
LCD driver power supply (–4 to –6 V)</td></tr>
<tr><td>Y1 to Y20
Y21 to Y40</td><td>Channel 1 LCD driver output pins
Channel 2 LCD driver output pins</td></tr>
<tr><td>V1, V2
V3, V4
V5, V6</td><td>Reference voltage for selected driver outputs
Reference voltage for non-selected driver outputs (channel 1)
Reference voltage for non-selected driver outputs (channel 2)</td></tr>
<tr><td>L/R1</td><td>Shift direction for channel 1 shift register
<table>
<tr><th>L/R1</th><th>LDATA1</th><th>RDATA1</th></tr>
<tr><td>High-level</td><td>Output</td><td>Input</td></tr>
<tr><td>Low-level</td><td>Input</td><td>Output</td></tr>
</table></td></tr>
<tr><td>L/R2</td><td>Shift direction for channel 2 shift register
<table>
<tr><th>L/R2</th><th>LDATA2</th><th>RDATA2</th></tr>
<tr><td>High-level</td><td>Output</td><td>Input</td></tr>
<tr><td>Low-level</td><td>Input</td><td>Output</td></tr>
</table></td></tr>
<tr><td>LDATA1
RDATA1</td><td>Serial data input/output pins for channel 1 shift register</td></tr>
<tr><td>LDATA2
RDATA2</td><td>Serial data input/output pins for channel 2 shift register</td></tr>
<tr><td>M</td><td>Switching clock signal for LCD driver.</td></tr>
<tr><td>CLK_{LA}</td><td>Latches channael 1 data on the falling edge.
This also will latch channel 2 data on the falling edge if CH2-BP is low.</td></tr>
<tr><td>CLK_{SR}</td><td>Shift channel 1 data on the falling edge.
This also will shift channel 2 data on the falling edge if CH2-BP is low.</td></tr>
<tr><td>CH2-BP</td><td>Switches the mode of channel 2.
Exchanges the latch signal for the shift signal of channel 2 and invert the M signal.
Channel 2, then, can be used as a scan-line driver.
<table>
<tr><th rowspan="2">CH2-BP</th><th colspan="2">Channel 2</th><th rowspan="2">M</th><th rowspan="2"></th></tr>
<tr><th>Latch</th><th>Shift</th></tr>
<tr><td>High</td><td>CLK_{SR} ↑</td><td>CLK_{LA} ↑</td><td>$\overline{M}$</td><td>For scan-line driver</td></tr>
<tr><td>Low</td><td>CLK_{LA} ↓</td><td>CLK_{SR} ↓</td><td>M</td><td>For signal line driver</td></tr>
</table></td></tr>
</table>

Functional Description

LC7930N, LC7930NW are serial data transfer type LCD drivers.
Data inputted serially from the data pin is shifted successively by the synchronizing clock (CLK_{SR}) and latched by the latch clock (CLK_{LA}) when the all data are shifted.

- Segment terminal
  When CH2-BP goes to low, the data of channel 1 and channel 2 are shifted at the falling edge of CLK_{SR}, and then latched at the falling edge of the CLK_{LA}. The reference pulse will be switched to selected or unselected due to the latched data.
- Scan terminal
  When CH2-BP goes to high, the data of channel 2 is shifted at the rising edge of CLK_{LA}, and then latched at the rising edge of the CLK_{SR}. When FLM signal, as a data, is inputted, the output will be scan terminal drive mode.

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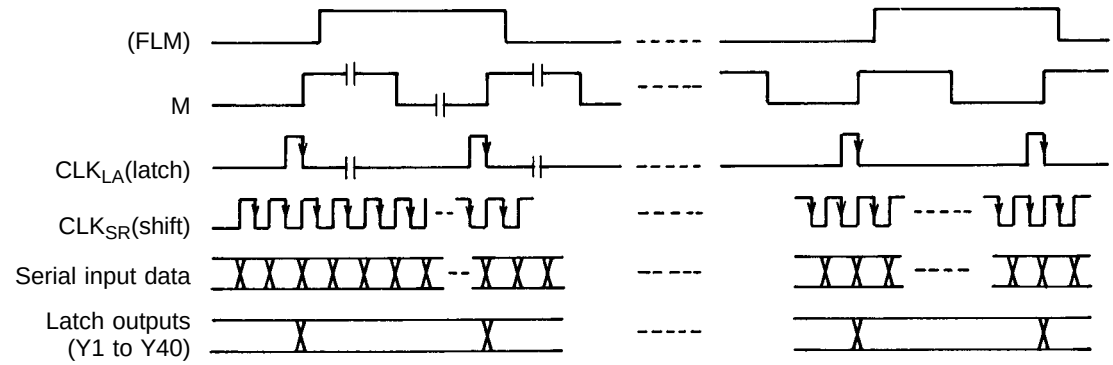
(1) Waveform Diagrams for Segment Drive Mode (CH2 – BP = "L")



(2) Waveform Diagrams for Scan-Line/Segment Drive Mode (CH2–BP = "H")

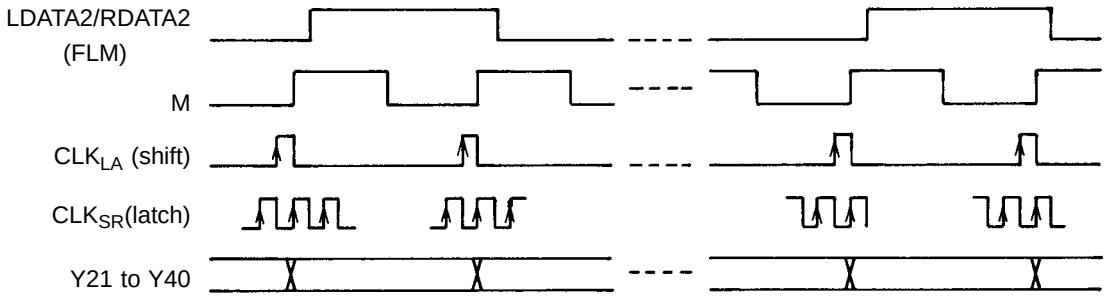


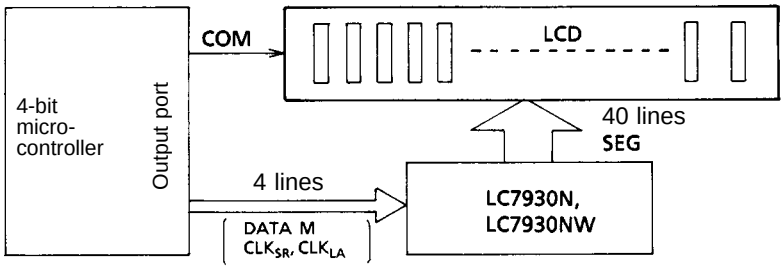
Table 1. LCD Driver Output Voltages (V1 to V6) for Y1 to Y40

CH2–BP	Serial Input Data	M	Output	
			Y1 to Y20	Y21 to Y40
High level (1)	1 (selected)	H	V1	V2
		L	V2	V1
	0 (un-selected)	H	V3	V6
		L	V4	V5
Low level (2)	1	H	V1	V1
		L	V2	V2
	0	H	V3	V5
		L	V4	V6

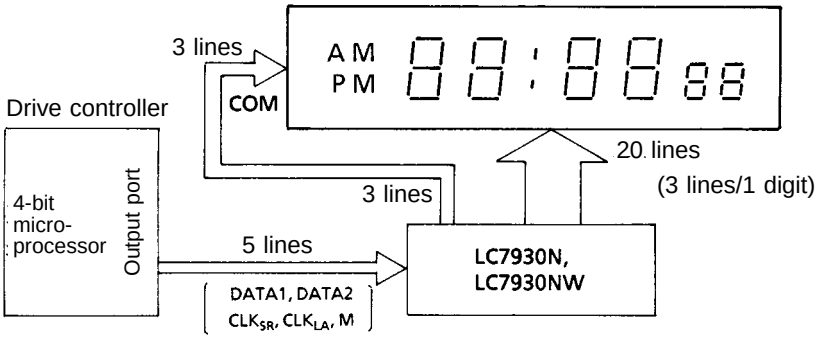
LCD Interface Examples

(Although the LCD divided voltage generator circuit is not shown here.)

(1) 40-segment bar-graph display (static)



(2) 6-digit, 7-segment + sign display. (1/3 duty cycle, 1/3 voltage bias)



(3) 20 × 60 pixel graphic display. (1/20 duty cycle, 1/5 voltage bias)