Ordering number : EN5280A

CMOS LSI

LC4101C

LCD Dot Matrix Segment Driver for STN Displays

Overview

The LC4101C is a segment driver for large-scale dot matrix LCD panels. It latches 240 bits of display data sent from the controller over a 4-bit or 8-bit parallel connection and generates the LCD drive signals. The LC4100C and LC4101C form a large-screen LCD panel driver chip set.

Features

- Fabricated in a CMOS (P-sub) high-voltage process.
- LCD drive voltage: 36 V
- Logic system power-supply voltage: 3.0 to 5.5 V
- f_{cp} max: 12 MHz (V_{DD} = 5 V ±10 %), 6.5 MHz (V_{DD} = 3 to 4.5 V)
- 240 outputs
- Parallel input switchable between 4 and 8 bits
- DISPOFF function that locks the drive voltages output to the LCD at fixed levels.
- Display duty: 1/160 to 1/480

Specifications

Absolute Maximum Ratings at Ta = 25°C ± 2°C, standard V_{SS}, $V_{EEn} = V_{EE1}$ or V_{EE2}, $V_{SSn} = V_{SS1}$ or V_{SS2}

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		–0.3 to +7	V
	V_{EEn}		–0.3 to +40	V
	V_{SSn}		–0.3 to +0.3	V
Input voltage	V_{IN}	D0 to D7, LOAD, CP, L/R, BS, TEST, DISP, DF, EIO1, EIO2	–0.3 to V_{DD} + 0.3	V
	V_0, V_2	V_0, V_2	V_{EEn} – 7 to V_{EEn} + 0.3	V
	V_3	V_3	–0.3 to V_{SSn} + 7	V
	V_5	V_5	–0.3 to +0.3	V
Operating temperature	Topr		–20 to +75	°C
Storage temperature	Tstg		–55 to +125	°C

Note: The voltages V_0, V_2, V_3, and V_5 must obey the relationships $V_{EEn} \geq V_0 \geq V_2 \geq V_{EE} - 7$, and $7 \geq V_3 \geq V_5 \geq V_{SSn}$. (Unit: V)

Allowable Operating Ranges at Ta = –20 to +75°C, standard V_{SS}, $V_{EEn} = V_{EE1}$ or V_{EE2}, $V_{SSn} = V_{SS1}$ or V_{SS2}

Parameter		Symbol	Conditions	min	typ	max	Unit
Supply voltage		V_{DD}		3.0		5.5	V
		V_{EEn}		20		36	V
		V_{SSn}			0		V
Input high-level voltage		V_{IH}	D0 to D7, CP, L/R, BS, DF, TEST, DISP, EIO1, EIO2, LOAD	0.8 V_{DD}		V_{DD}	V
Input low-level voltage		V_{IL}	D0 to D7, CP, L/R, BS, DF, TEST, DISP, EIO1, EIO2, LOAD	0		0.2 V_{DD}	V
Input voltage		V_0, V_2	V_0, V_2	V_{EEn} – 7		V_{EEn}	V
		V_3	V_3	0		V_{SSn} + 7	V
		V_5	V_5		0		V
V_{DD} = 5 V ± 10%	CP clock frequency	f_{cp}	CP			12	MHz
	High-level load pulse width	$t_{w\,(ldh)}$	LOAD	50			ns
	High-level clock pulse width	$t_{w\,(cph)}$	CP	28			ns
	Low-level clock pulse width	$t_{w\,(cpl)}$	CP	28			ns
	Load clock frequency	f_{load}	LOAD			1	MHz
	LOAD/CP setup time	$t_{su\,(ld)}$	LOAD, CP	30			ns
	LOAD/CP hold time	$t_{ho\,(ld)}$	LOAD, CP	200			ns
	DATA/CP setup time	$t_{su\,(cp)}$	CP, D0 to D7	28			ns
	DATA/CP hold time	$t_{ho\,(cp)}$	CP, D0 to D7	20			ns
	EIO input setup time	$t_{su\,(ei)}$	CP, EIO1, EIO2	30			ns
	Clock rise time	t_r	LOAD, CP			50	ns
	Clock fall time	t_f	LOAD, CP			50	ns
V_{DD} = 3 to 4.5 V	CP clock frequency	f_{cp}	CP			6.5	MHz
	High-level load pulse width	$t_{w\,(ldh)}$	LOAD	50			ns
	High-level clock pulse width	$t_{w\,(cph)}$	CP	40			ns
	Low-level clock pulse width	$t_{w\,(cpl)}$	CP	40			ns
	Load clock frequency	f_{load}	LOAD			200	kHz
	LOAD/CP setup time	$t_{su\,(ld)}$	LOAD, CP	35			ns
	LOAD/CP hold time	$t_{ho\,(ld)}$	LOAD, CP	350			ns
	DATA/CP setup time	$t_{su\,(cp)}$	CP, D0 to D7	50			ns
	DATA/CP hold time	$t_{ho\,(cp)}$	CP, D0 to D7	50			ns
	EIO input setup time	$t_{su\,(ei)}$	CP, EIO1, EIO2	45			ns
	Clock rise time	t_r	LOAD, CP			50	ns
	Clock fall time	t_f	LOAD, CP			50	ns

Note: 1. The voltages V_0, V_2, V_3, and V_5 must obey the relationships $V_{EEn} \geq V_0 \geq V_2 \geq V_{EE} - 7$, and $7 \geq V_3 \geq V_5 \geq V_{SSn}$. (Unit: V)

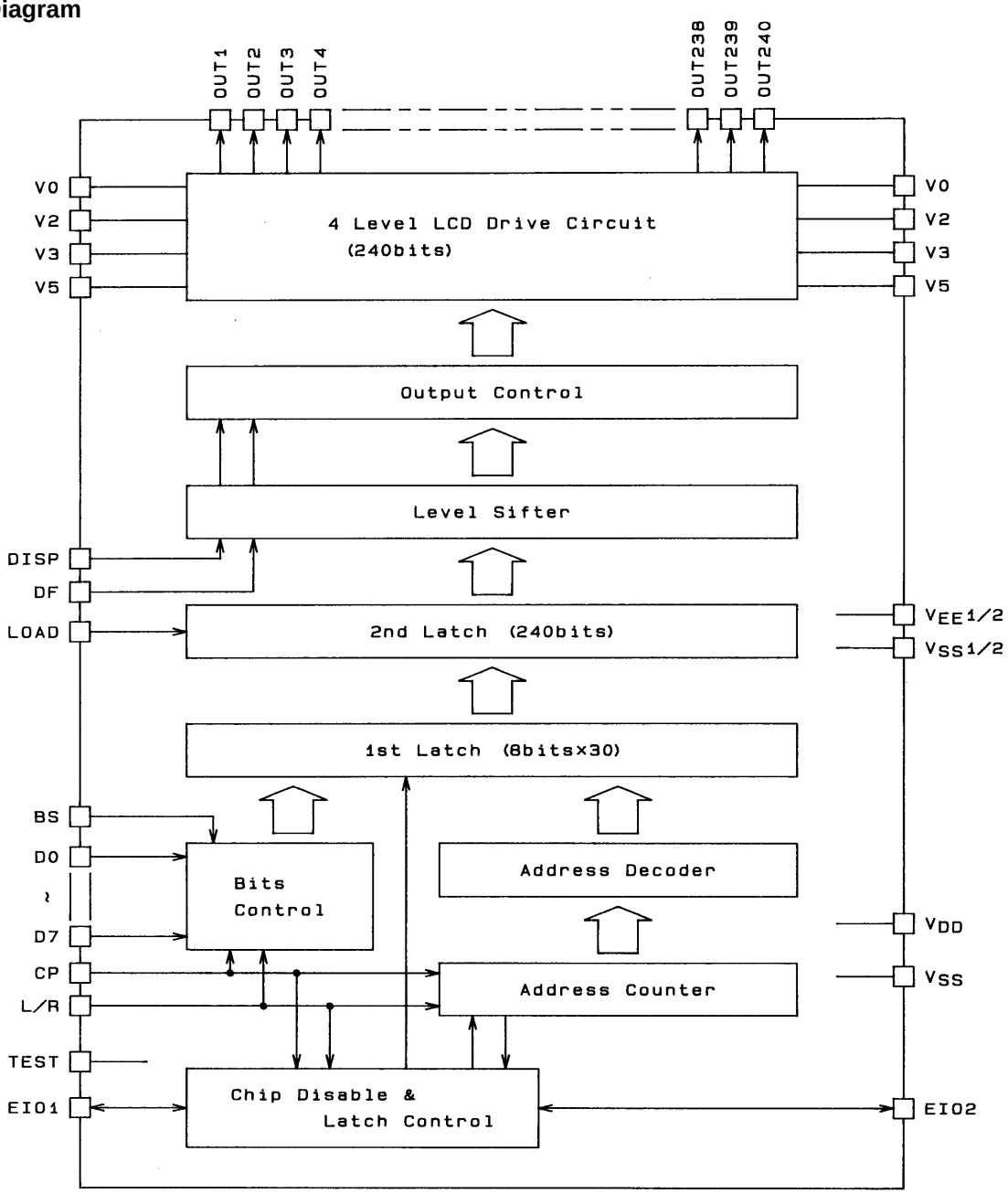
2. When turning on the power supplies, first turn on the logic system power supply and then turn on the high-voltage system power supply; alternatively, turn both on at the same time.
When turning off the power supplies, first turn off the high-voltage system power supply and then turn off the logic system power supply; alternatively, turn both off at the same time.

Electrical Characteristics at Ta = –20 to +75°C, standard V_{SS}, V_{DD} = 3 to 5.5 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Input high-level current	I_{IH}	$V_{IN} = V_{DD}$: D0 to D7, CP, L/R, BS, DF, TEST, DISP, EIO1, EIO2, LOAD			1	µA
Input low-level current	I_{IL}	$V_{IN} = V_{SS}$: D0 to D7, CP, L/R, BS, DF, TEST, DISP, EIO1, EIO2, LOAD	–1			µA
Output high-level voltage	V_{OH}	I_O = –0.4 mA: EIO1, EIO2	0.8 V_{DD}		V_{DD}	V
Output low-level voltage	V_{OL}	I_O = 0.4 mA: EIO1, EIO2	V_{SS}		0.2 V_{DD}	V
Output on resistance	R_{OUT}	V_{EE} = 20 V, $V_0 – V_0$ = 0.5 V, $V_2 – V_0$ = 0.5 V, $V_0 – V_3$ = 0.5 V, $V_0 – V_5$ = 0.5 V, V_0 = 20 V, V_2 = 20 V, V_3 = 0 V, V_5 = 0 V: OUT1 to OUT240		0.8	1.6	kΩ
Current drain	I_{DD}	V_{DD} = 3 to 5.5 V			7.5	µA
Operating current drain	I_{EE}	V_{DD} = 3 to 5.5 V, V_{EEn} = 26 V*1			3.0	mA
		V_{DD} = 5 V ± 10%, V_{EEn} = 36 V			3.0	mA
Static current	Istb	*2			750	µA

Note: 1. With LOAD = 28 kHz, fcp = 6.5 MHz, f_{DF} = 75 Hz, or with no output load. Input voltages V_{IH} and V_{IL} must be V_{DD} and V_{SS}, respectively.
2. The standby current drain rating assumes that the EIOn (input) are at V_{DD}.

Block Diagram



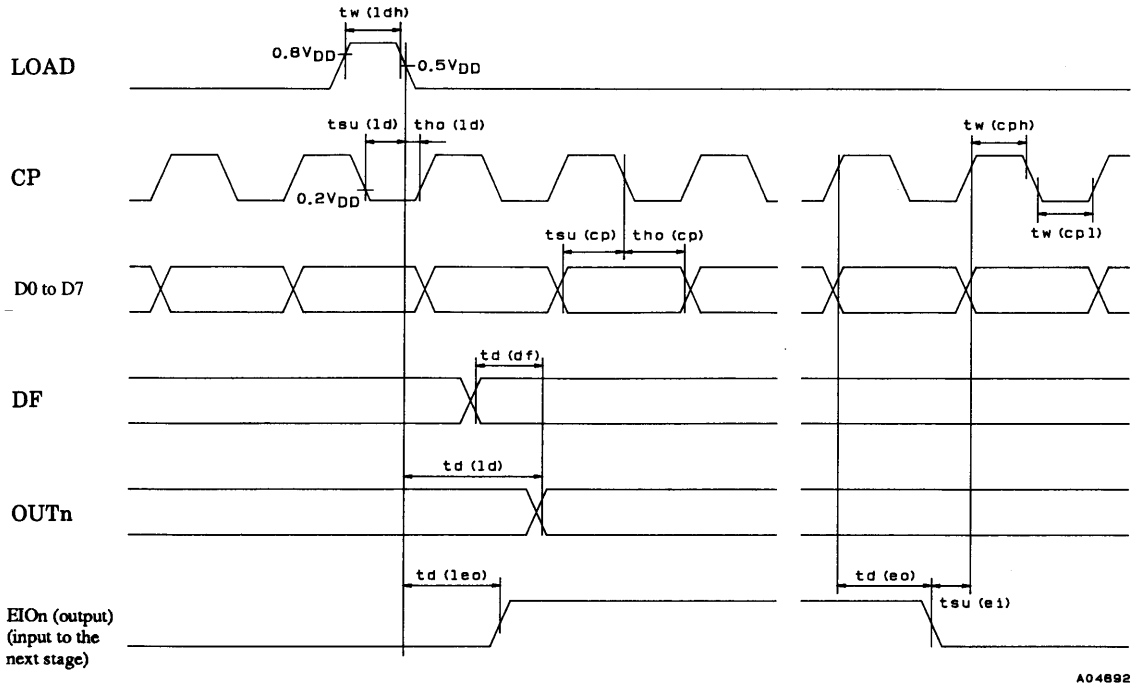
Switching Characteristics

at V_{DD} = 5 V ± 10%, Ta = –20 to +75°C

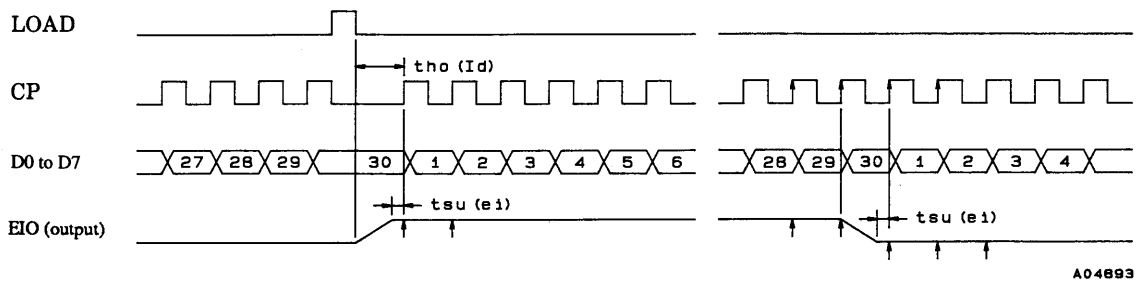
Parameter	Symbol	Conditions	min	typ	max	Unit
EIO output delay time	$t_{d\ (eo)}$	30 pF capacitive load			39	ns
LD/EIO output delay time	$t_{d\ (leo)}$	30 pF capacitive load			70	ns
LOAD-OUTn delay time	$t_{d\ (ldo)}$	100 pF capacitive load			700	µs
DF-OUTn delay time	$t_{d\ (dfo)}$	100 pF capacitive load			1.4	µs

at V_{DD} = 3 to 4.5 V, Ta = –20 to +75°C

Parameter	Symbol	Conditions	min	typ	max	Unit
EIO output delay time	$t_{d\ (eo)}$	30 pF capacitive load			80	ns
LD/EIO output delay time	$t_{d\ (leo)}$	30 pF capacitive load			130	ns
LOAD-OUTn delay time	$t_{d\ (ldo)}$	100 pF capacitive load			3	µs
DF-OUTn delay time	$t_{d\ (dfo)}$	100 pF capacitive load			3	µs



Note: 1. Since this IC detects the EIO inputs on the rising edge of the CP signal, the EIO inputs must be set up before the first data is input. As a result, a tho(ld) clock stop period is required directly after the rise of the LOAD signal if the clock frequency is relatively high.



Note: 2. If this IC is used with a 4-bit width data input, the number of data clocks between one LOAD and the next LOAD must be doubled.

Pin Functions

<table>
<tr><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>OUT1 to
OUT240</td><td>O</td><td>LCD drive outputs
<table>
<tr><th>DF</th><th>Data</th><th>DISP</th><th>OUTn</th></tr>
<tr><td>1</td><td>1</td><td>1</td><td>V_0</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>V_2</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>V_3</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>V_5</td></tr>
<tr><td>*</td><td>*</td><td>0</td><td>V_5</td></tr>
</table>
Note: * don't care (0 or 1).</td></tr>
<tr><td>V_0
V_2
V_3
V_5</td><td>I
I
I
I</td><td>V_0 level drive voltage input
V_2 level drive voltage input
V_3 level drive voltage input
V_5 level drive voltage input
} All pins with the same name must be set to the same potential.</td></tr>
<tr><td>V_{EE1}/V_{EE2}</td><td>–</td><td>High-voltage block power supply. V_{EE1} and V_{EE2} must have the same potential.</td></tr>
<tr><td>V_{SS1}/V_{SS2}</td><td>–</td><td>High-voltage block ground. V_{SS1} and V_{SS2} must have the same potential.</td></tr>
<tr><td>DISP</td><td>I</td><td>All outputs will be held at a fixed V_5 level when this pin is low.</td></tr>
<tr><td>DF</td><td>I</td><td>Alternation input</td></tr>
<tr><td>EIO1
EIO2</td><td>I/O
I/O</td><td>Enable inputs and outputs
<table>
<tr><th>L/R</th><th>EIO1</th><th>EIO2</th></tr>
<tr><td>L</td><td>In</td><td>Out</td></tr>
<tr><td>H</td><td>Out</td><td>In</td></tr>
</table>
Enable inputs: Tie the first stage enable input to V_{SS}, and then connect the enable input of each following stage to the enable output of the preceding stage.
Enable outputs: When connecting multiple chips in cascade, connect the enable output to the enable input of the next stage.</td></tr>
<tr><td>CP</td><td>I</td><td>Data acquisition clock (falling edge)</td></tr>
<tr><td>LOAD</td><td>I</td><td>Data load clock (falling edge)</td></tr>
<tr><td>BS</td><td>I</td><td>4-bit/8-bit switching signal; high: 8 bits, low: 4 bits</td></tr>
<tr><td>L/R</td><td>I</td><td>8×30: Data latch (BS = high)
<table>
<tr><th>L/R</th><th>CP:</th><th>1</th><th>2</th><th>3</th><th>4</th><th>29</th><th>30</th></tr>
<tr><td rowspan="8">L</td><td>D7</td><td>1</td><td>9</td><td>17</td><td>25</td><td>• • • 225</td><td>233</td></tr>
<tr><td>D6</td><td>2</td><td>10</td><td>18</td><td>26</td><td>• • • 226</td><td>234</td></tr>
<tr><td>D5</td><td>3</td><td>11</td><td>19</td><td>27</td><td>• • • 227</td><td>235</td></tr>
<tr><td>D4</td><td>4</td><td>12</td><td>20</td><td>28</td><td>• • • 228</td><td>236</td></tr>
<tr><td>D3</td><td>5</td><td>13</td><td>21</td><td>29</td><td>• • • 229</td><td>237</td></tr>
<tr><td>D2</td><td>6</td><td>14</td><td>22</td><td>30</td><td>• • • 230</td><td>238</td></tr>
<tr><td>D1</td><td>7</td><td>15</td><td>23</td><td>31</td><td>• • • 231</td><td>239</td></tr>
<tr><td>D0</td><td>8</td><td>16</td><td>24</td><td>32</td><td>• • • 232</td><td>240</td></tr>
<tr><td rowspan="8">H</td><td>D7</td><td>240</td><td>232</td><td>224</td><td>216</td><td>• • • 16</td><td>8</td></tr>
<tr><td>D6</td><td>239</td><td>231</td><td>223</td><td>215</td><td>• • • 15</td><td>7</td></tr>
<tr><td>D5</td><td>238</td><td>230</td><td>222</td><td>214</td><td>• • • 14</td><td>6</td></tr>
<tr><td>D4</td><td>237</td><td>229</td><td>221</td><td>213</td><td>• • • 13</td><td>5</td></tr>
<tr><td>D3</td><td>236</td><td>228</td><td>220</td><td>212</td><td>• • • 12</td><td>4</td></tr>
<tr><td>D2</td><td>235</td><td>227</td><td>219</td><td>211</td><td>• • • 11</td><td>3</td></tr>
<tr><td>D1</td><td>234</td><td>226</td><td>218</td><td>210</td><td>• • • 10</td><td>2</td></tr>
<tr><td>D0</td><td>233</td><td>225</td><td>217</td><td>209</td><td>• • • 9</td><td>1</td></tr>
</table>
Note: The numbers 1 to 240 in the table indicate OUT output numbers.</td></tr>
</table>

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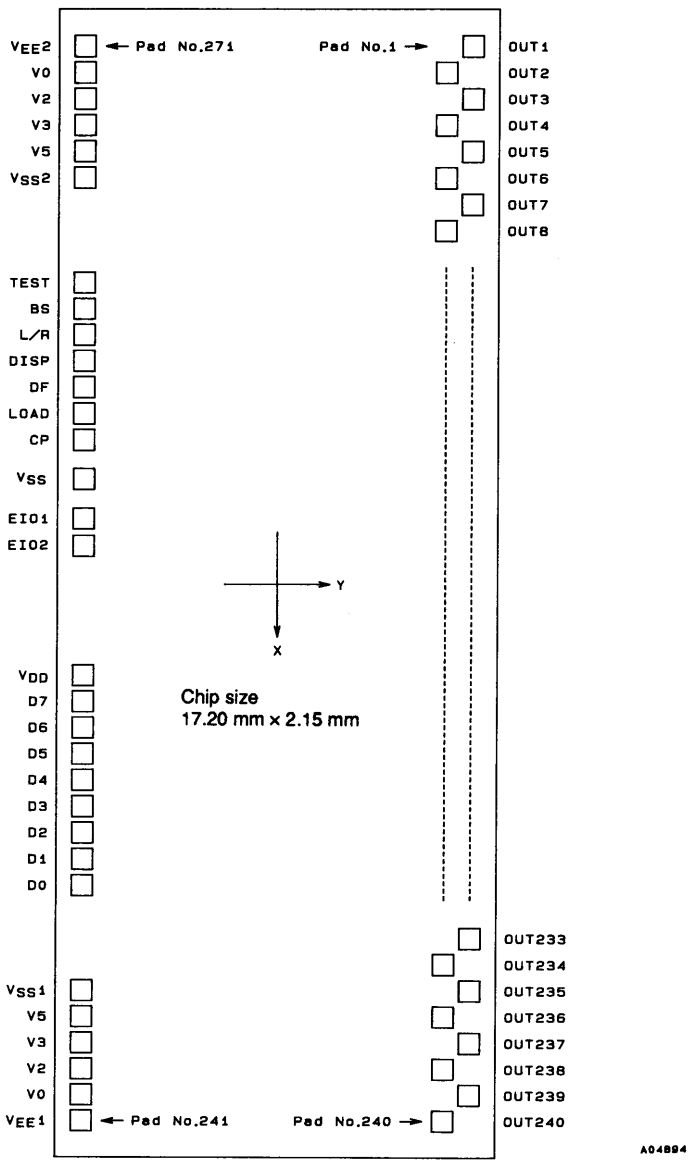
<table>
<tr><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>L/R</td><td>I</td><td>4×60: Data latch (BS = low)
<table>
<tr><th>L/R</th><th>CP:</th><th>1</th><th>2</th><th>3</th><th>59</th><th>60</th></tr>
<tr><td rowspan="4">L</td><td>D3</td><td>1</td><td>5</td><td>9</td><td>•••233</td><td>237</td></tr>
<tr><td>D2</td><td>2</td><td>6</td><td>10</td><td>•••234</td><td>238</td></tr>
<tr><td>D1</td><td>3</td><td>7</td><td>11</td><td>•••235</td><td>239</td></tr>
<tr><td>D0</td><td>4</td><td>8</td><td>12</td><td>•••236</td><td>240</td></tr>
<tr><td rowspan="4">H</td><td>D3</td><td>240</td><td>236</td><td>232</td><td>•••8</td><td>4</td></tr>
<tr><td>D2</td><td>239</td><td>235</td><td>231</td><td>•••7</td><td>3</td></tr>
<tr><td>D1</td><td>238</td><td>234</td><td>230</td><td>•••6</td><td>2</td></tr>
<tr><td>D0</td><td>237</td><td>233</td><td>229</td><td>•••5</td><td>1</td></tr>
</table>
Note: The numbers 1 to 240 in the table indicate OUT output numbers.</td></tr>
<tr><td>TEST</td><td>I</td><td>Test input. This pin must be connected to V_{SS} externally.</td></tr>
<tr><td>D0 to D7</td><td>I</td><td>Parallel data inputs. D0 to D3 are used when 4-bit input is used.
In that case, D4 to D7 must be connected to V_{DD} or V_{SS}.</td></tr>
<tr><td>V_{DD}</td><td>–</td><td>Logic system power supply</td></tr>
<tr><td>V_{SS}</td><td>–</td><td>Logic system ground</td></tr>
</table>

Pad Assignment



Pad Coordinates

Pad No.	Signal	X coordinate	Y coordinate	Pad No.	Signal	X coordinate	Y coordinate
1	OUT1	–8365	895	51	OUT51	–4865	895
2	OUT2	–8295	725	52	OUT52	–4795	725
3	OUT3	–8225	895	53	OUT53	–4725	895
4	OUT4	–8155	725	54	OUT54	–4655	725
5	OUT5	–8085	895	55	OUT55	–4585	895
6	OUT6	–8015	725	56	OUT56	–4515	725
7	OUT7	–7945	895	57	OUT57	–4445	895
8	OUT8	–7875	725	58	OUT58	–4375	725
9	OUT9	–7805	895	59	OUT59	–4305	895
10	OUT10	–7735	725	60	OUT60	–4235	725
11	OUT11	–7665	895	61	OUT61	–4165	895
12	OUT12	–7595	725	62	OUT62	–4095	725
13	OUT13	–7525	895	63	OUT63	–4025	895
14	OUT14	–7455	725	64	OUT64	–3955	725
15	OUT15	–7385	895	65	OUT65	–3885	895
16	OUT16	–7315	725	66	OUT66	–3815	725
17	OUT17	–7245	895	67	OUT67	–3745	895
18	OUT18	–7175	725	68	OUT68	–3675	725
19	OUT19	–7105	895	69	OUT69	–3605	895
20	OUT20	–7035	725	70	OUT70	–3535	725
21	OUT21	–6965	895	71	OUT71	–3465	895
22	OUT22	–6895	725	72	OUT72	–3395	725
23	OUT23	–6825	895	73	OUT73	–3325	895
24	OUT24	–6755	725	74	OUT74	–3255	725
25	OUT25	–6685	895	75	OUT75	–3185	895
26	OUT26	–6615	725	76	OUT76	–3115	725
27	OUT27	–6545	895	77	OUT77	–3045	895
28	OUT28	–6475	725	78	OUT78	–2975	725
29	OUT29	–6405	895	79	OUT79	–2905	895
30	OUT30	–6335	725	80	OUT80	–2835	725
31	OUT31	–6265	895	81	OUT81	–2765	895
32	OUT32	–6195	725	82	OUT82	–2695	725
33	OUT33	–6125	895	83	OUT83	–2625	895
34	OUT34	–6055	725	84	OUT84	–2555	725
35	OUT35	–5985	895	85	OUT85	–2485	895
36	OUT36	–5915	725	86	OUT86	–2415	725
37	OUT37	–5845	895	87	OUT87	–2345	895
38	OUT38	–5775	725	88	OUT88	–2275	725
39	OUT39	–5705	895	89	OUT89	–2205	895
40	OUT40	–5635	725	90	OUT90	–2135	725
41	OUT41	–5565	895	91	OUT91	–2065	895
42	OUT42	–5495	725	92	OUT92	–1995	725
43	OUT43	–5425	895	93	OUT93	–1925	895
44	OUT44	–5355	725	94	OUT94	–1855	725
45	OUT45	–5285	895	95	OUT95	–1785	895
46	OUT46	–5215	725	96	OUT96	–1715	725
47	OUT47	–5145	895	97	OUT97	–1645	895
48	OUT48	–5075	725	98	OUT98	–1575	725
49	OUT49	–5005	895	99	OUT99	–1505	895
50	OUT50	–4935	725	100	OUT100	–1435	725

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Pad No.	Signal	X coordinate	Y coordinate	Pad No.	Signal	X coordinate	Y coordinate
101	OUT101	–1365	895	151	OUT151	2135	895
102	OUT102	–1295	725	152	OUT152	2205	725
103	OUT103	–1225	895	153	OUT153	2275	895
104	OUT104	–1155	725	154	OUT154	2345	725
105	OUT105	–1085	895	155	OUT155	2415	895
106	OUT106	–1015	725	156	OUT156	2485	725
107	OUT107	–945	895	157	OUT157	2555	895
108	OUT108	–875	725	158	OUT158	2625	725
109	OUT109	–805	895	159	OUT159	2695	895
110	OUT110	–735	725	160	OUT160	2765	725
111	OUT111	–665	895	161	OUT161	2835	895
112	OUT112	–595	725	162	OUT162	2905	725
113	OUT113	–525	895	163	OUT163	2975	895
114	OUT114	–455	725	164	OUT164	3045	725
115	OUT115	–385	895	165	OUT165	3115	895
116	OUT116	–315	725	166	OUT166	3185	725
117	OUT117	–245	895	167	OUT167	3255	895
118	OUT118	–175	725	168	OUT168	3325	725
119	OUT119	–105	895	169	OUT169	3395	895
120	OUT120	–35	725	170	OUT170	3465	725
121	OUT121	35	895	171	OUT171	3535	895
122	OUT122	105	725	172	OUT172	3605	725
123	OUT123	175	895	173	OUT173	3675	895
124	OUT124	245	725	174	OUT174	3745	725
125	OUT125	315	895	175	OUT175	3815	895
126	OUT126	385	725	176	OUT176	3885	725
127	OUT127	455	895	177	OUT177	3955	895
128	OUT128	525	725	178	OUT178	4025	725
129	OUT129	595	895	179	OUT179	4095	895
130	OUT130	665	725	180	OUT180	4165	725
131	OUT131	735	895	181	OUT181	4235	895
132	OUT132	805	725	182	OUT182	4305	725
133	OUT133	875	895	183	OUT183	4375	895
134	OUT134	945	725	184	OUT184	4445	725
135	OUT135	1015	895	185	OUT185	4515	895
136	OUT136	1085	725	186	OUT186	4585	725
137	OUT137	1155	895	187	OUT187	4655	895
138	OUT138	1225	725	188	OUT188	4725	725
139	OUT139	1295	895	189	OUT189	4795	895
140	OUT140	1365	725	190	OUT190	4865	725
141	OUT141	1435	895	191	OUT191	4935	895
142	OUT142	1505	725	192	OUT192	5005	725
143	OUT143	1575	895	193	OUT193	5075	895
144	OUT144	1645	725	194	OUT194	5145	725
145	OUT145	1715	895	195	OUT195	5215	895
146	OUT146	1785	725	196	OUT196	5285	725
147	OUT147	1855	895	197	OUT197	5355	895
148	OUT148	1925	725	198	OUT198	5425	725
149	OUT149	1995	895	199	OUT199	5495	895
150	OUT150	2065	725	200	OUT200	5565	725

Continued on next page.

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Pad No.	Signal	X coordinate	Y coordinate	Pad No.	Signal	X coordinate	Y coordinate
201	OUT201	5635	895	237	OUT237	8155	895
202	OUT202	5705	725	238	OUT238	8225	725
203	OUT203	5775	895	239	OUT239	8295	895
204	OUT204	5845	725	240	OUT240	8365	725
205	OUT205	5915	895	241	V_{EE1}	8295	–895
206	OUT206	5985	725	242	V_0	7895	–885
207	OUT207	6055	895	243	V_2	7495	–885
208	OUT208	6125	725	244	V_3	7095	–895
209	OUT209	6195	895	245	V_5	6695	–895
210	OUT210	6265	725	246	V_{SS1}	6295	–895
211	OUT211	6335	895	247	D0	5055	–895
212	OUT212	6405	725	248	D1	4855	–895
213	OUT213	6475	895	249	D2	4655	–895
214	OUT214	6545	725	250	D3	4455	–895
215	OUT215	6615	895	251	D4	4255	–895
216	OUT216	6685	725	252	D5	4055	–895
217	OUT217	6755	895	253	D6	3855	–895
218	OUT218	6825	725	254	D7	3655	–895
219	OUT219	6895	895	255	V_{DD}	3335	–895
220	OUT220	6965	725	256	EIO2	–1295	–895
221	OUT221	7035	895	257	EIO1	–1895	–895
222	OUT222	7105	725	258	V_{SS}	–3095	–895
223	OUT223	7175	895	259	CP	–3495	–895
224	OUT224	7245	725	260	LOAD	–3695	–895
225	OUT225	7315	895	261	DF	–3895	–895
226	OUT226	7385	725	262	DISP	–4095	–895
227	OUT227	7455	895	263	L/R	–4495	–895
228	OUT228	7525	725	264	BS	–4695	–895
229	OUT229	7595	895	265	TEST	–5095	–895
230	OUT230	7665	725	266	V_{SS2}	–6295	–885
231	OUT231	7735	895	267	V_5	–6695	–885
232	OUT232	7805	725	268	V_3	–7095	–885
233	OUT233	7875	895	269	V_2	–7495	–885
234	OUT234	7945	725	270	V_0	–7895	–885
235	OUT235	8015	895	271	V_{EE2}	–8295	–895
236	OUT236	8085	725				

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