



# LC72P366

## On-Chip One-Time Programmable PROM Single-Chip PLL Controller



### Overview

The LC72P366 is a single-chip PLL-plus-controller one-time programmable PROM microcontroller that corresponds to the Sanyo LC72358N, LC72362N, and LC72366. The LC72P366 has the same package and pin assignment as the LC72358N, LC72362N, and LC72366 mask ROM versions, and provides 32 KB of on-chip PROM, organized as 16k words by 16 bits. The LC72P366 can prove useful in reducing the startup times for initial production runs and for reducing the switchover time when end-product specifications change.

### Features

- 32 KB (16k words × 16 bits) of on-chip PROM
  - This is a one-time programmable 32 KB (16k-word × 16-bit) PROM.
- Pin compatible with the mask ROM versions, i.e. identical package and pin assignment.

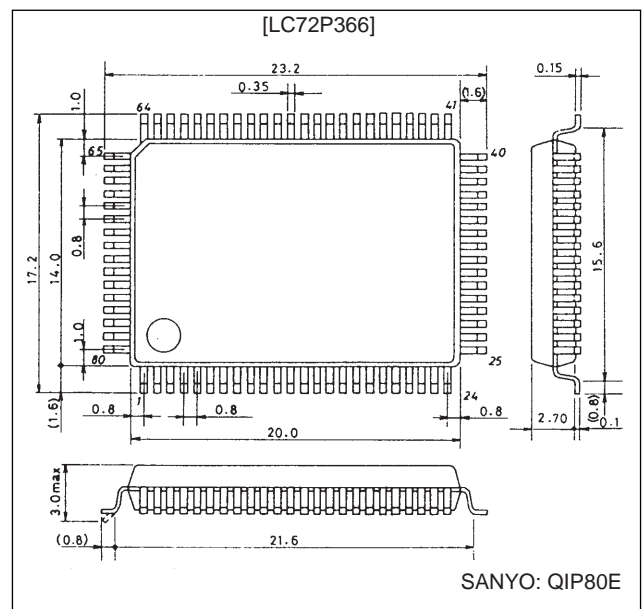
### Writing Sanyo ROMs

Sanyo provides a for-fee ROM writing service that consists of writing data to the PROM in one-time programmable PROM microcontrollers, printing, screening, and data readout verification. Contact your Sanyo sales representative for details.

### Package Dimensions

unit: mm

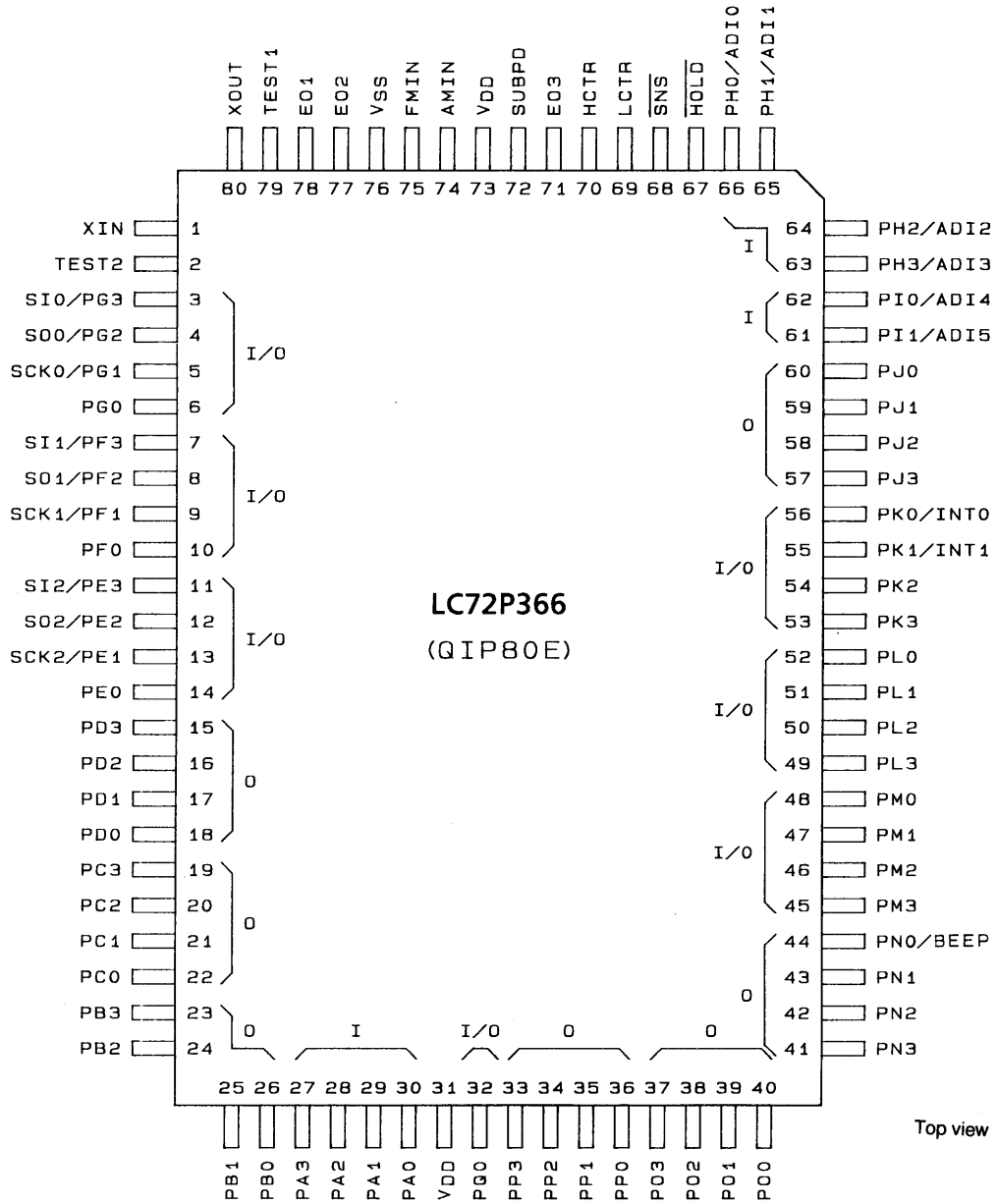
#### 3174-QFP80E



- CCB is a trademark of SANYO ELECTRIC CO., LTD.
- CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.

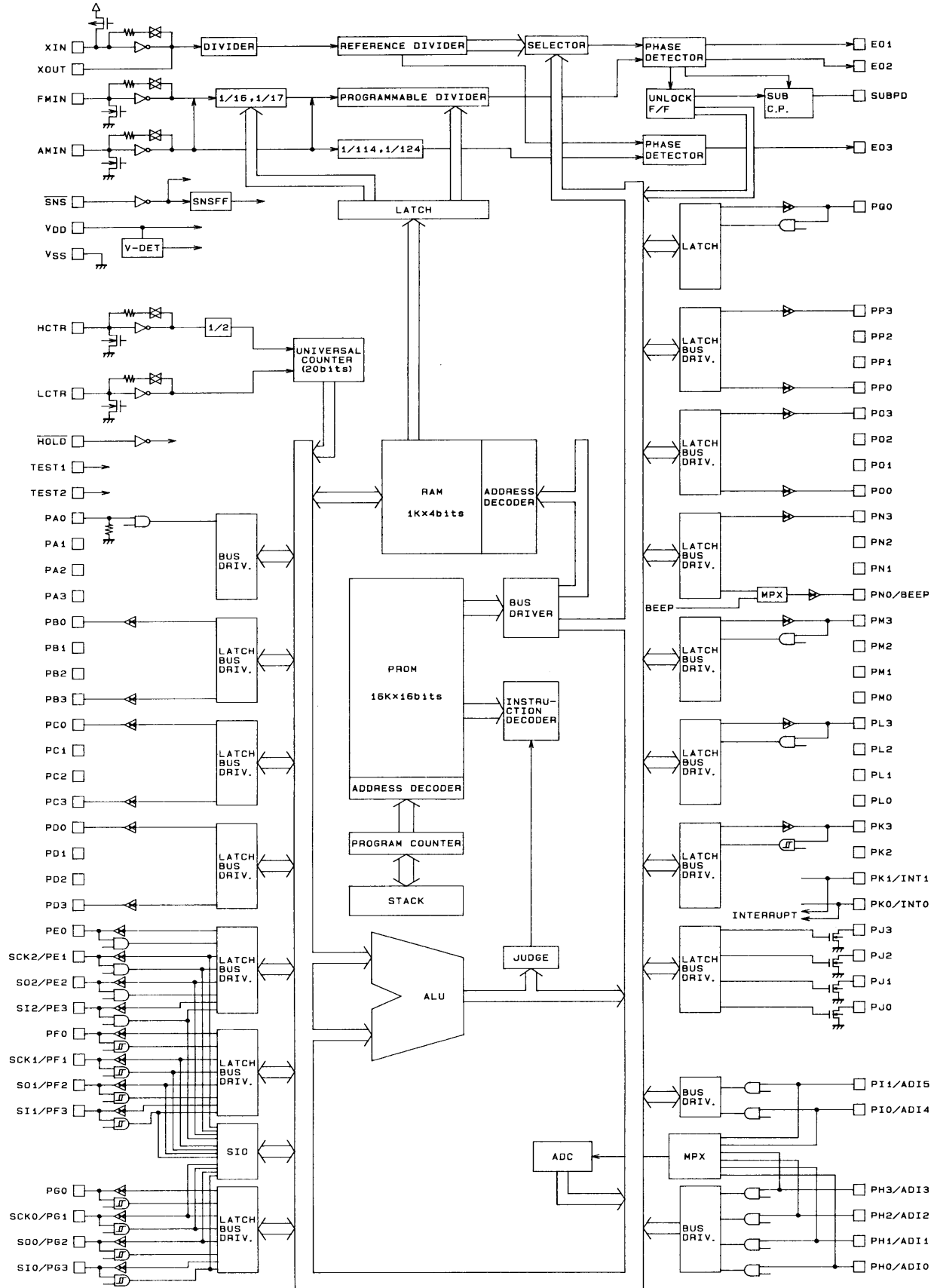
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## Pin Assignment



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Block Diagram



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## LC72P366

### Specifications

**Absolute Maximum Ratings at  $T_a = 25^\circ\text{C}$ ,  $V_{SS} = 0\text{ V}$**

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD\text{ max}}$		-0.3 to +6.5	V
Input voltage	$V_{IN}$	All input pins	-0.3 to $V_{DD} + 0.3$	V
Output voltage	$V_{OUT(1)}$	Port J	-0.3 to +15	V
	$V_{OUT(2)}$	All output ports other than $V_{OUT(1)}$	-0.3 to $V_{DD} + 0.3$	V
Output current	$I_{OUT(1)}$	Port J	0 to +5	mA
	$I_{OUT(2)}$	Ports D, E, F, G, K, L, M, N, O, P, and Q, EO1, EO2, EO3, SUBPD	0 to +3	mA
	$I_{OUT(3)}$	Ports B and C	0 to +1	mA
Allowable power dissipation	$Pd\text{ max}$	$T_a = -30\text{ to }+70^\circ\text{C}$	400	mW
Operating temperature	$T_{opr}$		-30 to +70	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-45 to +125	$^\circ\text{C}$

**Allowable Operating Ranges at  $T_a = -30\text{ to }+70^\circ\text{C}$ ,  $V_{DD} = 3.5\text{ to }5.5\text{ V}$**

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	$V_{DD(1)}$	CPU and PLL circuit operating	4.5	5.0	5.5	V
	$V_{DD(2)}$	CPU operating	4.0		5.5	V
	$V_{DD(3)}$	Memory retention voltage	1.3		5.5	V
Input high-level voltage	$V_{IH(1)}$	Ports E, H, I, L, M, and Q, HCTR, LCTR (when selected for input)	$0.7 V_{DD}$		$V_{DD}$	V
	$V_{IH(2)}$	Ports F, G, and K, LCTR (in period measurement mode), $\overline{\text{HOLD}}$	$0.8 V_{DD}$		$V_{DD}$	V
	$V_{IH(3)}$	$\overline{\text{SNS}}$	2.5		$V_{DD}$	V
	$V_{IH(4)}$	Port A	$0.6 V_{DD}$		$V_{DD}$	V
Input low-level voltage	$V_{IL(1)}$	Ports E, H, I, L, M, and Q, HCTR, LCTR (when selected for input)	0		$0.3 V_{DD}$	V
	$V_{IL(2)}$	Ports A, F, G, and K, LCTR (in period measurement mode)	0		$0.2 V_{DD}$	V
	$V_{IL(3)}$	$\overline{\text{SNS}}$	0		1.3	V
	$V_{IL(4)}$	$\overline{\text{HOLD}}$	0		$0.4 V_{DD}$	V
Input frequency	$f_{IN(1)}$	XIN	4.0	4.5	5.0	MHz
	$f_{IN(2)}$	FMIN : $V_{IN(2)}$ , $V_{DD(1)}$	10		150	MHz
	$f_{IN(3)}$	FMIN : $V_{IN(3)}$ , $V_{DD(1)}$	10		130	MHz
	$f_{IN(4)}$	AMIN(H) : $V_{IN(3)}$ , $V_{DD(1)}$	2.0		40	MHz
	$f_{IN(5)}$	AMIN(L) : $V_{IN(3)}$ , $V_{DD(1)}$	0.5		10	MHz
	$f_{IN(6)}$	HCTR : $V_{IN(3)}$ , $V_{DD(1)}$	0.4		12	MHz
	$f_{IN(7)}$	LCTR : $V_{IN(3)}$ , $V_{DD(1)}$	100		500	kHz
	$f_{IN(8)}$	LCTR (in period measurement mode): $V_{IH(2)}$ , $V_{IL(2)}$ , $V_{DD(1)}$	1		$20 \times 10^3$	Hz
Input amplitude	$V_{IN(1)}$	XIN	0.5		1.5	V <sub>rms</sub>
	$V_{IN(2)}$	FMIN	0.10		1.5	V <sub>rms</sub>
	$V_{IN(3)}$	FMIN, AMIN, HCTR, LCTR	0.07		1.5	V <sub>rms</sub>
Input voltage range	$V_{IN(4)}$	ADI0 to ADI5	0		$V_{DD}$	V

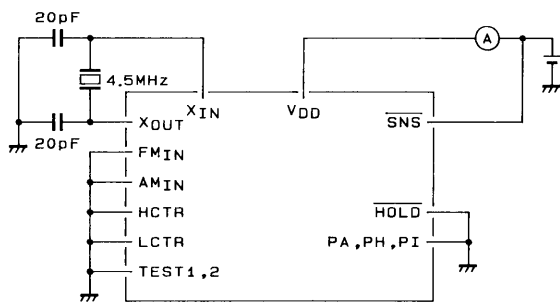
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## Electrical Characteristics in the Allowable Operating Ranges

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high-level current	$I_{IH(1)}$	XIN : $V_I = V_{DD} = 5.0\text{ V}$	2.0	5.0	15	$\mu\text{A}$
	$I_{IH(2)}$	FMIN, AMIN, HCTR, LCTR : $V_I = V_{DD} = 5.0\text{ V}$	4.0	10	30	$\mu\text{A}$
	$I_{IH(3)}$	Ports A, E, F, G, H, I, K, L, M, and Q, SNS, HOLD, HCTR, LCTR, and with no pull-down resistor on port A, $V_I = V_{DD} = 5.0\text{ V}$ With input mode selected for ports E, F, G, K, L, M, and Q			3.0	$\mu\text{A}$
	$I_{IH(4)}$	Port A: pull-down resistor present		50		$\mu\text{A}$
Input low-level current	$I_{IL(1)}$	XIN: $V_I = V_{SS}$	2.0	5.0	15	$\mu\text{A}$
	$I_{IL(2)}$	FMIN, AMIN, HCTR, LCTR : $V_{SS}$	4.0	10	30	$\mu\text{A}$
	$I_{IL(3)}$	Ports A, E, F, G, H, I, K, L, M, and Q, SNS, HOLD, HCTR, LCTR, and with no pull-down resistor on port A, $V_I = V_{SS}$ With input mode selected for ports E, F, G, K, L, M, and Q			3.0	$\mu\text{A}$
Input floating voltage	$V_{IF}$	Port A: pull-down resistor present			$0.05 V_{DD}$	V
Pull-down resistance	$R_{PD(1)}$	Port A: pull-down resistor present $V_{DD} = 5\text{ V}$	75	100	200	$\text{k}\Omega$
	$R_{PD(2)}$	TEST1, TEST2		10		$\text{k}\Omega$
Hysteresis	$V_H$	Ports F, G, and K, LCTR (in period measurement mode)	$0.1 V_{DD}$	$0.2 V_{DD}$		V
Output high-level voltage	$V_{OH(1)}$	Ports B and C: $I_O = -1\text{ mA}$	$V_{DD} - 2.0$	$V_{DD} - 1.0$		V
	$V_{OH(2)}$	Ports D, E, F, G, K, L, M, N, O, P, and Q: $I_O = -1\text{ mA}$	$V_{DD} - 1.0$			V
	$V_{OH(3)}$	EO1, EO2, EO3, SUBPD : $I_O = -500\ \mu\text{A}$	$V_{DD} - 1.0$			V
	$V_{OH(4)}$	XOUT : $I_O = -200\ \mu\text{A}$	$V_{DD} - 1.0$			V
Output low-level voltage	$V_{OL(1)}$	Ports B and C: $I_O = 50\ \mu\text{A}$		1.0	2.0	V
	$V_{OL(2)}$	Ports D, E, F, G, K, L, M, N, O, P, and Q: $I_O = 1\text{ mA}$			1.0	V
	$V_{OL(3)}$	EO1, EO2, EO3, SUBPD : $I_O = 500\ \mu\text{A}$			1.0	V
	$V_{OL(4)}$	XOUT : $I_O = 200\ \mu\text{A}$			1.5	V
	$V_{OL(5)}$	Port J: $I_O = 5\text{ mA}$			2.0	V
Output off leakage current	$I_{OFF(1)}$	Ports B, C, D, E, F, G, K, L, M, N, O, P, and Q	-3.0		+3.0	$\mu\text{A}$
	$I_{OFF(2)}$	EO1, EO2, EO3, SUBPD	-100		+100	nA
	$I_{OFF(3)}$	Port J	-5.0		+5.0	$\mu\text{A}$
A/D conversion error		AD10 to AD15 : $V_{DD(1)}$	-1/2		+1/2	LSB
Rejected pulse width	$P_{REJ}$	SNS			50	$\mu\text{s}$
Power down detection voltage	$V_{DET}$		3.0	3.5	4.0	V
Current drain	$I_{DD(1)}$	$V_{DD(1)}$ : $f_{IN(2)} = 130\text{ MHz}$ , $T_a = 25^\circ\text{C}$		12	24	mA
	$I_{DD(2)}$	$V_{DD(2)}$ : halt mode*, $T_a = 25^\circ\text{C}$ (See figure 1.)		0.45		mA
	$I_{DD(3)}$	$V_{DD} = 5.5\text{ V}$ , oscillator stopped $T_a = 25^\circ\text{C}$ (See figure 2.)			5	$\mu\text{A}$
	$I_{DD(4)}$	$V_{DD} = 2.5\text{ V}$ , oscillator stopped $T_a = 25^\circ\text{C}$ (See figure 2.)			1	$\mu\text{A}$

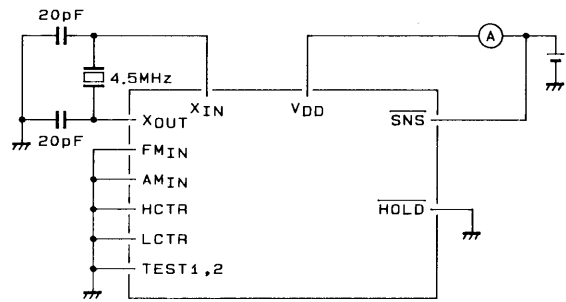
Note: \* Executing 20 STEP instructions every millisecond. With the PLL and counter circuits stopped.

### Test Circuit Diagrams



Note: With PB to PG, and PJ to PQ all open.  
However, with PE to PG, PK to PM, and PQ selected for output.

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Note: With PA to PQ all open.

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Figure 1  $I_{DD(2)}$  in Halt Mode

Figure 2  $I_{DD(3)}$  and  $I_{DD(4)}$  in Backup Mode



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Pin No.	Symbol	I/O	I/O type	Function															
76 73 31	$V_{SS}$ $V_{DD}$ $V_{DD}$	—	—	Power supply connections															
75	FMIN	I	Input	<p>FM VCO (local oscillator) input This pin is selected by the PLL instruction CW1 (b1, b0 are ignored). Capacitor coupling must be used for signal input. Input is disabled when the <math>\overline{HOLD}</math> pin is set low in the hold enable state. Input is disabled in clock stop mode, during the power-on reset, and in the PLL stop state.</p>															
74	AMIN	I	Input	<p>AM VCO (local oscillator) input This pin is selected and the band set by the PLL instruction CW1 (b1, b0).</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>b1</th> <th>b0</th> <th>Band</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td>2 to 40 MHz (SW)</td> </tr> <tr> <td>1</td> <td>1</td> <td>0.5 to 10 MHz (MW, LW)</td> </tr> </tbody> </table> <p>Capacitor coupling must be used for signal input. Input is disabled when the <math>\overline{HOLD}</math> pin is set low in the hold enable state. Input is disabled in clock stop mode, during the power-on reset, and in the PLL stop state.</p>	b1	b0	Band	1	0	2 to 40 MHz (SW)	1	1	0.5 to 10 MHz (MW, LW)						
b1	b0	Band																	
1	0	2 to 40 MHz (SW)																	
1	1	0.5 to 10 MHz (MW, LW)																	
72	SUBPD	O	CMOS tristate	<p>Sub-charge pump output This pin, in combination with the main charge pump, allows the construction of a high-speed locking circuit. The DZC instruction controls the sub-charge pump.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>b3</th> <th>b2</th> <th>Operation</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>High impedance</td> </tr> <tr> <td>0</td> <td>1</td> <td>Only operates in the unlocked state (450 kHz)</td> </tr> <tr> <td>1</td> <td>0</td> <td>Only operates in the unlocked state (900 kHz)</td> </tr> <tr> <td>1</td> <td>1</td> <td>Normal operation</td> </tr> </tbody> </table> <p>This pin goes to the high-impedance state when the <math>\overline{HOLD}</math> pin is set low in the hold enable state. This pin goes to the high-impedance state in clock stop mode, during the power-on reset, and in the PLL stop state.</p>	b3	b2	Operation	0	0	High impedance	0	1	Only operates in the unlocked state (450 kHz)	1	0	Only operates in the unlocked state (900 kHz)	1	1	Normal operation
b3	b2	Operation																	
0	0	High impedance																	
0	1	Only operates in the unlocked state (450 kHz)																	
1	0	Only operates in the unlocked state (900 kHz)																	
1	1	Normal operation																	
71	EO3	O	CMOS tristate	<p>Second PLL charge pump output This pin outputs a low level when the frequency generated by dividing the local oscillator signal frequency by N is higher than the reference frequency, and a high level when that frequency is lower. This pin goes to the high-impedance state when the frequencies match. (Note that this pin's output logic is the opposite of that of the EO1 and EO2 pins.) This pin goes to the high-impedance state when the <math>\overline{HOLD}</math> pin is set low in the hold enable state. This pin goes to the high-impedance state in clock stop mode, during the power-on reset, and in the PLL stop state.</p>															

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Pin No.	Symbol	I/O	I/O type	Function
70	HCTR	I	Input	<p>Universal counter/general-purpose input shared-function input port The IOS instruction b3 with PWn = 3 switches the pin function between universal counter input and general-purpose input.</p> <ul style="list-style-type: none"> <li>• Frequency measurement The universal counter function is selected by an IOS instruction with PWn = 3 and b3 = 0. HCTR frequency measurement mode is set up by a UCS instruction with b3 = 0 and b2 = 0, and counting is started with a UCC instruction after the count time is selected. The CNTEND flag is set when the count completes. To operate this circuit as an AC amplifier in this mode, the input must be capacitor coupled.</li> <li>• General-purpose input pin use The general-purpose input port function is selected by an IOS instruction with PWn = 3 and b3 = 1. An internal register (address: 0EH) input instruction INR (b0) is used to acquire data from this pin. Input is disabled in clock stop mode. (The input pin will be pulled down.) During the power-on reset, the universal counter function is selected.</li> </ul>
69	LCTR	I	Input	<p>Universal counter (frequency and period measurement)/general-purpose input shared-function input port The IOS instruction b2 with PWn = 3 switches the pin function between universal counter input and general-purpose input.</p> <ul style="list-style-type: none"> <li>• Frequency measurement The universal counter function is selected by an IOS instruction with PWn = 3 and b2 = 0. LCTR frequency measurement mode is set up by a UCS instruction with b3 = 0 b2 = 1, and counting is started with a UCC instruction after the count time is selected. The CNTEND flag is set when the count completes. To operate this circuit as an AC amplifier in this mode, the input must be capacitor coupled.</li> <li>• Period measurement With the universal counter function selected, set up period measurement mode with a UCS instruction with b3 = 1 and b2 = 0, and start the count with a UCC instruction after selecting the count time. The CNTEND flag will be set when the count completes. In this mode, the signal must be input with DC coupling to turn off the bias feedback resistor.</li> <li>• General-purpose input pin use The general-purpose input port function is selected by an IOS instruction with PWn = 3, b2 = 1. An internal register (address: 0EH) input instruction INR (b1) is used to acquire data from this pin. Input is disabled in clock stop mode. (The input pin will be pulled down.) During the power-on reset, the universal counter function (in HCTR frequency measurement mode) is selected.</li> </ul>
68	$\overline{\text{SNS}}$	I	Input	<p>Voltage sense/general-purpose input pin shared-function port This circuit is designed for a relatively low input threshold voltage.</p> <ul style="list-style-type: none"> <li>• Voltage sense pin usage This input pin is used to determine whether or not a power failure occurred after recovery from backup (clock stop) mode. An internal sense F/F is used for this determination. The sense F/F is tested with a TUL instruction (b2).</li> <li>• General-purpose input port usage When used as a general-purpose input port, the state is sensed by using a TUL instruction (b3).</li> </ul> <p>Since, unlike other input ports, input is not disabled in clock stop mode and during the power-on reset, special care is required with respect to through currents.</p>

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Pin No.	Symbol	I/O	I/O type	Function
67	$\overline{\text{HOLD}}$	I	Input	<p>PLL control and clock stop mode control</p> <p>Setting this pin low in the hold enabled state disables input to the FMIN and AMIN pins and sets the EO pin to the high-impedance state.</p> <p>To enter clock stop mode, set the HOLDEN flag, set this pin low, and execute a CKSTP instruction.</p> <p>To clear clock stop mode, set this pin high.</p>
66 65 64 63 62 61	PH0/ADI0 PH1/ADI1 PH2/ADI2 PH3/ADI3 PI0/ADI4 PI1/ADI5	I	Input	<p>General-purpose input port/A/D converter shared-function pins</p> <p>The IOS instruction with PWn = 7 or 8 switches the pin function between general-purpose input ports and A/D converter inputs.</p> <ul style="list-style-type: none"> <li>General-purpose input port usage Specify general-purpose input port usage with the IOS instruction with PWn = 7 or 8 in bit units.</li> <li>A/D converter usage Specify A/D converter usage with the IOS instruction with PWn = 7 or 8 in bit units. Specify the pin to convert with the IOS instruction with PWn = 1. Start a conversion with the UCC instruction (b2). The ADCE flag will be set when the conversion completes.</li> </ul> <p>Note: Executing an input instruction for a port specified for ADI usage will always return low since input is disabled. These pins must be set up for general-purpose input port usage before an input instruction is executed.</p> <p>Input is disabled in clock stop mode.</p> <p>During the power-on reset, these pins go to the general-purpose input port function.</p>
60 59 58 57	PJ0 PJ1 PJ2 PJ3	O	N-channel open drain	<p>General-purpose output ports</p> <p>An external pull-up resistor is required since these pins are open-drain circuits.</p> <p>In clock stop mode, these pins go to the transistor off state (high level output).</p> <p>During the power-on reset, these pins are set up as general-purpose output ports and go to the transistor off state (high level output).</p>
56 55 54 53	PK0/INT0 PK1/INT1 PK2 PK3	I/O	CMOS push-pull	<p>General-purpose I/O/external interrupt shared-function ports</p> <p>There is no instruction that switches the function of these ports between general-purpose ports and external interrupt ports. These pins function as external interrupt pins at the point where the external interrupt enable flag is set.</p> <ul style="list-style-type: none"> <li>General-purpose I/O port usage These pins can be set for input or output in bit units (bit I/O). The IOS instruction is used to specify input or output in bit units.</li> <li>External interrupt pin usage This function can be used by setting the external interrupt enable flags (INT0EN and INT1EN) in status register 2. The corresponding pin must be set up for input. To enable interrupt operation, the interrupt enable flag (INTEN) in status register 1 also must be set. The IOS instruction with PWn = 3, b1 = INT1, and b0 = INT0 is used to select rising or falling edge detection.</li> </ul> <p>In clock stop mode, input is disabled and these pins go to the high impedance state.</p> <p>During the power-on reset, these pins function as general-purpose input ports.</p>
52 to 45	PL0 to PL3 PM0 to PM3	I/O	CMOS push-pull	<p>General-purpose I/O ports</p> <p>The IOS instruction is used to specify input or output.</p> <p>In clock stop mode input is disabled and these pins go to the high impedance state.</p> <p>During the power-on reset, these pins function as general-purpose input ports.</p>

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Pin No.	Symbol	I/O	I/O type	Function
44 43 42 41	PN0/BEEP PN1 PN2 PN3	O	CMOS push-pull	<p>General-purpose output port/BEEP tone shared-function output pins The BEEP instruction switches between the general-purpose output port and BEEP tone functions.</p> <ul style="list-style-type: none"> <li>• General-purpose output port usage The BEEP instruction with b3 = 0 sets up the general-purpose output port function. Pins PN1 to PN3 are general-purpose output-only pins.</li> <li>• BEEP output usage The BEEP instruction with b3 = 1 sets up BEEP output. The BEEP instruction bits b0, b1 and b2 sets the frequency. When set up as the BEEP port, executing an output instruction will set the internal latch data but has no influence on the output.</li> </ul> <p>These pins go to the output high-impedance state in clock stop mode. These pins go to the output high-impedance state during the power-on reset and hold that state until an output instruction is executed.</p>
40 to 33	PO0 to PO3 PP0 to PP3	O	CMOS push-pull	<p>Output-only ports These pins go to the output high-impedance state in clock stop mode. These pins go to the output high-impedance state during the power-on reset and hold that state until an output instruction is executed.</p>
32	PQ0	I/O	CMOS push-pull	<p>General-purpose I/O ports The IOS instruction is used to specify input or output. The OUTF and INR instructions are used for output and input. The bit set, reset and test instruction cannot be used. In clock stop mode input is disabled and these pins go to the high impedance state. During the power-on reset, these pins function as general-purpose input ports.</p>
79 2	TEST1 TEST2			<p>LSI test pins These pins must be either left open or connected to ground.</p>

### Usage Notes

The LC72P366 is provided for use in initial shipments of products designed to use the Sanyo LC72358N, LC72362N, or LC72366. Keep the following points in mind when using this product.

- Differences between the LC72P366 and the LC72358N, LC72362N, and LC72366

Parameter	LC72P366	LC72358N, 72362N, 72366
Operating temperature	-30 to +70°C	-40 to +85°C
CPU operating voltage	Minimum 4.0 V	Minimum 3.5 V
	Typical	Typical
	Maximum 5.5 V	Maximum 5.5 V
Power down detection voltage (VDET)	Minimum 3.0 V	Minimum 2.7 V
	Typical 3.5 V	Typical 3.0 V
	Maximum 4.0 V	Maximum 3.3 V

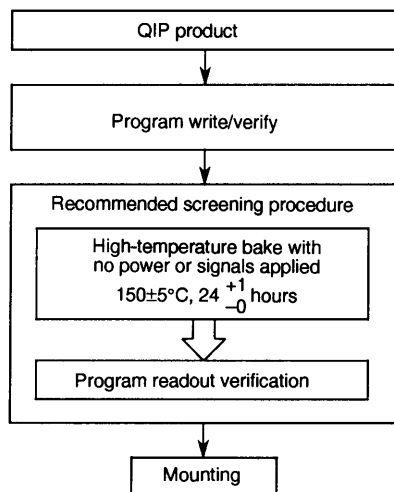
- ROM ordering procedure when using Sanyo's for-fee PROM programming service
  - When ordering one-time programmable versions and mask versions at the same time:  
The customer must provide the mask ROM version program, the mask ROM version order forms, and the one-time programmable version order forms.
  - When order just the one-time programmable version:  
The customer must provide the one-time programmable version program and the one-time programmable version order forms.

## LC72P366

- Conditions required for mounting the LC72P366

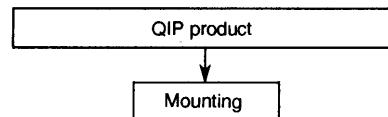
### 1. Products programmed by the user:

Mount the LC72P366 using the following procedure when using products shipped from Sanyo without the PROM having been programmed.



### 2. Products programmed by Sanyo:

Mount the LC72P366 using the following procedure when using products shipped from Sanyo with the PROM programmed by Sanyo.



#### [Caution]

- Due to the nature of the product, it is not possible for Sanyo to fully test one-time programmable PROM microcontrollers (i.e., products with blank PROMs) before shipment to the customer. This means that there will be some amount of yield reduction after programming.

## Usage Procedures

- Programming the on-chip PROM

There are two methods for writing the LC72P366 on-chip PROM as follows:

- Using a general-purpose PROM programmer

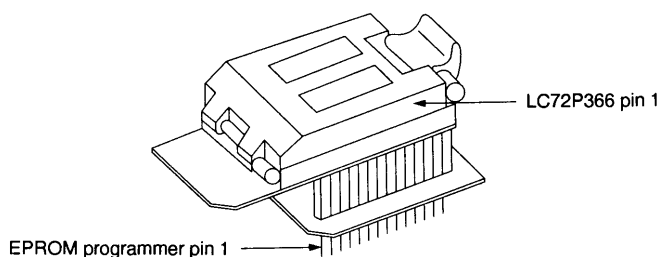
A general-purpose PROM programmer can be used if a special-purpose PROM programming adapter (product name: LC72P366 EPROM PROGRAMMER) is used. The write procedure used is the 27512 or 27C512 (with  $V_{pp} = 12.5$  V) Intel fast write method. Specify 0000H to 7FFFH as the address settings.

- Using the RE32N in-circuit emulator:

The RE32N in-circuit emulator can be used if a special-purpose PROM programming adapter (product name: LC72P366 RE32N) is used. Use the PGOTP command as the write method.

- Special-purpose writing adapters

Since there are two special-purpose PROM programming adapters as mentioned above, the correct adapter must be used.



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General-purpose EPROM programmer adapter	: Product name LC72P366 EPROM PROGRAMMER
	: Catalog no. NDK-DC-018
In-circuit emulator RE32 adapter	: Product name LC72P366 RE32N
	: Catalog no. NDK-DC-020

**LC72P366 Instruction Overview**

Abbreviations : ADDR : Program memory address

b : Borrow

C : Carry

DH : Data memory address high (Row address) [2 bits]

DL : Data memory address low (Column address) [4 bits]

I : Immediate data [4 bits]

M : Data Memory address

N : Bit position [4 bits]

Pn : Port number [4 bits]

PWn : Port control word number [4 bits]

r : General register (on of location 00 to 0FH in the current bank)

Rn : Register number [4 bits]

( ) : Contents of register or memory


( )n : Contents of bit N of register or memory

Instruction group	Mnemonic	Operand		Function	Operation	Machine code															
		1st	2nd			D15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	D0
Addition instructions	AD	r	M	Add M to r	$r \leftarrow (r) + (M)$	0	1	0	0	0	0	D <sub>H</sub>		D <sub>L</sub>				r			
	ADS	r	M	Add M to r, then skip if carry	$r \leftarrow (r) + (M)$ skip if carry	0	1	0	0	0	1	D <sub>H</sub>		D <sub>L</sub>				r			
	AC	r	M	Add M to r with carry	$r \leftarrow (r) + (M) + C$	0	1	0	0	1	0	D <sub>H</sub>		D <sub>L</sub>				r			
	ACS	r	M	Add M to r with carry, then skip if carry	$r \leftarrow (r) + (M) + C$ skip if carry	0	1	0	0	1	1	D <sub>H</sub>		D <sub>L</sub>				r			
	AI	M	I	Add I to M	$M \leftarrow (M) + I$	0	1	0	1	0	0	D <sub>H</sub>		D <sub>L</sub>				I			
	AIS	M	I	Add I to M, then skip if carry	$M \leftarrow (M) + I$ skip if carry	0	1	0	1	0	1	D <sub>H</sub>		D <sub>L</sub>				I			
	AIC	M	I	Add I to M with carry	$M \leftarrow (M) + I + C$	0	1	0	1	1	0	D <sub>H</sub>		D <sub>L</sub>				I			
	AICS	M	I	Add I to M with carry, then skip if carry	$M \leftarrow (M) + I + C$ skip if carry	0	1	0	1	1	1	D <sub>H</sub>		D <sub>L</sub>				I			
Subtraction instructions	SU	r	M	Subtract M from r	$r \leftarrow (r) - (M)$	0	1	1	0	0	0	D <sub>H</sub>		D <sub>L</sub>				r			
	SUS	r	M	Subtract M from r, then skip if borrow	$r \leftarrow (r) - (M)$ skip if borrow	0	1	1	0	0	1	D <sub>H</sub>		D <sub>L</sub>				r			
	SB	r	M	Subtract M from r with borrow	$r \leftarrow (r) - (M) - b$	0	1	1	0	1	0	D <sub>H</sub>		D <sub>L</sub>				r			
	SBS	r	M	Subtract M from r with borrow, then skip if borrow	$r \leftarrow (r) - (M) - b$ skip if borrow	0	1	1	0	1	1	D <sub>H</sub>		D <sub>L</sub>				I			
	SI	M	I	Subtract I from M	$M \leftarrow (M) - I$	0	1	1	1	0	0	D <sub>H</sub>		D <sub>L</sub>				I			
	SIS	M	I	Subtract I from M, then skip if borrow	$M \leftarrow (M) - I$ skip if borrow	0	1	1	1	0	1	D <sub>H</sub>		D <sub>L</sub>				I			
	SIB	M	I	Subtract I from M with borrow	$M \leftarrow (M) - I - b$	0	1	1	1	1	0	D <sub>H</sub>		D <sub>L</sub>				I			
	SIBS	M	I	Subtract I from M with borrow, then skip if borrow	$M \leftarrow (M) - I - b$ skip if borrow	0	1	1	1	1	1	D <sub>H</sub>		D <sub>L</sub>				I			
Comparison instructions	SEQ	r	M	Skip if r equal to M	(r) - (M) skip if zero	0	0	0	1	0	0	D <sub>H</sub>		D <sub>L</sub>				r			
	SEQI	M	I	Skip if M equal to I	(M) - I skip if zero	0	0	0	1	0	1	D <sub>H</sub>		D <sub>L</sub>				I			
	SNEI	M	I	Skip if M not equal to I	(M) - I skip if not zero	0	0	0	0	0	1	D <sub>H</sub>		D <sub>L</sub>				I			
	SGE	r	M	Skip if r is greater than or equal to M	(r) - (M) skip if not borrow	0	0	0	1	1	0	D <sub>H</sub>		D <sub>L</sub>				r			
	SGEI	M	I	Skip if M is greater than or equal to I	(M) - I skip if not borrow	0	0	0	1	1	1	D <sub>H</sub>		D <sub>L</sub>				I			
	SLEI	M	I	Skip if M is less than I	(M) - I skip if zero	0	0	0	0	1	1	D <sub>H</sub>		D <sub>L</sub>				I			

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Instruction group	Mnemonic	Operand		Function	Operation	Machine code																	
		1st	2n			D15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	D0		
Logical instructions	AND	r	M	AND M with r	$r \leftarrow (r) \text{ AND } (M)$	0	0	1	0	0	0	D <sub>H</sub>		D <sub>L</sub>				r					
	ANDI	M	I	AND I with M	$M \leftarrow (M) \text{ AND } I$	0	0	1	0	0	1	D <sub>H</sub>		D <sub>L</sub>				I					
	OR	r	M	OR M with r	$r \leftarrow (r) \text{ OR } (M)$	0	0	1	0	1	0	D <sub>H</sub>		D <sub>L</sub>				r					
	ORI	M	I	OR I with M	$M \leftarrow (M) \text{ OR } I$	0	0	1	0	1	1	D <sub>H</sub>		D <sub>L</sub>				r					
	EXL	r	M	Exclusive OR I with r	$r \leftarrow (r) \text{ XOR } I$	0	0	1	1	0	1	D <sub>H</sub>		D <sub>L</sub>				r					
	EXLI	M	I	Exclusive OR I with M	$M \leftarrow (M) \text{ XOR } I$	0	0	1	1	0	1	D <sub>H</sub>		D <sub>L</sub>				I					
	SHR	r		Shift r right with carry		0	0	0	0	0	0	0 0		1	1	1	0	r					
Transfer instructions	LD	r	M	Load M to r	$r \leftarrow (M)$	1	1	0	1	0	0	D <sub>H</sub>		D <sub>L</sub>				r					
	ST	M	r	Store r to M	$M \leftarrow (r)$	1	1	0	1	0	1	D <sub>H</sub>		D <sub>L</sub>				r					
	MVRD	r	M	Move M to destination M referring to r in the same row	$[DH, r] \leftarrow (M)$	1	1	0	1	1	0	D <sub>H</sub>		D <sub>L</sub>				r					
	MVRS	M	r	Move M to destination M referring to r in the same row	$M \leftarrow [DH, r]$	1	1	0	1	1	1	D <sub>H</sub>		D <sub>L</sub>				r					
	MVSR	M1	M2	Move source M referring to r to M in the same row	$[DH, DL1] \leftarrow [DH, DL2]$	1	1	1	0	0	0	D <sub>H</sub>		D <sub>L1</sub>				D <sub>L2</sub>					
	MVI	M	I	Move I to M	$M \leftarrow I$	1	1	1	0	0	1	D <sub>H</sub>		D <sub>L</sub>				I					
Bit test instructions	TMT	M	N	Test M bits, then skip if all bits specified are true	if $M(N) = \text{all "1"}$ , then skip	1	1	1	1	0	0	D <sub>H</sub>		D <sub>L</sub>				N					
	TMF	M	N	Test M bits, then skip if all bits specified are false	if $M(N) = \text{all "0"}$ , then skip	1	1	1	1	0	1	D <sub>H</sub>		D <sub>L</sub>				N					
Jump and subroutine instructions	JMP	ADDR		Jump to the address	$PC \leftarrow ADDR$	1	0	ADDR (14 bits)															
	CAL	ADDR		Call subroutine	$Stack \leftarrow (PC) + 1$	1	1	0	0	ADDR (12 bits)													
	RT			Return from subroutine	$PC \leftarrow Stack$	0	0	0	0	0	0	0	0	1 0 0 0									
	RTS			Return from subroutine and skip	$PC \leftarrow Stack + 1$	0	0	0	0	0	0	0	0	1 0 1 0									
	RTB			Return from subroutine with bank data	$PC \leftarrow Stack$ $BANK \leftarrow Stack$	1	1	1	1	1	1	1	1	1 1 0 0									
	RTBS			Return from subroutine with bank data and skip	$PC \leftarrow Stack + 1$ $BANK \leftarrow Stack$	1	1	1	1	1	1	1	1	1 1 0 1									
	RTI			Return from interrupt	$PC \leftarrow Stack$ $BANK \leftarrow Stack$ $CARRY \leftarrow Stack$	0	0	0	0	0	0	0	0	1 0 0 1									
Status register instructions	SS	I	N	Set status register	$(\text{Status reg } I) N \leftarrow 1$	1	1	1	1	1	1	1	1	0	0	0	I	N					
	RS	I	N	Reset status register	$(\text{Status reg } I) N \leftarrow 0$	1	1	1	1	1	1	1	1	0	0	1	I	N					
	TST	I	N	Test status register true	if $(\text{Status reg } I) N = \text{all "1"}$ , then skip	1	1	1	1	1	1	1	1	0	1	I		N					
	TSF	I	N	Test status register false	if $(\text{Status reg } I) N = \text{"0"}$ , then skip	1	1	1	1	1	1	1	1	1	0	I		N					
FF test instructions	TUL	N	Test unlock F/F then skip if it has not been set	if $\text{Unlock FF } (N) = \text{all "0"}$ , then skip	0	0	0	0	0	0	0	0	1 1 0 1				N						
Internal register transfer instructions	PLL	M	r	Load M to PLL register	$PLL \text{ reg } \leftarrow \text{PLL data}$	1	1	1	1	1	0	D <sub>H</sub>		D <sub>L</sub>				r					
	INR	M	Rn	Input register/port data to M	$M \leftarrow (Rn \text{ reg})$	0	0	1	1	1	0	D <sub>H</sub>		D <sub>L</sub>				Rn					
	OUTR	M	Rn	Output contents of M to register/port	$Rn \text{ reg } \leftarrow (M)$	0	0	1	1	1	1	D <sub>H</sub>		D <sub>L</sub>				Rn					

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Instruction group	Mnemonic	Operand		Function	Operation	Machine code																
		1st	2n			D15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	D0	
Hardware control instructions	SIO	I1	I2	Serial I/O control	SIO reg ← I1,I2	0	0	0	0	0	0	0	0	1	I1				I2			
	UCS	I		Set I to UCCW1	UCCW1 ← I	0	0	0	0	0	0	0	0	0	0	0	0	1	I			
	UCC	I		Set I to UCCW2	UCCW2 ← I	0	0	0	0	0	0	0	0	0	0	1	0	I				
	BEEP	I		Beep control	BEEP reg ← I	0	0	0	0	0	0	0	0	0	1	1	0	I				
	DZC	I		Dead zone control	DZC reg ← I	0	0	0	0	0	0	0	0	1	0	1	1	I				
	TMS	N		Set timer register	Timer reg ← I	0	0	0	0	0	0	0	0	1	1	0	0	N				
	IOS	PWn	N	Set port control word	IOS reg PWn ← N	1	1	1	1	1	1	1	0	PWn				N				
I/O instructions	IN	M	Pn	Input port data to M	M ← (Pn)	1	1	1	0	1	0	D <sub>H</sub>		D <sub>L</sub>				Pn				
	OUT	M	Pn	Output contents of M to port	Pn ← M	1	1	1	0	1	1	D <sub>H</sub>		D <sub>L</sub>				Pn				
	SPB	Pn	N	Set port bits	(Pn) N ← 1	0	0	0	0	0	0	1	0	Pn				N				
	RPB	Pn	N	Reset port bits	(Pn) N ← 0	0	0	0	0	0	0	1	1	Pn				N				
	TPT	Pn	N	Test port bit, then skip if all bits specified are true	if (Pn) N = all "1", then skip	1	1	1	1	1	1	0	0	Pn				N				
	TPF	Pn	N	Test port bits, then skip if all bits specified are false	if (Pn) N = all "0", then skip	1	1	1	1	1	1	0	1	Pn				N				
Bank switching instructions	BANK	I		Select Bank	BANK ← I	0	0	0	0	0	0	0	0	0	1	1	1	I				
Other instructions	HALT	I		Halt mode control	HALT reg ← I, then CPU clock stop	0	0	0	0	0	0	0	0	0	1	0	0	I				
	CKSTP			Clock stop	stop X'tal OSC if HOLD = 0	0	0	0	0	0	0	0	0	0	1	0	1					
	NOP			No operation	No operation	0	0	0	0	0	0	0	0	0	0	0	0					

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