

**LC74751****On-Screen Display LSI****Preliminary****Overview**

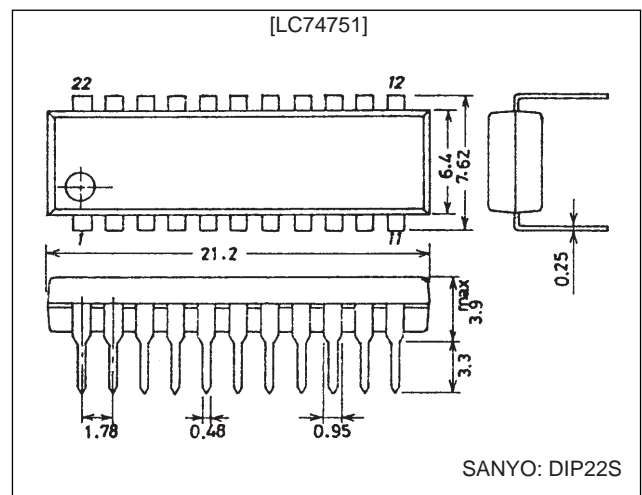
The LC74751 is a CMOS LSI that supports on-screen display of characters and patterns on a TV screen under the control of a microcontroller. The LC74751 includes an on-chip character ROM that provides 128 characters in a 12 × 18 dot format. This IC supports display of up to 12 lines of 24 characters each for a maximum of 288 characters.

Features

- Display format: 24 characters by 12 rows
- Characters displayed: Up to 288 characters
- Display control ROM (line ROM): ROM for 64 lines (Control in line units: lines consisting of 24 characters)
- Display RAM: 176 characters (Used for the specification of user-defined characters.)
- Character format: 12 (horizontal) × 18 (vertical) dots
- Characters in font: 128
- Character sizes: Four sizes each in the horizontal and vertical directions
- Initial display positions: 64 horizontal positions and 64 vertical positions
- Blinking: Specifiable in character units
- Blinking types:
 - Two periods supported: 1.0 second and 0.5 second
 - Three duty types supported: 25%, 50%, and 75%
- Blanking: Over the whole font (12 × 18 dots)
- Background color
 - 8 background colors (in internal synchronization mode): 4fsc (NTSC/PAL/PAL-M/PAL-N)
 - 4 background colors (in internal synchronization mode): 2fsc (NTSC)
 - Single background color (blue) (in internal synchronization mode): 2fsc (PAL/PAL-M/PAL-N)
- External control input: Serial data input
- Synchronizing signals: Supports switching between internal and external synchronizing signals.
- On-chip sync separator circuit
- Video output: Composite video output in the NTSC, PAL, PAL-M, or PAL-N format
- Superimpose function: Superimposes the character output on the composite video output.

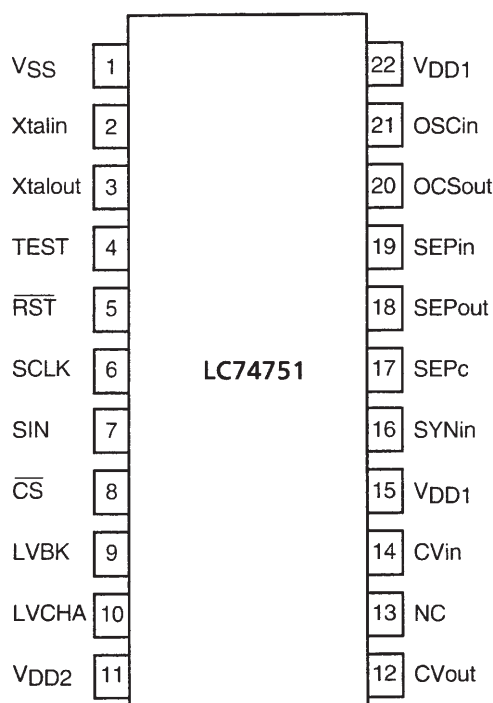
Package Dimensions

unit: mm

3059-DIP22S

LC74751

Pin Assignment



(Top view) A05637

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}	V_{DD1} and V_{DD2}	$V_{SS}-0.3$ to $V_{SS}+7.0$	V
Input voltage	V_{IN}	All input pins	$V_{SS}-0.3$ to $V_{DD}+0.3$	V
Output voltage	V_{OUT}		$V_{SS}-0.3$ to $V_{DD}+0.3$	V
Allowable power dissipation	$P_d \text{ max}$	$T_a = 25^\circ\text{C}$	300	mW
Operating temperature	T_{opr}		-30 to +70	$^\circ\text{C}$
Storage temperature	T_{stg}		-40 to +125	$^\circ\text{C}$

Allowable Operating Ranges

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD1}	V_{DD1}	4.5	5.0	5.5	V
	V_{DD2}	V_{DD2}	4.5	5.0	$1.27 V_{DD1}$	V
Input high-level voltage	V_{IH}	\overline{CS} , SIN, \overline{RST} , SCLK, and SEP_{IN}	$0.8 V_{DD1}$		$V_{DD1} + 0.3$	V
Input low-level voltage	V_{IL}	\overline{CS} , SIN, \overline{RST} , SCLK, and SEP_{IN}	$V_{SS} - 0.3$		$0.2 V_{DD1}$	V
Composite video input voltage	V_{IN1}	CV_{IN}		2 Vp-p		V
	V_{IN2}	SYN_{IN}		2 Vp-p	$2.5 V_{p-p}$	V
Oscillator frequency	f_{OSC1}	Crystal oscillator pins (NTSC: 2fsc mode)		7.15909		MHz
	f_{OSC2}	Crystal oscillator pins (NTSC: 4fsc mode)		14.31818		MHz
	f_{OSC3}	Crystal oscillator pins (PAL: 4fsc mode)		17.73447		MHz
	f_{OSC4}	Crystal oscillator pins (PAL-M: 4fsc mode)		14.30244		MHz
	f_{OSC5}	Crystal oscillator pins (PAL-N: 4fsc mode)		14.32822		MHz
	f_{OSC6}	LC oscillator pin (When an LC oscillator is used)		5	7	11

Electrical Characteristics at $T_a = -30$ to $+70^\circ\text{C}$, $V_{DD1} = 5$ V unless otherwise specified

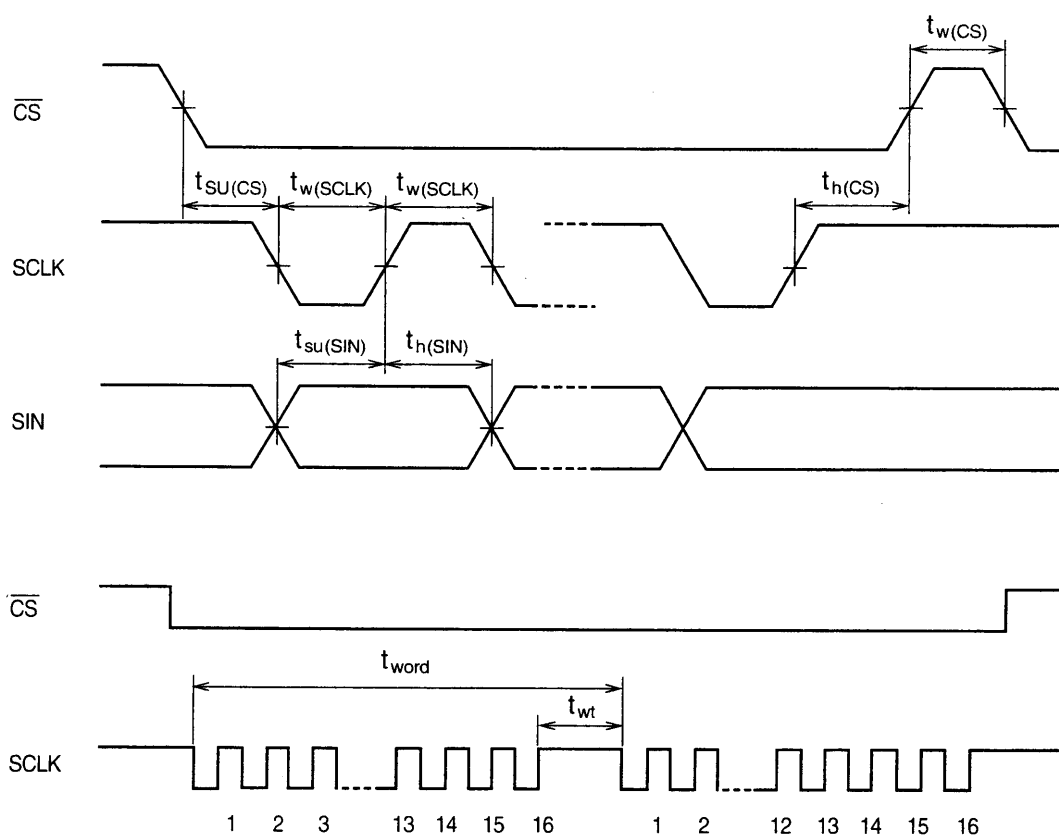
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Output off leakage current	I_{leak}	CV_{OUT}			10	μA
Output high-level voltage	V_{OH1}	SEP_{OUT} : $V_{DD1} = 4.5$ V, $I_{OH} = -1.0$ mA	3.5			V
Output low-level voltage	V_{OL1}	SEP_{OUT} : $V_{DD1} = 4.5$ V, $I_{OL} = 1.0$ mA			1.0	V
Input current	I_{IH}	\overline{CS} , SIN, \overline{RST} , SCLK, and SEP_{IN} : $V_{IN} = V_{DD1}$			1	μA
	I_{IL}	OSC_{IN} : $V_{IN} = V_{SS}$	-1			μA
Operating current drain	I_{DD1}	V_{DD1} : All outputs open, Xtal: 17.734MHz, LC = 7MHz			10	mA
	I_{DD2}	V_{DD2} : $V_{DD2} = 5.0$ V			15	mA

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Timing Characteristics at $T_a = -30$ to $+70^\circ\text{C}$, $V_{DD1} = 5 \pm 0.5\text{ V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Minimum input pulse width	$t_{w(\text{SCLK})}$	SCLK	200			ns
	$t_{w(\text{CS})}$	$\overline{\text{CS}}$ (the period when $\overline{\text{CS}}$ is high)	1			μs
Data setup time	$t_{\text{SU}(\text{CS})}$	$\overline{\text{CS}}$	200			ns
	$t_{\text{SU}(\text{SIN})}$	SIN	200			ns
Data hold time	$t_{\text{H}(\text{CS})}$	$\overline{\text{CS}}$	2			μs
	$t_{\text{H}(\text{SIN})}$	SIN	200			ns
One-word write time	t_{word}	The time to write 16 bits of data	10			μs
	t_{wt}	The time to write data to RAM	1			μs

Serial Data Input Timing



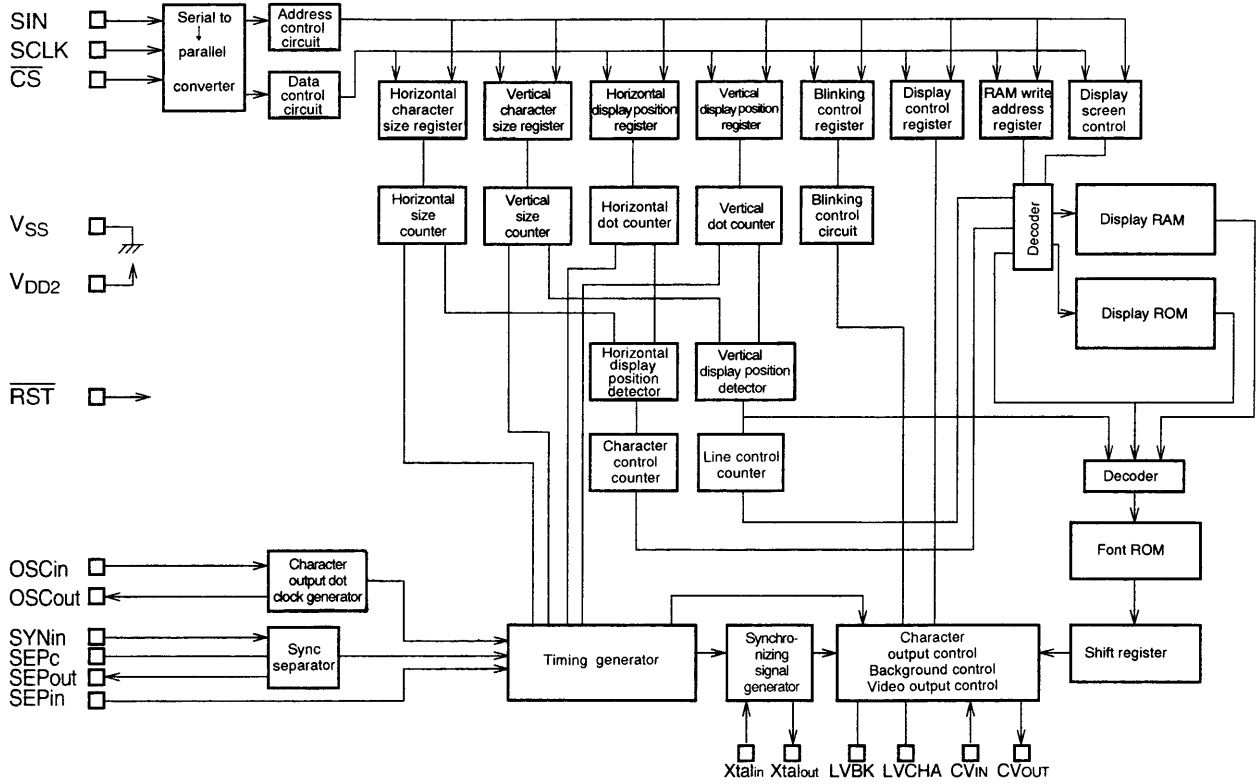
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Pin Functions

Pin no.	Pin	Function	Notes
1	V _{SS}	Ground	Ground (digital system ground)
2	Xtal _{IN}	Crystal oscillator	Connections for the crystal and capacitors used to form the crystal oscillator for generating internal synchronizing signals.
3	Xtal _{OUT}		
4	TEST	Test output	Test data output
5	RST	Reset input	System reset input (This input has hysteresis characteristics.)
6	SCLK	Clock input	Clock input for the serial data input function (This input has hysteresis characteristics.)
7	SIN	Data input	Serial data input (This input has hysteresis characteristics.) Data is input in 16-bit units.
8	CS	Enable input	Serial data input enable input (This input has hysteresis characteristics.) Serial data input is enabled when this pin is low.
9	LVBK	Blanking level adjustment input	Level input signal used to adjust the blanking level.
10	LVCHA	Character level adjustment input	Level input signal used to adjust the character level.
11	V _{DD2}	Power supply	Composite video signal adjustment power supply (analog system power supply)
12	CV _{OUT}	Video signal output	Composite video signal output
13	NC		This pin must be either connected to ground or left open.
14	CV _{IN}	Video signal input	Composite video signal input
15	V _{DD1}	Power supply	Power supply (+5 V)
16	SYN _{IN}	Sync separator circuit input	Input to the composite sync signal sync separator circuit
17	SEP _C	Sync separator circuit adjustment	Sync separator circuit adjustment
18	SEP _{OUT}	Composite sync signal output	Sync separator circuit composite sync signal output
19	SEP _{IN}	Vertical synchronizing signal input	Connect an integration circuit between the SEP _{OUT} pin and this pin, which inputs the vertical synchronizing signal, to integrate the output signal from the SEP _{OUT} pin.
20	OSC _{OUT}	LC oscillator	Connections for the coil and capacitor that form the oscillator used to generate the character output dot clock.
21	OSC _{IN}		
22	V _{DD1}	Power supply (+5 V)	Power supply (+5 V)

System Block Diagram



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Display Screen Structure

The display mode has a 24-character by 12-row format.

The maximum number of characters that can be displayed is 288.

When character sizes are enlarged, the maximum number of characters that can be displayed is reduced.

Display ROM (12-line specification) and display RAM (for 176 characters)

- Specify fixed characters in the display line ROM.
- Application programs use the display RAM to specify characters for sections of the display in which the characters change.

		← 24 characters →																							
12 lines		00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23
		24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
		48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71
		72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
		96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119
		120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143
		144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167
		168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191
		192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215
		216	217	218	219	220	221	222	223	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239
		240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255	256	257	258	259	260	261	262	263
		264	265	266	267	268	269	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287

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Memory Organization (display RAM and control RAM)

Both memory addresses and data are 16-bit quantities.

The locations at addresses 000 (000 hexadecimal) to 175 (0AF hexadecimal) hold display memory (RAM) data.

The locations at addresses 176 (0B0 hexadecimal) to 191 (0BF hexadecimal) hold display control register data.

Bit Address	DA F	DA E	DA D	DA C	DA B	DA A	DA 9	DA 8	DA 7	DA 6	DA 5	DA 4	DA 3	DA 2	DA 1	DA 0	Notes
000 (000h)	0	0	0	0	0	0	0	0	ATTR	C6	C5	C4	C3	C2	C1	C0	Display RAM
↓	ATTR									Character code							
175 (0AFh)	0	0	0	0	0	0	0	0	ATTR	C6	C5	C4	C3	C2	C1	C0	
176 (0B0h)	0	0	0	0	0	ADR A	ADR 9	ADR 8	ADR 7	ADR 6	ADR 5	ADR 4	ADR 3	ADR 2	ADR 1	ADR 0	Display line ROM specification First character in the first line
177 (0B1h)	0	0	0	0	0	ADR A	ADR 9	ADR 8	ADR 7	ADR 6	ADR 5	ADR 4	ADR 3	ADR 2	ADR 1	ADR 0	Display line ROM specification First character in the second line
178 (0B2h)	0	0	0	0	0	ADR A	ADR 9	ADR 8	ADR 7	ADR 6	ADR 5	ADR 4	ADR 3	ADR 2	ADR 1	ADR 0	Display line ROM specification First character in the third line
179 (0B3h)	0	0	0	0	0	ADR A	ADR 9	ADR 8	ADR 7	ADR 6	ADR 5	ADR 4	ADR 3	ADR 2	ADR 1	ADR 0	Display line ROM specification First character in the fourth line
180 (0B4h)	0	0	0	0	0	ADR A	ADR 9	ADR 8	ADR 7	ADR 6	ADR 5	ADR 4	ADR 3	ADR 2	ADR 1	ADR 0	Display line ROM specification First character in the fifth line
181 (0B5h)	0	0	0	0	0	ADR A	ADR 9	ADR 8	ADR 7	ADR 6	ADR 5	ADR 4	ADR 3	ADR 2	ADR 1	ADR 0	Display line ROM specification First character in the sixth line
182 (0B6h)	0	0	0	0	0	ADR A	ADR 9	ADR 8	ADR 7	ADR 6	ADR 5	ADR 4	ADR 3	ADR 2	ADR 1	ADR 0	Display line ROM specification First character in the seventh line
183 (0B7h)	0	0	0	0	0	ADR A	ADR 9	ADR 8	ADR 7	ADR 6	ADR 5	ADR 4	ADR 3	ADR 2	ADR 1	ADR 0	Display line ROM specification First character in the eighth line
184 (0B8h)	0	0	0	0	0	ADR A	ADR 9	ADR 8	ADR 7	ADR 6	ADR 5	ADR 4	ADR 3	ADR 2	ADR 1	ADR 0	Display line ROM specification First character in the ninth line
185 (0B9h)	0	0	0	0	0	ADR A	ADR 9	ADR 8	ADR 7	ADR 6	ADR 5	ADR 4	ADR 3	ADR 2	ADR 1	ADR 0	Display line ROM specification First character in the tenth line
186 (0BAh)	0	0	0	0	0	ADR A	ADR 9	ADR 8	ADR 7	ADR 6	ADR 5	ADR 4	ADR 3	ADR 2	ADR 1	ADR 0	Display line ROM specification First character in the eleventh line
187 (0BBh)	0	0	0	0	0	ADR A	ADR 9	ADR 8	ADR 7	ADR 6	ADR 5	ADR 4	ADR 3	ADR 2	ADR 1	ADR 0	Display line ROM specification First character in the twelfth line
188 (0BCh)	0	0	0	0	HSZ 31	HSZ 30	HSZ 21	HSZ 20	HSZ 11	HSZ 10	HP5	HP4	HP3	HP2	HP1	HP0	Horizontal display position Horizontal character size
189 (0BDh)	0	0	0	0	VSZ 31	VSZ 30	VSZ 21	VSZ 20	VSZ 11	VSZ 10	VP5	VP4	VP3	VP2	VP1	VP0	Vertical display position Vertical character size
190 (0BEh)	0	0	0	0	INT/ NON	LC/ XTAL	2fsc/ 4fsc	OSC STP	DSP ON	MUTE	SYS RST	SIG MD1	SIG MD0	PHASE 2	PHASE 1	PHASE 0	Video signal and other items
191 (0BFh)	0	0	0	0	TST MOD	VSN SEP	0	BLK 1	BLK 0	RVS ON	BLINK 2	BLINK 1	BLINK 0	EXT/ INT	CBOFF	BCOL	Control register

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Address 188 (OBC hexadecimal)

DA 0 to C	Register	Contents		Notes									
		State	Function										
0	HP0 (LSB)	0	If HS is the horizontal start position then: $HS = T_c \times (4 \sum_{n=0}^5 HP_n)$ Tc: Period of the oscillator connected to OSCIN/OSCOU in operating mode.	The 6 bits HP5:0 specify the horizontal display start position. The weight of the low order bit is 4·Tc.									
		1											
1	HP1	0											
		1											
2	HP2	0											
		1											
3	HP3	0											
		1											
4	HP4	0											
		1											
5	HP5 (MSB)	0											
		1											
6	HSZ10	0	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td style="text-align: center;">HSZ10 HSZ11</td> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1 Tc/dot</td> <td style="text-align: center;">2 Tc/dot</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">3 Tc/dot</td> <td style="text-align: center;">4 Tc/dot</td> </tr> </table>	HSZ10 HSZ11	0	1	0	1 Tc/dot	2 Tc/dot	1	3 Tc/dot	4 Tc/dot	The horizontal character size for line 1
		HSZ10 HSZ11		0	1								
0	1 Tc/dot	2 Tc/dot											
1	3 Tc/dot	4 Tc/dot											
1													
7	HSZ11	0											
		1											
8	HSZ20	0	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td style="text-align: center;">HSZ20 HSZ21</td> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1 Tc/dot</td> <td style="text-align: center;">2 Tc/dot</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">3 Tc/dot</td> <td style="text-align: center;">4 Tc/dot</td> </tr> </table>	HSZ20 HSZ21	0	1	0	1 Tc/dot	2 Tc/dot	1	3 Tc/dot	4 Tc/dot	The horizontal character size for line 2
		HSZ20 HSZ21		0	1								
0	1 Tc/dot	2 Tc/dot											
1	3 Tc/dot	4 Tc/dot											
1													
9	HSZ21	0											
		1											
A	HSZ30	0	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td style="text-align: center;">HSZ30 HSZ31</td> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1 Tc/dot</td> <td style="text-align: center;">2 Tc/dot</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">3 Tc/dot</td> <td style="text-align: center;">4 Tc/dot</td> </tr> </table>	HSZ30 HSZ31	0	1	0	1 Tc/dot	2 Tc/dot	1	3 Tc/dot	4 Tc/dot	The horizontal character size for lines 2 through 12
		HSZ30 HSZ31		0	1								
0	1 Tc/dot	2 Tc/dot											
1	3 Tc/dot	4 Tc/dot											
1													
B	HSZ31	0											
		1											

Note: The states of all registers are set to zero when the IC is reset by the \overline{RST} pin.

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Address 189 (OBD hexadecimal)

DA 0 to C	Register	Contents		Notes										
		State	Function											
0	VP0 (LSB)	0	If VS is the vertical display start position then: $VS = H \times (4 \sum_{n=0}^5 VP_n)$	The 6 bits VP5:0 specify the vertical display start position. The weight of the low order bit is 4·H.										
		1												
1	VP1	0	H: the horizontal synchronization pulse period											
		1												
2	VP2	0	<p style="text-align: center;">HSYNC</p> <p style="text-align: center;">VS</p> <p style="text-align: center;">HS</p> <p style="text-align: center;">Character display area</p>											
		1												
3	VP3	0												
		1												
4	VP4	0												
		1												
5	VP5 (MSB)	0												
		1												
6	VSZ10	0		<table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td style="text-align: center;">VSZ10 VSZ11</td> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1 H/dot</td> <td style="text-align: center;">2 H/dot</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">3 H/dot</td> <td style="text-align: center;">4 H/dot</td> </tr> </table>	VSZ10 VSZ11	0	1	0	1 H/dot	2 H/dot	1	3 H/dot	4 H/dot	The vertical character size for line 1
		VSZ10 VSZ11			0	1								
0	1 H/dot	2 H/dot												
1	3 H/dot	4 H/dot												
1														
7	VSZ11	0												
		1												
8	VSZ20	0	<table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td style="text-align: center;">VSZ20 VSZ21</td> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1 H/dot</td> <td style="text-align: center;">2 H/dot</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">3 H/dot</td> <td style="text-align: center;">4 H/dot</td> </tr> </table>	VSZ20 VSZ21	0	1	0	1 H/dot	2 H/dot	1	3 H/dot	4 H/dot	The vertical character size for line 2	
		VSZ20 VSZ21		0	1									
0	1 H/dot	2 H/dot												
1	3 H/dot	4 H/dot												
1														
9	VSZ21	0												
		1												
A	VSZ30	0	<table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td style="text-align: center;">VSZ30 VSZ31</td> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1 H/dot</td> <td style="text-align: center;">2 H/dot</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">3 H/dot</td> <td style="text-align: center;">4 H/dot</td> </tr> </table>	VSZ30 VSZ31	0	1	0	1 H/dot	2 H/dot	1	3 H/dot	4 H/dot	The vertical character size for lines 3 through 12	
		VSZ30 VSZ31		0	1									
0	1 H/dot	2 H/dot												
1	3 H/dot	4 H/dot												
1														
B	VSZ31	0												
		1												

Note: The states of all registers are set to zero when the IC is reset by the \overline{RST} pin.

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Address 190 (OBE hexadecimal)

DA 0 to C	Register	Contents				Notes																																																
		State	Function																																																			
0	PHASE0	0	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th rowspan="2">PHASE2</th> <th rowspan="2">PHASE1</th> <th rowspan="2">PHASE0</th> <th colspan="2">Background color (phase)</th> </tr> <tr> <th>NTSC</th> <th>PAL (PAL-M, N)</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>$\pi/2$</td> <td>$\pm \pi/2$</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>π</td> <td>In phase</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>$3\pi/2$</td> <td>$\mp \pi/2$</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>In phase</td> <td>$\pm \pi$</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>$\pi/4$</td> <td>$\pm 3\pi/4$</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>$3\pi/4$</td> <td>$\pm \pi/4$</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>$5\pi/4$</td> <td>$\mp \pi/4$</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>$7\pi/4$</td> <td>$\pm 3\pi/4$</td> </tr> </tbody> </table>				PHASE2	PHASE1	PHASE0	Background color (phase)		NTSC	PAL (PAL-M, N)	0	0	0	$\pi/2$	$\pm \pi/2$	0	0	1	π	In phase	0	1	0	$3\pi/2$	$\mp \pi/2$	0	1	1	In phase	$\pm \pi$	1	0	0	$\pi/4$	$\pm 3\pi/4$	1	0	1	$3\pi/4$	$\pm \pi/4$	1	1	0	$5\pi/4$	$\mp \pi/4$	1	1	1	$7\pi/4$	$\pm 3\pi/4$	Background color The phase of the background color with respect to the color burst signal.
		PHASE2								PHASE1	PHASE0	Background color (phase)																																										
NTSC	PAL (PAL-M, N)																																																					
0	0	0					$\pi/2$	$\pm \pi/2$																																														
0	0	1					π	In phase																																														
0	1	0					$3\pi/2$	$\mp \pi/2$																																														
0	1	1					In phase	$\pm \pi$																																														
1	0	0					$\pi/4$	$\pm 3\pi/4$																																														
1	0	1					$3\pi/4$	$\pm \pi/4$																																														
1	1	0					$5\pi/4$	$\mp \pi/4$																																														
1	1	1	$7\pi/4$	$\pm 3\pi/4$																																																		
1	PHASE1	0																																																				
1	PHASE1	1																																																				
		0																																																				
2	PHASE2	0																																																				
		1																																																				
3	SIGMD0	0	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>SIGMD1</th> <th>SIGMD0</th> <th>Signal format</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>NTSC</td> </tr> <tr> <td>0</td> <td>1</td> <td>PAL</td> </tr> <tr> <td>1</td> <td>0</td> <td>PAL-M</td> </tr> <tr> <td>1</td> <td>1</td> <td>PAL-N</td> </tr> </tbody> </table>				SIGMD1	SIGMD0	Signal format	0	0	NTSC	0	1	PAL	1	0	PAL-M	1	1	PAL-N																																	
		SIGMD1					SIGMD0	Signal format																																														
0	0	NTSC																																																				
0	1	PAL																																																				
1	0	PAL-M																																																				
1	1	PAL-N																																																				
1																																																						
4	SIGMD1	0																																																				
		1																																																				
5	SYRST	0					The IC is reset by a low level on the \overline{CS} pin, and the reset state is cleared by a high level on that pin.																																															
		1	Resets all registers and turns display off.																																																			
6	MUTE	0	Normal output																																																			
		1	CV_{IN} is cut and CV_{OUT} is fixed at the pedestal level.																																																			
7	DSPON	0	Character display off																																																			
		1	Character display on																																																			
8	OSCSTP	0	Crystal oscillator and LC oscillator circuits are not stopped.				Only valid in external synchronization mode when character display is off.																																															
		1	Stops the crystal oscillator and LC oscillator circuits.																																																			
9	$\overline{2fsc}/$ $4fsc/$	0	Clock frequency: 2fsc				Crystal oscillator circuit frequency																																															
		1	Clock frequency: 4fsc																																																			
A	$\overline{LC}/$ XTAL	0	The LC oscillator is used for the dot clock.				The OSC_{IN} pin must be tied to V_{DD} if the LC oscillator circuit is not used.																																															
		1	The crystal oscillator is used for the dot clock.																																																			
B	$\overline{INT}/$ NON	0	Interlaced (262.5 H per field: NTSC, 312.5 H per field: PAL)				Switches interlaced and noninterlaced display.																																															
		1	Noninterlaced (263 H per field: NTSC, 313 H per field: PAL)																																																			

Note: The states of all registers are set to zero when the IC is reset by the \overline{RST} pin.

LC74751

Address 191 (OBF hexadecimal)

DA 0 to C	Register	Contents		Notes									
		State	Function										
0	BCOL	0	Background color provided (only valid in internal synchronization mode)										
		1	No background color (Only the background level is set)										
1	CBOFF	0	The burst signal is always output.										
		1	The burst signal is not output when BCOL is high.										
2	$\overline{\text{EXT}}/\text{INT}$	0	External synchronization	Switches between external and internal sources for the $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ signals.									
		1	Internal synchronization										
3	BLINK0	0	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td style="text-align: center;">BLINK0 BLINK1</td> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> </tr> <tr> <td style="text-align: center;">0</td> <td>Blinking off</td> <td>25% duty</td> </tr> <tr> <td style="text-align: center;">1</td> <td>50% duty</td> <td>75% duty</td> </tr> </table>	BLINK0 BLINK1	0	1	0	Blinking off	25% duty	1	50% duty	75% duty	Changes the blinking duty ratio.
BLINK0 BLINK1	0	1											
0	Blinking off	25% duty											
1	50% duty	75% duty											
1													
4	BLINK1	0											
1													
5	BLINK2	0	Blinking period: 0.5 s	Changes the blinking period.									
		1	Blinking period: 1.0 s										
6	RVSON	0	Reverse video off										
		1	Reverse video on										
7	BLK0	0	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td style="text-align: center;">BLK0 BLK1</td> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> </tr> <tr> <td style="text-align: center;">0</td> <td>Blinking off</td> <td>Character size</td> </tr> <tr> <td style="text-align: center;">1</td> <td>Frame size</td> <td>Whole area size</td> </tr> </table>	BLK0 BLK1	0	1	0	Blinking off	Character size	1	Frame size	Whole area size	Changes the blanking size
BLK0 BLK1	0	1											
0	Blinking off	Character size											
1	Frame size	Whole area size											
1													
8	BLK1	0											
1													
9	—	0											
		1											
A	VSNSEP	0	External V input used (SEP_{IN} : pin 19)	Selects V input when superimpose mode is used.									
		1	Internal V separation circuit used										
B	TSTMOD	0	Normal operating mode	This bit must be set to 0.									
		1	Test mode										

Note: The states of all registers are set to zero when the IC is reset by the $\overline{\text{RST}}$ pin.

LC74751

Memory (Display ROM) Organization

This memory has addresses ranging from 0 (000 hexadecimal) to 1535 (5FF hexadecimal).

Data has 8 bits.

Bit Address	DA	DA	DA	DA	DA	DA	DA	DA	DA	DA	DA	DA	DA	DA	DA	DA	Notes
	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0	
000 (000h)	0	0	0	0	0	0	0	0	ROM/ RAM	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Line ROM: First character in the first line
↓																	
0023 (017h)	0	0	0	0	0	0	0	0	ROM/ RAM	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Line ROM: 24th character in the first line
0024 (018h)	0	0	0	0	0	0	0	0	ROM/ RAM	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Line ROM: First character in the second line
↓																	
↓																	
1535 (5FFh)	0	0	0	0	0	0	0	0	ROM/ RAM	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Line ROM: 24th character in the 64th line

ROM/
RAM Character code

DA 0 to 8	Register	Contents		Notes		
		State	Function			
0	ADR0	0	Specifies an address in character ROM. When specifying display control RAM, DA7 must be set to 1 and ADR0 to ADR6 must be set to 0. The address specification range for character ROM is 0 to 127 (7F hexadecimal).			
		1				
1	ADR1	0				
		1				
2	ADR2	0				
		1				
3	ADR3	0				
		1				
4	ADR4	0				
		1				
5	ADR5	0				
		1				
6	ADR6	0				
		1				
7	ROM/ RAM	0			Data is read directly from character ROM.	
		1			Data is read from character ROM through RAM.	

Display Line ROM: Line Address Table



Line no.	Address	Line no.	Address
Line 1	000 _{HEX} (0000)	Line 33	300 _{HEX} (0768)
Line 2	018 _{HEX} (0024)	Line 34	318 _{HEX} (0792)
Line 3	030 _{HEX} (0048)	Line 35	330 _{HEX} (0816)
Line 4	048 _{HEX} (0072)	Line 36	348 _{HEX} (0840)
Line 5	060 _{HEX} (0096)	Line 37	360 _{HEX} (0864)
Line 6	078 _{HEX} (0120)	Line 38	378 _{HEX} (0888)
Line 7	090 _{HEX} (0144)	Line 39	390 _{HEX} (0912)
Line 8	0A8 _{HEX} (0168)	Line 40	3A8 _{HEX} (0936)
Line 9	0C0 _{HEX} (0129)	Line 41	3C0 _{HEX} (0960)
Line 10	0D8 _{HEX} (0216)	Line 42	3D8 _{HEX} (0984)
Line 11	0F0 _{HEX} (0240)	Line 43	3F0 _{HEX} (1008)
Line 12	108 _{HEX} (0264)	Line 44	408 _{HEX} (1032)
Line 13	120 _{HEX} (0288)	Line 45	420 _{HEX} (1056)
Line 14	138 _{HEX} (0312)	Line 46	438 _{HEX} (1080)
Line 15	150 _{HEX} (0336)	Line 47	450 _{HEX} (1104)
Line 16	168 _{HEX} (0360)	Line 48	468 _{HEX} (1128)
Line 17	180 _{HEX} (0384)	Line 49	480 _{HEX} (1152)
Line 18	198 _{HEX} (0408)	Line 50	498 _{HEX} (1176)
Line 19	1B0 _{HEX} (0432)	Line 51	4B0 _{HEX} (1200)
Line 20	1C8 _{HEX} (0456)	Line 52	4C8 _{HEX} (1224)
Line 21	1E0 _{HEX} (0480)	Line 53	4E0 _{HEX} (1248)
Line 22	1F8 _{HEX} (0504)	Line 54	4F8 _{HEX} (1272)
Line 23	210 _{HEX} (0528)	Line 55	510 _{HEX} (1296)
Line 24	228 _{HEX} (0552)	Line 56	528 _{HEX} (1320)
Line 25	240 _{HEX} (0576)	Line 57	540 _{HEX} (1344)
Line 26	258 _{HEX} (0600)	Line 58	558 _{HEX} (1368)
Line 27	270 _{HEX} (0624)	Line 59	570 _{HEX} (1392)
Line 28	288 _{HEX} (0648)	Line 60	588 _{HEX} (1416)
Line 29	2A0 _{HEX} (0672)	Line 61	5A0 _{HEX} (1440)
Line 30	2B8 _{HEX} (0696)	Line 62	5B8 _{HEX} (1464)
Line 31	2D0 _{HEX} (0720)	Line 63	5D0 _{HEX} (1488)
Line 32	2E8 _{HEX} (0744)	Line 64	5E8 _{HEX} (1512)

Display Screen Structure (Display Example)

Specify the display of line 12 for display line ROM (64 lines).

From within line ROM, specify display control RAM for the sections where the characters are variable.

The addresses in display control RAM are automatically allocated in display order from 0 to 175 (AF hexadecimal).

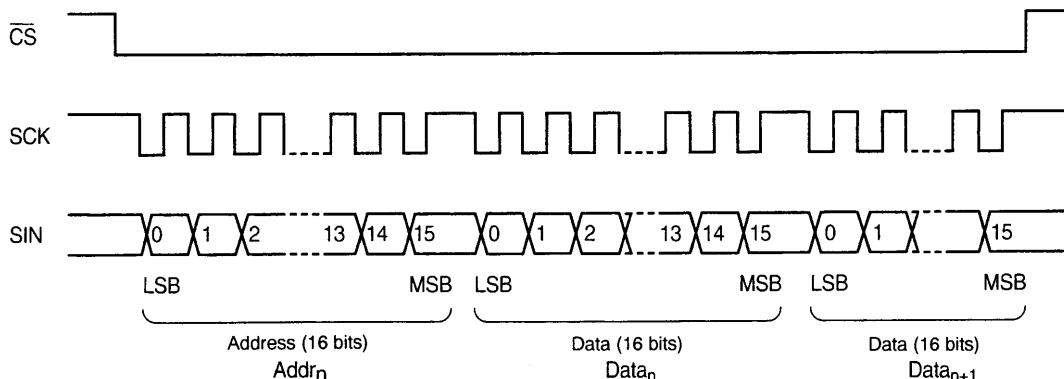
-  Items enclosed in thick lines specify characters in display control RAM, and
-  items enclosed in thin lines are character specified in line ROM.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24			
1	ROM 000 00h	ROM 001 01h	ROM 002 02h	ROM 003 03h	ROM 004 04h	ROM 005 05h	ROM 006 06h	ROM 007 07h	ROM 008 08h	ROM 009 09h	ROM 010 0Ah	ROM 011 0Bh	ROM 012 0Ch	ROM 013 0Dh	ROM 014 0Eh	ROM 015 0Fh	RAM 000 00h	RAM 001 01h	RAM 002 02h	RAM 003 03h	RAM 004 04h	RAM 005 05h	ROM 022 16h	ROM 023 17h			
2	ROM 024 18h	RAM 006 06h	RAM 007 07h	RAM 008 08h	RAM 009 09h	ROM 029 1Dh	ROM 030 1Eh	ROM 031 1Fh	ROM 032 20h	ROM 033 21h	RAM 016 0Ah	RAM 017 0Bh	RAM 018 0Ch	RAM 019 0Dh	RAM 020 0Eh	RAM 021 0Fh	ROM 040 28h	ROM 041 29h	ROM 042 2Ah	ROM 043 2Bh	ROM 044 2Ch	ROM 045 2Dh	ROM 046 2Eh	ROM 047 2Fh			
3	ROM 048 18h	RAM 016 10h	RAM 017 11h	RAM 018 12h	RAM 019 13h	RAM 020 14h	ROM 054 36h	ROM 055 37h	ROM 056 38h	ROM 057 39h	RAM 021 15h	RAM 022 16h	RAM 023 17h	RAM 024 18h	RAM 025 19h	RAM 026 1Ah	RAM 027 1Bh	RAM 028 1Ch	RAM 029 1Dh	RAM 030 1Eh	ROM 068 44h	ROM 069 45h	ROM 070 46h	ROM 071 47h			
4	ROM 072 48h	ROM 073 49h	ROM 074 4Ah	ROM 075 4Bh	ROM 076 4Ch	RAM 031 1Fh	RAM 032 20h	RAM 033 21h	RAM 034 22h	ROM 081 51h	RAM 035 23h	RAM 036 24h	RAM 037 25h	RAM 038 26h	RAM 039 27h	RAM 040 28h	RAM 041 29h	RAM 042 2Ah	RAM 043 2Bh	RAM 044 2Ch	RAM 045 2Dh	ROM 091 5Ch	ROM 092 5Dh	ROM 093 5Eh	ROM 094 5Fh		
5	ROM 096 60h	RAM 041 29h	RAM 042 2Ah	RAM 043 2Bh	RAM 044 2Ch	RAM 045 2Dh	RAM 046 2Eh	RAM 047 2Fh	RAM 048 30h	ROM 105 69h	RAM 049 31h	RAM 050 32h	RAM 051 33h	RAM 052 34h	RAM 053 35h	RAM 054 36h	RAM 055 37h	RAM 056 38h	RAM 057 39h	RAM 058 3Ah	RAM 059 3Bh	ROM 114 72h	ROM 115 73h	ROM 116 74h	ROM 117 75h	ROM 118 76h	ROM 119 77h
6	ROM 120 78h	RAM 055 3Fh	RAM 056 40h	RAM 057 41h	RAM 058 42h	RAM 059 43h	RAM 060 44h	RAM 061 45h	RAM 062 46h	ROM 128 80h	RAM 063 47h	RAM 064 48h	RAM 065 49h	RAM 066 4Ah	RAM 067 4Bh	RAM 068 4Ch	RAM 069 4Dh	RAM 070 4Eh	RAM 071 4Fh	RAM 072 50h	RAM 073 51h	ROM 139 87h	ROM 140 88h	ROM 141 89h	ROM 142 8Ah	ROM 143 8Bh	ROM 144 8Ch
7	RAM 073 48h	RAM 074 49h	RAM 075 4Ah	RAM 076 4Bh	RAM 077 4Ch	RAM 078 4Dh	RAM 079 4Eh	RAM 080 4Fh	RAM 081 50h	RAM 082 51h	RAM 083 52h	RAM 084 53h	RAM 085 54h	RAM 086 55h	RAM 087 56h	RAM 088 57h	RAM 089 58h	RAM 090 59h	RAM 091 5Ah	RAM 092 5Bh	RAM 093 5Ch	RAM 094 5Dh	RAM 095 5Eh	RAM 096 5Fh	RAM 097 60h	RAM 098 61h	RAM 099 62h
8	RAM 085 55h	RAM 086 56h	RAM 087 57h	RAM 088 58h	RAM 089 59h	RAM 090 5Ah	RAM 091 5Bh	RAM 092 5Ch	RAM 093 5Dh	RAM 094 5Eh	RAM 095 5Fh	RAM 096 60h	RAM 097 61h	RAM 098 62h	RAM 099 63h	RAM 100 64h	RAM 101 65h	RAM 102 66h	RAM 103 67h	RAM 104 68h	RAM 105 69h	RAM 106 6Ah	RAM 107 6Bh	RAM 108 6Ch	RAM 109 6Dh	RAM 110 6Eh	RAM 111 6Fh
9	ROM 192 C0h	ROM 193 C1h	ROM 194 C2h	ROM 195 C3h	ROM 196 C4h	ROM 197 C5h	ROM 198 C6h	ROM 199 C7h	ROM 200 C8h	ROM 201 C9h	ROM 202 CAh	ROM 203 CBh	RAM 097 61h	RAM 098 62h	RAM 099 63h	RAM 100 64h	RAM 101 65h	RAM 102 66h	RAM 103 67h	RAM 104 68h	RAM 105 69h	RAM 106 6Ah	RAM 107 6Bh	RAM 108 6Ch	RAM 109 6Dh	RAM 110 6Eh	RAM 111 6Fh
10	ROM 216 D8h	ROM 217 D9h	ROM 218 DAh	ROM 219 DBh	ROM 220 DCh	RAM 109 6Dh	RAM 110 6Eh	RAM 111 6Fh	RAM 112 70h	RAM 113 71h	RAM 114 72h	RAM 115 73h	RAM 116 74h	RAM 117 75h	RAM 118 76h	RAM 119 77h	RAM 120 78h	RAM 121 79h	RAM 122 7Ah	RAM 123 7Bh	RAM 124 7Ch	RAM 125 7Dh	RAM 126 7Eh	RAM 127 7Fh	RAM 128 80h	RAM 129 81h	RAM 130 82h
11	ROM 240 F0h	ROM 241 F1h	ROM 242 F2h	ROM 243 F3h	ROM 244 F4h	ROM 245 F5h	ROM 246 F6h	ROM 247 F7h	ROM 248 F8h	ROM 249 F9h	ROM 250 FAh	ROM 251 FBh	ROM 252 FCh	ROM 253 FDh	ROM 254 FEh	RAM 123 7Bh	RAM 124 7Ch	RAM 125 7Dh	RAM 126 7Eh	RAM 127 7Fh	RAM 128 80h	RAM 129 81h	RAM 130 82h	RAM 131 83h	RAM 132 84h	RAM 133 85h	RAM 134 86h
12	RAM 129 81h	RAM 130 82h	RAM 131 83h	RAM 132 84h	RAM 133 85h	RAM 134 86h	RAM 135 87h	RAM 136 88h	RAM 137 89h	RAM 138 8Ah	RAM 139 8Bh	RAM 140 8Ch	RAM 141 8Dh	RAM 142 8Eh	RAM 143 8Fh	RAM 144 90h	RAM 145 91h	RAM 146 92h	RAM 147 93h	RAM 148 94h	RAM 149 95h	RAM 150 96h	RAM 151 97h	RAM 152 98h	RAM 153 99h	RAM 154 9Ah	RAM 155 9Bh

Control Data External Input Timing

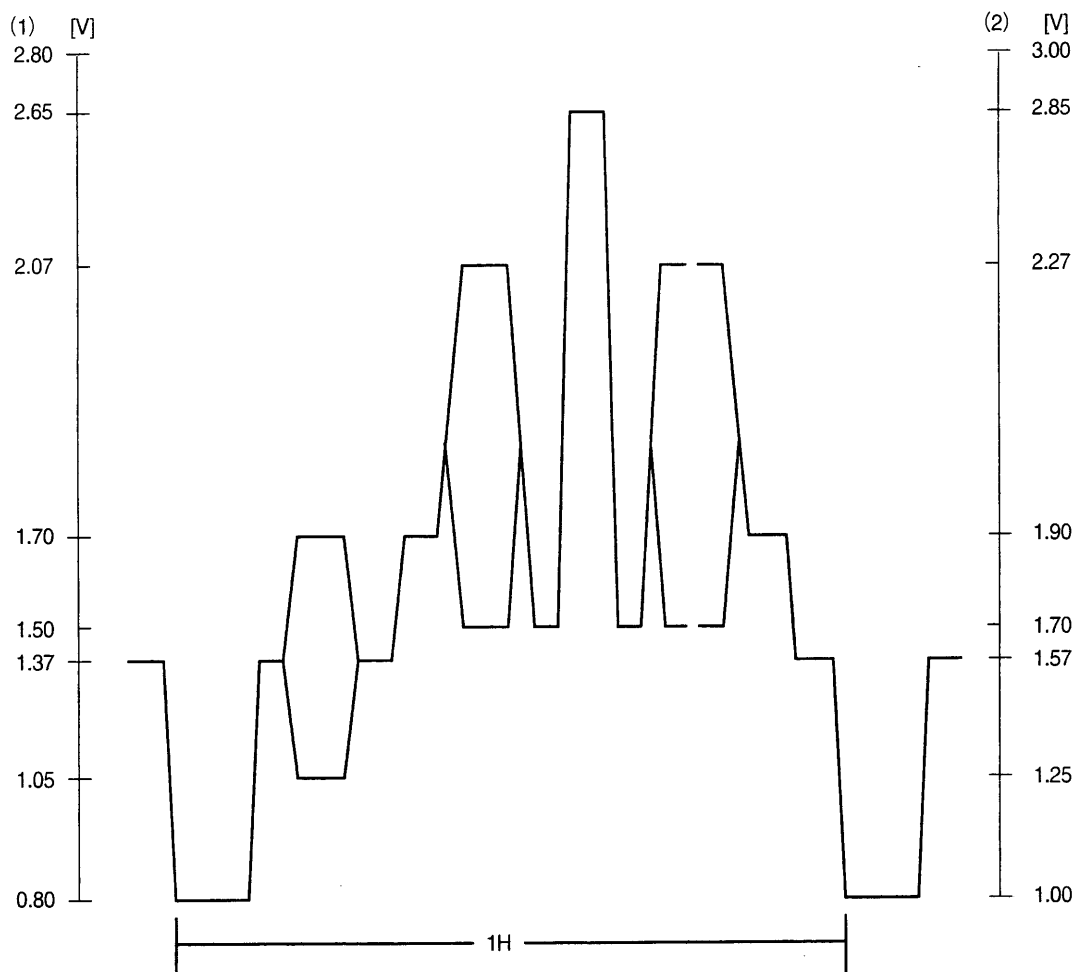
Data is input in a 16-bit serial format that includes both an address and data items.

- ①An address has 16 bits.
 - The lower 8 bits are the valid address bits. The upper 8 bits must be set to 0.
- ②Data consists of 16 bits.
 - For addresses 0B0 to 0BB (hexadecimal) the lower 11 bits are valid data. The upper 5 bits must be set to 0.
 - For addresses 0BC to 0BF (hexadecimal) the lower 12 bits are valid data. The upper 4 bits must be set to 0.
- ③When data is input, the first 16 bits after the fall of the CS signal are acquired as the address, and then data is acquired in 16-bit units. The address is automatically incremented ever 16 bits.



Composite Video Signal Output Levels (Internally Generated Levels)

CV_{OUT} output level waveform (V_{DD2} = 5.00 V)

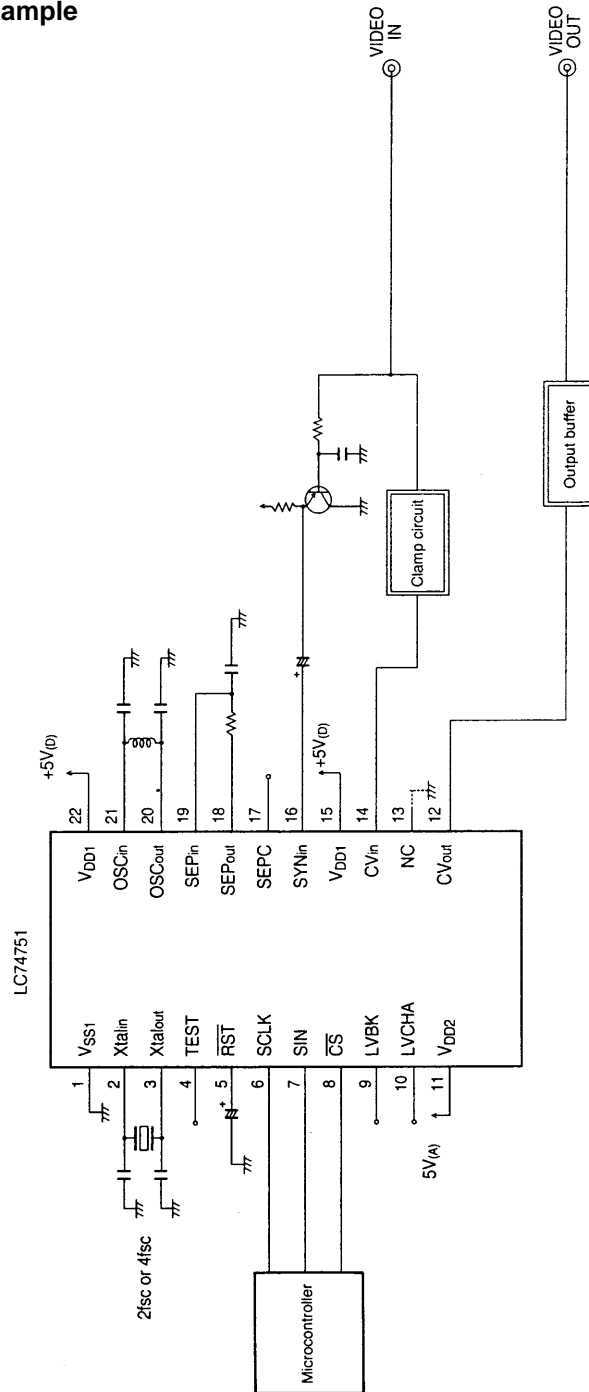


A05641

Output level	Output voltage (1) (V _{DC})	Output voltage (2) (V _{DC})
V _{CHA} : Character	2.650	2.875
V _{RSH} : Background color high	2.075	2.275
V _{CBH} : Color burst high	1.700	1.900
V _{RSL} : Background color low	1.500	1.700
V _{BK} : Frame	1.500	1.700
V _{PD} : Pedestal level	1.375	1.575
V _{CBL} : Color burst low	1.050	1.250
V _{SN} : Sync	0.800	1.000

V_{DD2} = 5.000V_{DC}

Application Circuit Example



ACS642

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