



LC79400D

Dot Matrix LCD Driver

Overview

The LC79400D is a large-scale dot matrix LCD segment driver LSI. Display data transferred from the controller (4-bit parallel format) is processed through 80-bit latching and a LCD drive signal is generated. The LC79400D can be used in conjunction with common driver LC7943D (QIP80D) as well as LC79430D (QIP100D) and LC79431D (QIP100D) to drive a wide-screen LCD panel.

Features

- On-chip LCD drive circuit (80 bits)
- Display duty selection ranging from 1/64 to 1/256
- Supports use of chip disable pin for lower large panel power supply dissipation
- Supports externally supplied bias voltage
- Operating power supply voltage/operating temperature include

V_{DD} (logic block) : 5 V \pm 10 % / -20 to +75 °C

$V_{DD}-V_{EE}$ (LCD block) : 12 V to 32 V / -20 to +75°C

- Data transfer clock provides maximum 3.0 MHz and supports bidirectional shift
- 4-bit parallel data input
- CMOS process
- 100-pin flat plastic package

Specifications

Absolute Maximum Ratings at $T_a = 25 \pm 2^\circ\text{C}$, $V_{SS} = 0\text{ V}$

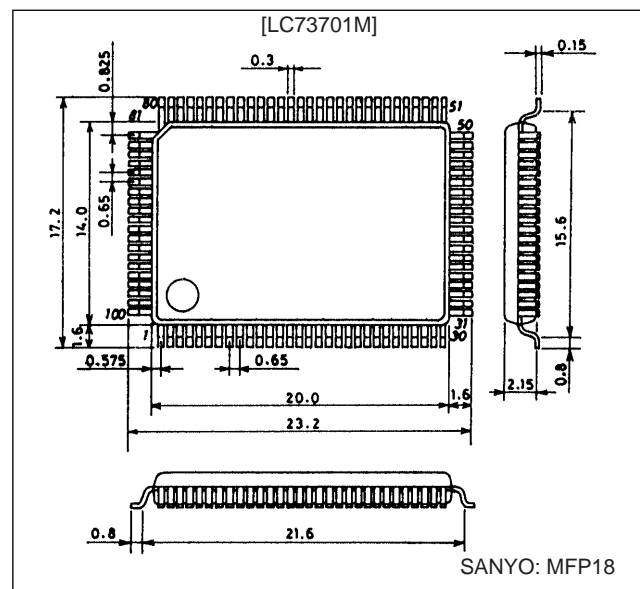
Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage (logic)	V_{DD} max		-0.3 to +7.0	V
Maximum supply voltage (LCD)	$V_{DD}-V_{EE}$ max*1		0 to 35	V
Maximum input voltage	V_I max		-0.3 to $V_{DD} + 0.3$	V
Storage temperature range	T_{stg}		-40 to +125	°C

Note: 1. The voltages V_1 , V_3 , V_4 , V_7 , V_{DD} and V_{EE} must obey the relationships: $V_{DD} \geq V_1 > V_3 > V_4 > V_{EE}$, $V_{DD} - V_3 \leq 7V$, $V_4 - V_{EE} \leq 7V$.

Package Dimensions

unit : mm

3180-QFP100D



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Allowable Operating Ranges at $T_a = -20$ to $+75^\circ\text{C}$, $V_{SS} = 0$ V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage (logic)	V_{DD}		4.5		5.5	V
Supply voltage (LCD)	$V_{DD} - V_{EE}$	*2, *3	12		32	V
Input high-level voltage	V_{IH}	DI1 to 4, CP, LOAD, CDR, CDL R/L, M, $\overline{\text{DISP OFF}}$	$0.8 V_{DD}$			V
Input low-level voltage	V_{IL}	DI1 to 4, CP, LOAD, CDR, CDL R/L, M, $\overline{\text{DISP OFF}}$			$0.2 V_{DD}$	V
CP (shift clock)	f_{CP}	CP			3.0	MHz
CP (pulse width)	t_{WC}	CP	100			ns
LOAD pulse width	t_{WL}	LOAD	100			ns
Setup time	t_{SETUP}	DI1 to 4 \rightarrow CP	80			ns
Hold time	t_{HOLD}	DI1 to 4 \rightarrow CP	80			ns
CP \rightarrow LOAD	t_{CL1}	CP \rightarrow LOAD	0			ns
	t_{CL2}	CP \rightarrow LOAD	100			ns
LOAD \rightarrow CP	t_{LC}	LOAD \rightarrow CP	63			ns
Rise/Fall time	t_R	CP			50	ns
	t_F	CP			50	ns
	t_{RL}	LOAD			50	ns
	t_{FL}	LOAD			50	ns

Note:2. The voltages V_1 , V_3 , V_4 , V_7 , V_{DD} and V_{EE} must obey the relationships: $V_{DD} \geq V_1 > V_3 > V_4 > V_{EE}$, $V_{DD} - V_3 \leq 7V$, $V_4 - V_{EE} \leq 7V$.

3. When applying power, apply power to the LCD drive block after applying power to the logic block or apply power to both the blocks simultaneously. When turning off power, turn off power to the logic block after turning off power to the LCD drive block or turn off power to both the blocks simultaneously.

Electrical Characteristics at $T_a = 25 \pm 2^\circ\text{C}$, $V_{SS} = 0$ V, $V_{DD} = 5$ V $\pm 10\%$

Parameter	Symbol	Conditions	min	typ	max	Unit
Input high-level current	I_{IH}	$V_{IN} = V_{DD}$; LOAD, CP, CDR (CDL), R/L, DI1 to DI4, M, $\overline{\text{DISP OFF}}$			1	μA
Input low-level current	I_{IL}	$V_{IN} = V_{SS}$; LOAD, CP, CDR (CDL), R/L, DI1 to DI4, M, $\overline{\text{DISP OFF}}$	-1			μA
Output high-level voltage	V_{OH}	$I_{OH} = -400 \mu\text{A}$; CDL (CDR)	$V_{DD} - 0.4$			V
Output low-level voltage	V_{OL}	$I_{OL} = 400 \mu\text{A}$; CDL (CDR)			0.4	V
Driver on resistor	R_{ON1}	$V_{DD} - V_{EE} = 30$ V, $ V_{DE} - V_O = 0.5$ V*4; O1 to O80		1.5	3.0	k Ω
	R_{ON2}	$V_{DD} - V_{EE} = 20$ V, $ V_{DE} - V_O = 0.5$ V*4; O1 to O80		2.0	3.5	k Ω
Standby current dissipation	I_{ST}	CDR (CDL) = V_{DD} ; $V_{DD} - V_{EE} = 30$ V CP = 3.0 MHz, no-load output: V_{SS}			200	μA
Operation current dissipation	I_{SS}^{*5}	$V_{DD} - V_{EE} = 30$ V, CP = 3 MHz, LOAD = 14 kHz, M = 35 Hz; V_{SS}			4.0	mA
	I_{SS}^{*6}	$V_{DD} - V_{EE} = 30$ V, CP = 3 MHz, LOAD = 14 kHz, M = 35 Hz; V_{EE}			0.1	mA
Input capacity	C_1	$f = 3.0$ MHz; CP		5		pF

Note:4. $V_{DE} = V_1$ or V_3 or V_4 or V_{EE} , $V_1 = V_{DD}$, $V_3 = 15/17 (V_{DD} - V_{EE})$, $V_4 = 2/17 (V_{DD} - V_{EE})$

5. I_{SS} current flows from V_{DD} to V_{SS} .

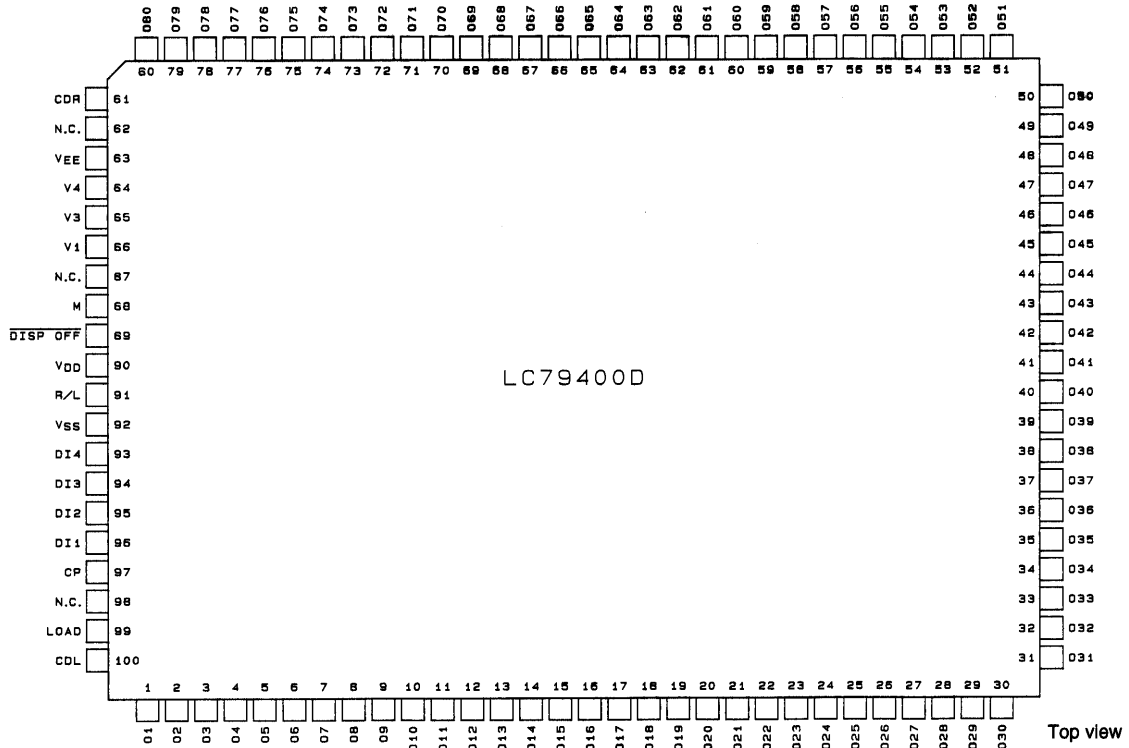
6. I_{EE} current flows from V_{DD} to V_{EE} .

Switching Characteristics at $T_a = 25 \pm 2^\circ\text{C}$, $V_{SS} = 0$ V, $V_{DD} = 5$ V $\pm 10\%$

Parameter	Symbol	Conditions	min	typ	max	Unit
Output delay time	t_D	Load = 15 pF; CDR (CDL)			200	ns

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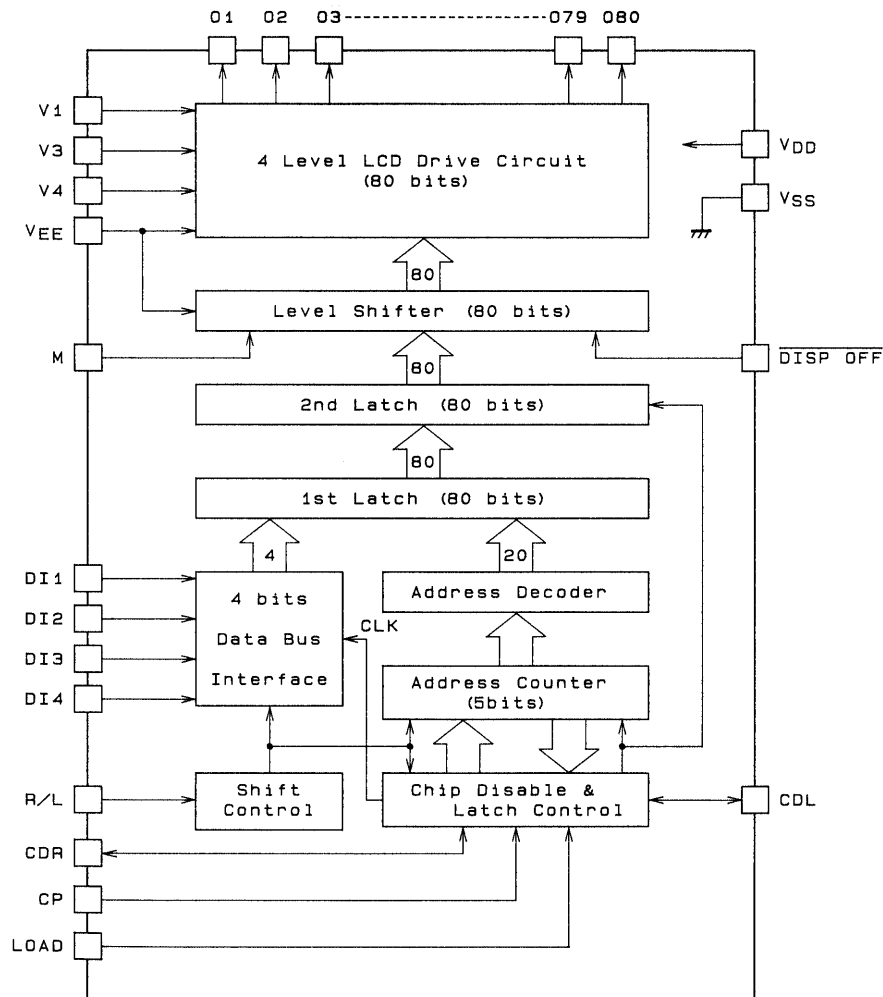
Pin Assignment



Top view

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Equivalent Circuit Block Diagram



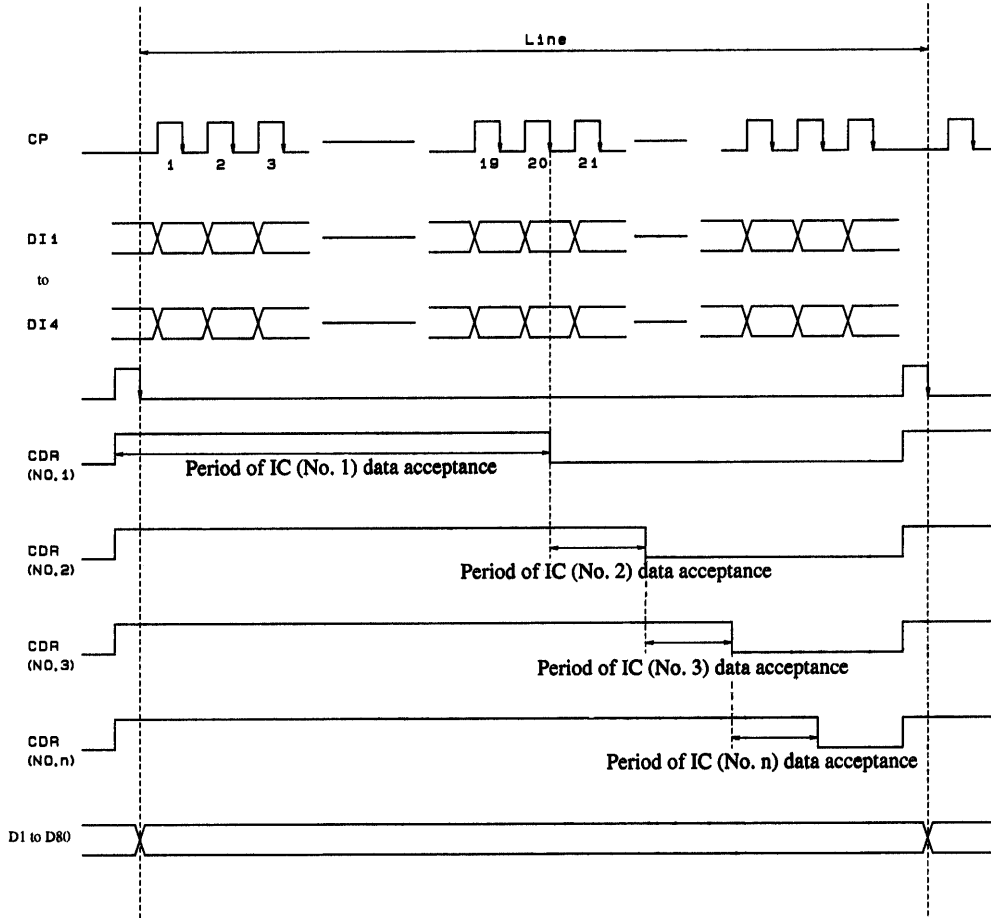
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Pin Descriptions

Pin No	Pin name	Input/Output	Functions																								
90	V _{DD}	Power supply	V _{DD} and V _{SS} : Power supply for logic section																								
92	V _{SS}																										
83	V _{EE}		V _{DD} and V _{EE} : Power supply for LCD drive circuit																								
86	V1	Power supply	LCD drive level power supply																								
85	V3		V1 and V _{EE} : Select level																								
84	V4		V3 and V4: Nonselect level																								
97	CP	Input	Display data shift clock (triggering on the trailing edge)																								
81	CDR	Input/Output	Chip disable pin H level: Data not accepted L level: Data accepted																								
100	CDL	Input/Output																									
			<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">Pin Name</th> <th style="width: 15%;">Input/Output</th> <th style="width: 10%;">R/L</th> <th style="width: 60%;">Pin Description</th> </tr> </thead> <tbody> <tr> <td>CDR</td> <td style="text-align: center;">Input</td> <td rowspan="2" style="text-align: center;">L</td> <td>Control input pin for the IC's internal disable F/F.</td> </tr> <tr> <td>CDL</td> <td style="text-align: center;">Output</td> <td>Output pin of the IC's internal disable F/F. Connects to the next stage CDR pin when establishing a cascade connection.</td> </tr> <tr> <td>CDL</td> <td style="text-align: center;">Input</td> <td rowspan="2" style="text-align: center;">H</td> <td>Control input pin for the IC's internal disable F/F.</td> </tr> <tr> <td>CDR</td> <td style="text-align: center;">Output</td> <td>Output pin of the IC's internal disable F/F. Connects to the next stage CDL pin when establishing a cascade connection.</td> </tr> </tbody> </table>	Pin Name	Input/Output	R/L	Pin Description	CDR	Input	L	Control input pin for the IC's internal disable F/F.	CDL	Output	Output pin of the IC's internal disable F/F. Connects to the next stage CDR pin when establishing a cascade connection.	CDL	Input	H	Control input pin for the IC's internal disable F/F.	CDR	Output	Output pin of the IC's internal disable F/F. Connects to the next stage CDL pin when establishing a cascade connection.						
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99	LOAD	Input	Display data latch clock (triggering on the trailing edge). On the trailing edge, output levels switch in response to the particular combination of display data, M and DISP OFF signals.																								
93	DI4	Input	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 10%;">R/L</th> <th style="width: 90%;">Input data and latch address</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">L</td> <td> </td> </tr> <tr> <td style="text-align: center;">H</td> <td> </td> </tr> </tbody> </table>	R/L	Input data and latch address	L		H																			
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L																											
H																											
94	DI3																										
95	DI2																										
96	DI1																										
88	M	Input	LCD drive output alternating signal																								
91	R/L	Input	Input pin which performs input/output switching for CDR and CDL pins and directional shift for 4-bit parallel input data.																								
1	O1	Output	LCD drive output The combination of display data, M signal, and $\overline{\text{DISP OFF}}$ signal can be used to create output levels as shown below.																								
2	O2																										
...	...																										
79	O79																										
80	O80																										
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M	Q	$\overline{\text{DISP OFF}}$	Output																								
L	L	H	V3																								
L	H	H	V1																								
H	L	H	V4																								
H	H	H	V _{EE}																								
*	*	L	V1																								
89	$\overline{\text{DISP OFF}}$	Input	Input pin which controls output pins O1 to O80. V1 level is output from O1 to O80 pin output during the low level input interval (See logic table).																								

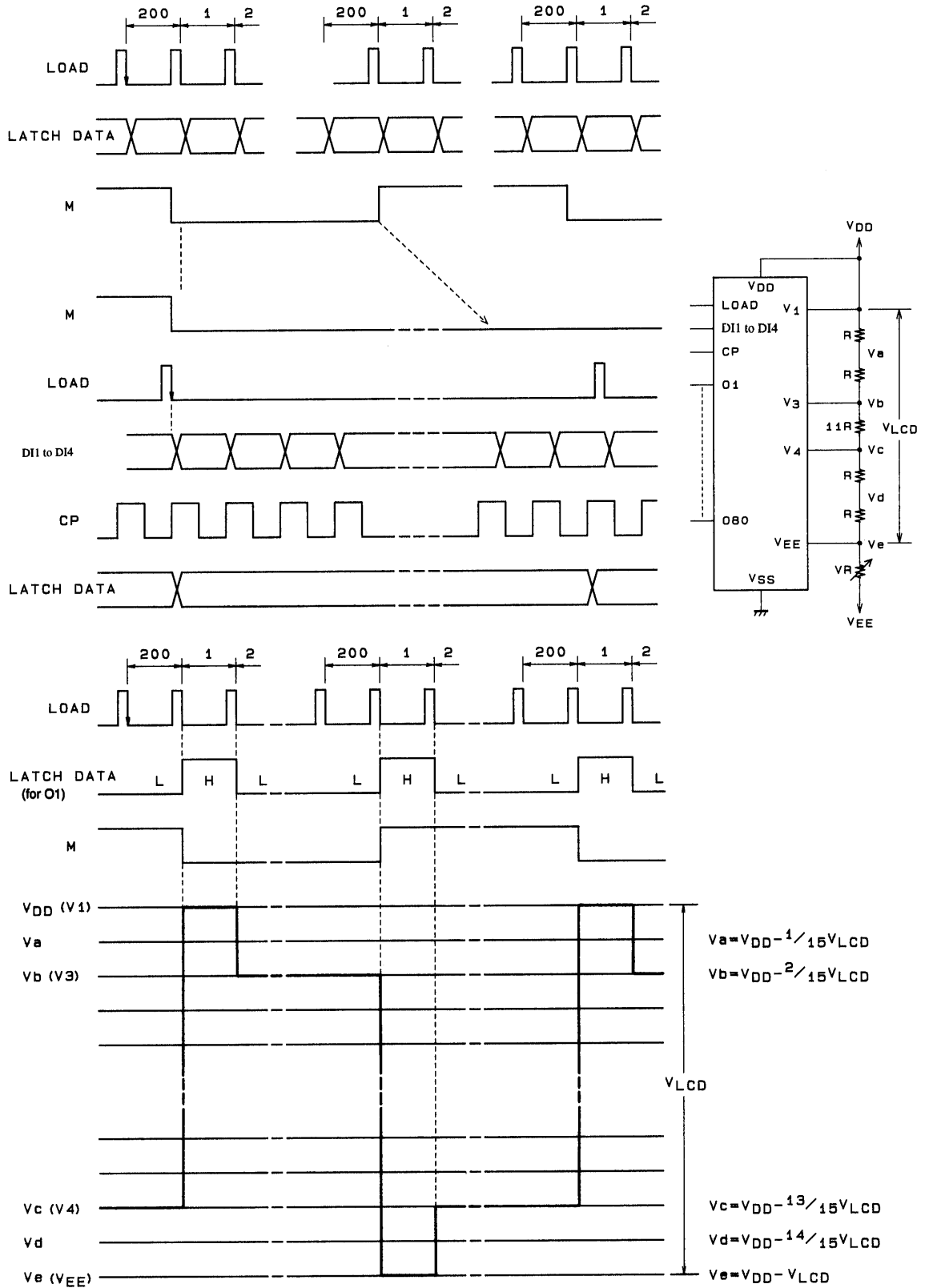
Operation Timing (for R/L = H)



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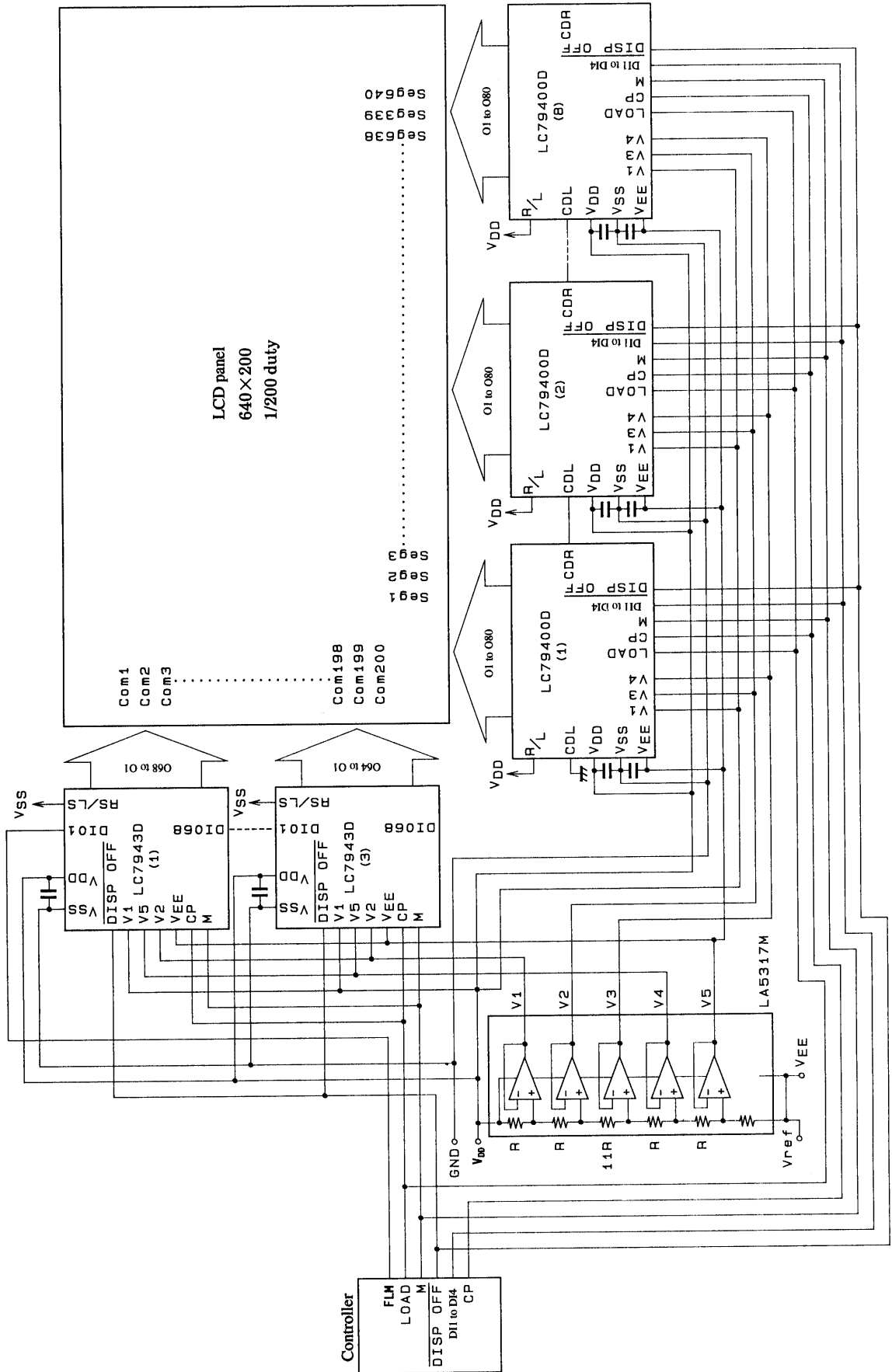
Time Chart (1/200 Duty 1/15 Bias) Switching Characteristics



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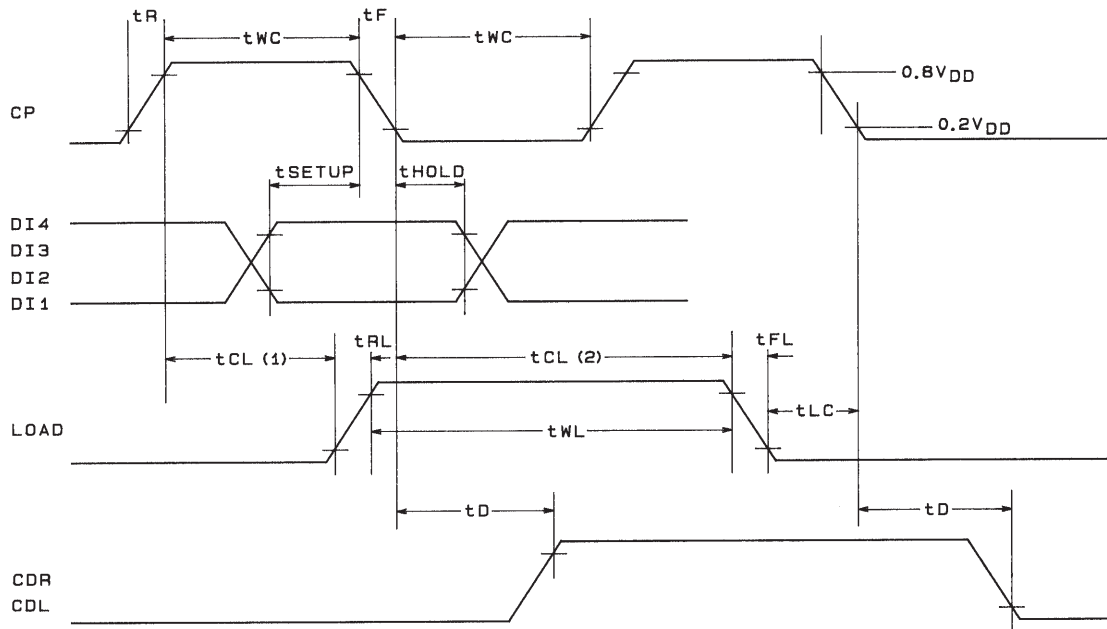
Sample Application



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Switching Characteristics



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