Ordering number: EN ※5632

CMOS LSI

LC86E5032

8-Bit Single-Chip Microcontroller

Preliminary

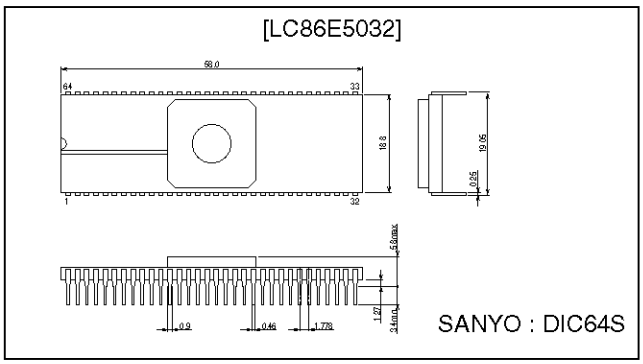
Overview

The LC86E5032 microcontroller, a new addition to the LC865000 series, is an 8-bit single chip CMOS microcontroller with UVEPROM.
This microcontroller has the same functions and pin assignment as for the LC865000 series mask ROM version, and a 32K-byte EPROM. Program data is rewritable.
It is suitable for program developments.

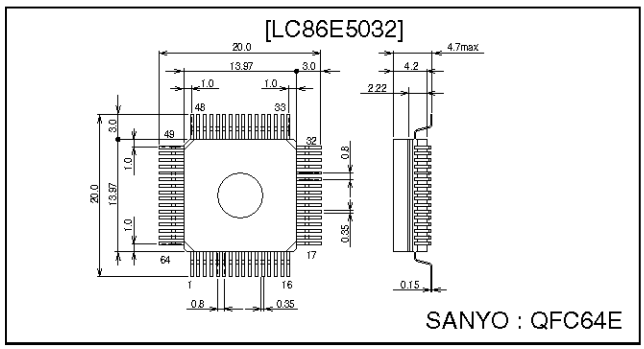
Package Dimensions

unit : mm

3126-DIC64S



3194-QFC64E



Features

(1) Option switching using EPROM data
The optional functions of the LC865000 series can be specified using EPROM data.
The trial products of the LC86E5032 can be evaluated with the mass production board.
(2) Internal EPROM capacity : 32768 bytes
(3) Internal RAM capacity : 512 bytes

Mask ROM version	PROM capacity	RAM capacity
LC865032	32512 bytes	512 bytes
LC865028	28672 bytes	512 bytes
LC865024	24576 bytes	512 bytes
LC865020	20480 bytes	384 bytes
LC865016	16384 bytes	384 bytes
LC865012	12288 bytes	384 bytes
LC865008	8192 bytes	384 bytes

(4) Operating voltage : 4.5 to 6.0 V
(5) Instruction cycle time : 0.98 to 400 μs
(6) Operating temperature range : +10°C to +40°C
(7) The pin compatible with the mask ROM version
(8) Applicable mask version : LC865032, LC865028, LC865024, LC865020, LC865016, LC865012, LC865008
(9) Factory shipment : DIC-64S
QFC-64E

SANYO Electric Co.,Ltd. Semiconductor Business Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

Usage Notes

When using, please take note of the following.

(1) Differences between the LC86E5032 and the LC865000 series

Items	LC86E5032	LC865032/28/24/20/16/12/08
Port status at reset	Please refer to "Port status at reset" on the next page.	
Operation after releasing reset	The option is specified by degrees within 3 ms after applying a 'H' level to the reset pin. The program is located at 00H is executed.	The program located at 00H is executed immediately after applying a 'H' level the reset pin.
Operating voltage range (V_{DD})	4.5 to 6.0 V	2.7 to 6.0 V
Operating temperature range (Topr)	+10°C to +40°C	–30°C to +70°C
Total output current [$\Sigma I_{OAH}(1)$] [$\Sigma I_{OAH}(1)$]	Refer to 'Electrical Characteristics' on the semiconductor news.	
Current drain [$I_{DDOP}(1)$] [$I_{DDOP}(2)$] [$I_{DDOP}(3)$] [$I_{DDOP}(4)$]		

• LC86E5032 Options.

Options	Pins, Circuits	Option settings
Configuration of input/output ports	Port 0 (Can be specified for each bit.)	1. Input : No pull-up MOS transistor Output : N-channel open drain 2. Input : Pull-up MOS transistor Output : CMOS
	Ports 1, 2 (Can be specified for each bit.)	1. Input : No programmable pull-up MOS transistor Output : N-channel open drain 2. Input : Programmable pull-up MOS transistor Output : CMOS
	Ports 3, 4, 5 (Can be specified for each bit.)	1. Input : No programmable pull-up MOS transistor Output : N-channel open drain 2. Input : Programmable pull-up MOS transistor Output : CMOS
Port 7 pull-up MOS transistor	Port 7 (Can be specified for each bit.)	1. Pull-up MOS transistor not provided 2. Pull-up MOS transistor provided *$\overline{P74}$ has no pull-up resistor option.

At reset, some port operations related to the option are different between the LC86E5032 and the LC865032/28/24/20/16/12/08. Please refer to the next table.

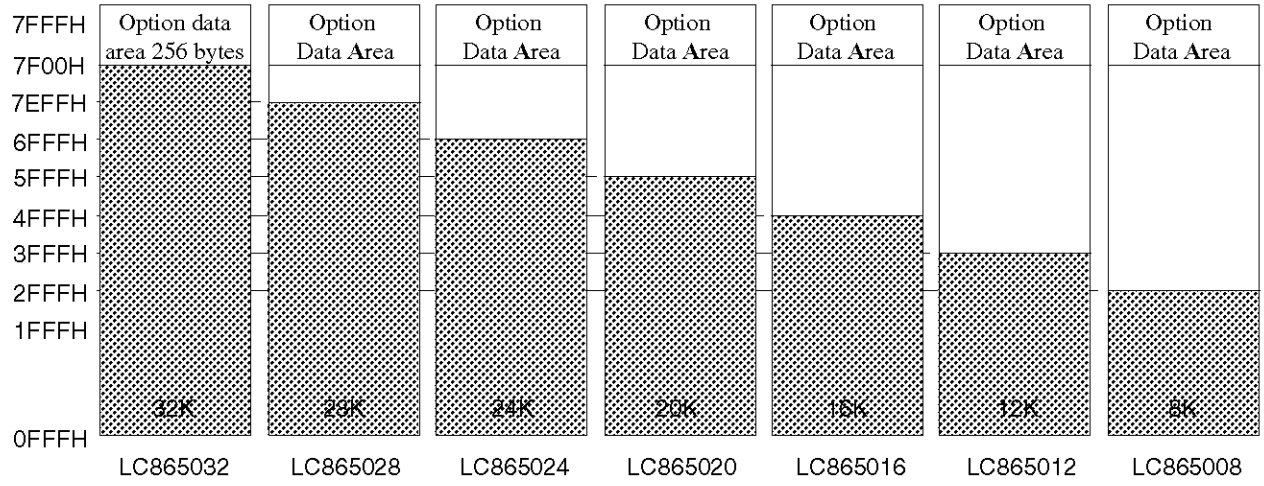
• Port configuration at reset

Pin	Option settings	LC86E5032	LC865032/28/24/20/16/12/08
P0	Input : No pull-up MOS transistor Output : N-channel open drain	(Same as for the mask version)	Input mode without pull-up MOS transistor (Output is OFF)
	Input : Pull-up MOS transistor Output : CMOS	Input mode • The pull-up MOS transistor is not present during reset or several hundred microseconds after releasing reset. After that, the pull-up MOS transistor is present. (Output is OFF)	Input mode with pull-up MOS transistor (Output is OFF)
P1, P2	Input : Programmable pull-up MOS transistor Output : N-channel open drain	(Same as for the mask version)	Input mode without pull-up MOS transistor (Output is OFF)
	Input : Programmable pull-up MOS transistor Output : CMOS	(Same as for the mask version)	Input mode without pull-up MOS transistor (Output is OFF)
P3, P4, P5	Input : Nonprogrammable pull-up MOS transistor Output : N-channel open drain	(Same as for the mask version)	Input mode without pull-up MOS transistor (Output is OFF)
	Input : Programmable pull-up MOS transistor Output : CMOS	(Same as for the mask version)	Input mode without pull-up MOS transistor (Output is OFF)
P7	Pull-up MOS transistor not provided	(Same as the mask version)	Input mode without pull-up MOS transistor
	Pull-up MOS transistor provided	Input mode • The pull-up MOS transistor is not present during reset or several hundred microseconds after releasing reset. After that, the pull-up MOS transistor is present.	Input mode with pull-up MOS transistor

(2) Option

The LC86E5032 uses 256 bytes addressed 7F00H to 7FFFH in program memory as option data area. This area does not affect the execution of program but means that the LC865032 program memory is 32512 bytes addressed 0000H to 7EFFH.
The option data is specified by the option-setting program "SU865000. EXE". The specified option data is linked to the program area by linkage editor "L865000. EXE".

(3) ROM space



Writing to EPROM

(1) Specification of options
Programming data for the LC86E5032's EPROM is required.
The debugged evaluation file (EVA file) must be converted to an INTEL-HEX format file (HEX file) with the file converter program, EVA2HEX.EXE. The HEX file is used as the programming data for the LC86E5032.

(2) How to write data to EPROM
The LC86E5032 can be programmed by a general-purpose EPROM programmer with attachments W86EP5032D and W86EP5032Q.

- Recommended EPROM programmers

Supplier	EPROM programmer
Advantest	R4945, R4944, R4943
Andou	AF-9704
AVAL	PKW-1100, PKW-3000
Minato Electronics	MODEL 1890A

- "27512 (Vp-p = 12.5 V) Intel high-speed programming" mode should be used. The address must be set to "0000H to 7FFFH" and the jumper (DASEC) must be set 'OFF' at programming.

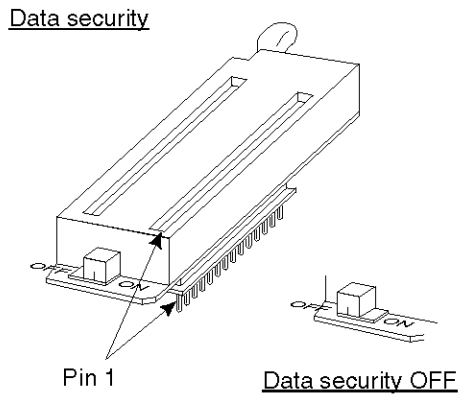
(3) How to use the data security function
"Data security" is a function to prevent the EPROM data from being read.
Instructions on using the data security function:

1. Set the jumper of the attachment 'ON'.
2. Attempt to program the EPROM. The EPROM programmer displays an error. The error is a result of normal activity of the data security feature. This is not a problem with the EPROM programmer chip.

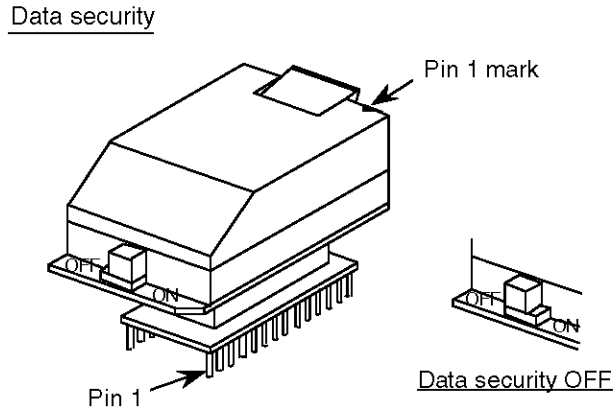
Notes
- The data security function is not carried out when the data of all address contain 'FF' at step 2 above.
- Data security cannot be executed when the sequential writing operation of programming "BLANK=>PROGRAM=>VERIFY" is used at step 2 above.
- Set the jumper 'OFF' after the execution of data security.

(4) Erasing data
Use a general-purpose EPROM eraser to erase the written data.

(5) Shielding
The UVEPROM (ultraviolet erasable programmable ROM) is incorporated in the IC. Cover the window of the IC with a seal in use.

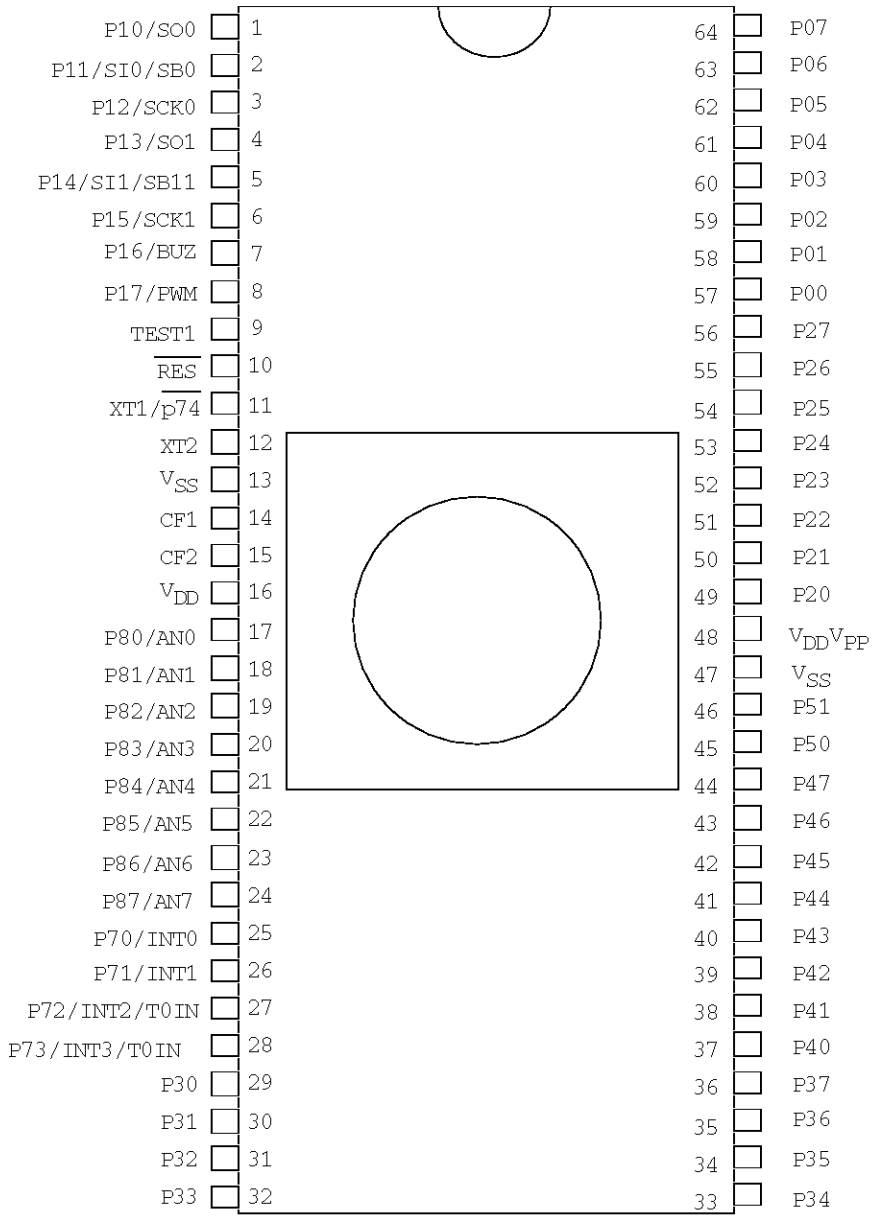


W86EP5032D



W86EP5032Q

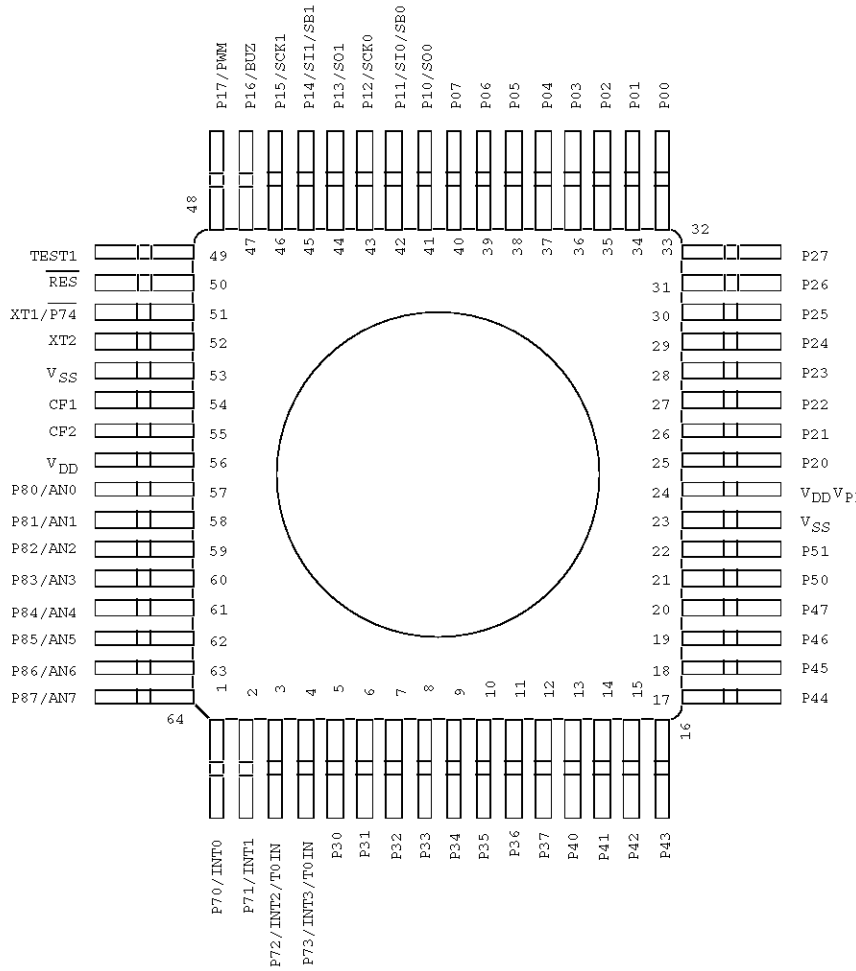
Pin Assignment



Top view

SANYO : DIC64S

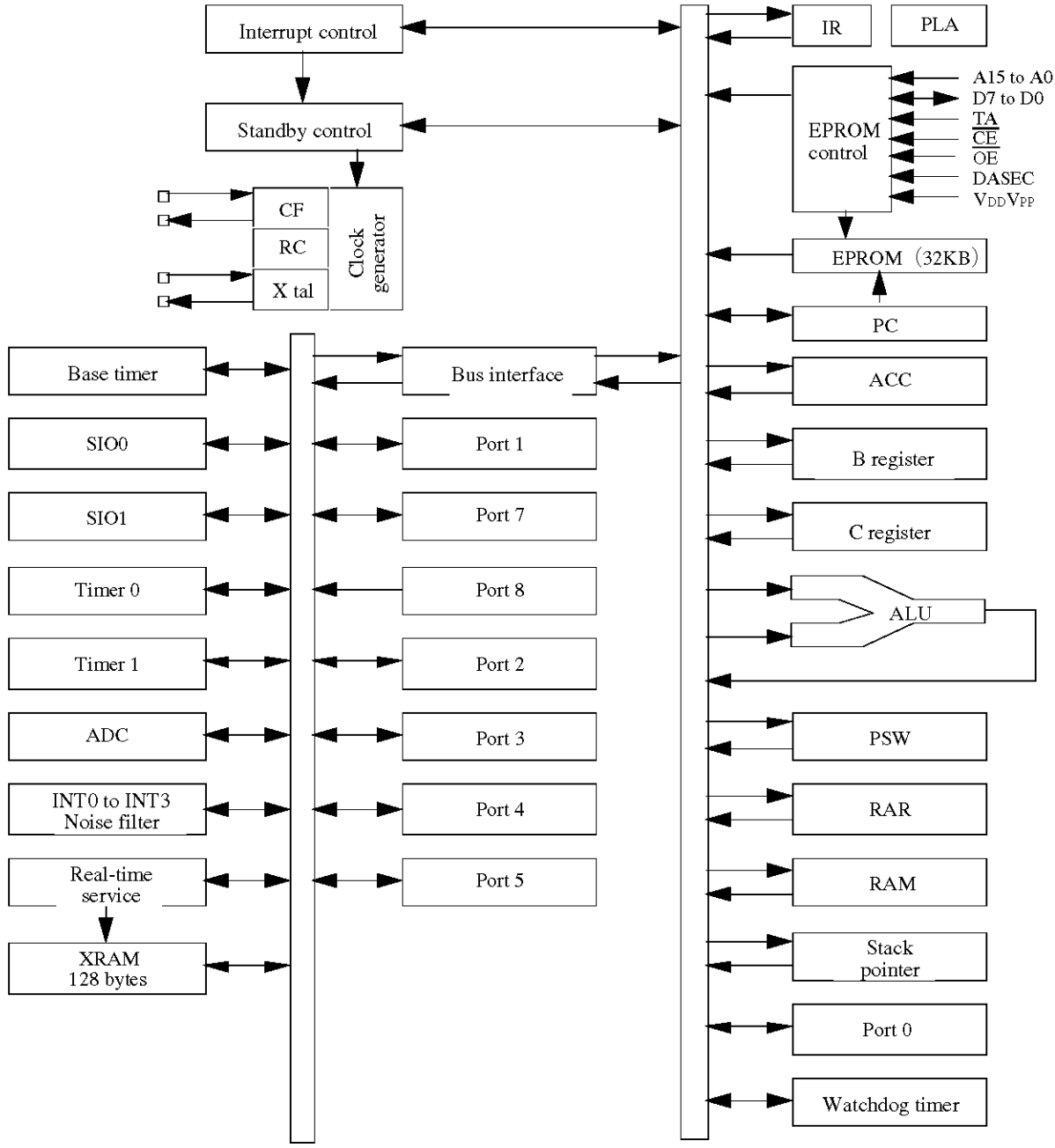
Pin Assignment



Top view

SANYO : QFC64E

System Block Diagram



LC86E5032 Pin Description

<table>
<tr><th>Pin name</th><th>I/O</th><th>Function description</th><th>Option</th><th>Function in PROM mode</th></tr>
<tr><td>V_{SS}</td><td></td><td>Power supply pin (–)</td><td></td><td></td></tr>
<tr><td>V_{DD}</td><td></td><td>Power supply pin (+)</td><td></td><td></td></tr>
<tr><td>$V_{DD}V_{PP}$</td><td></td><td>Power supply pin (+)</td><td></td><td>Power for programming</td></tr>
<tr><td>PORT0
P00 to P07</td><td>I/O</td><td>• 8-bit input/output port
• Input for port 0 interrupt
• Input/output in nibble units
• Input for HOLD release</td><td>• Pull-up resistor :
Present/Not present

• Output form : CMOS/
N-channel open-drain.</td><td></td></tr>
<tr><td>PORT1
P10 to P17</td><td>I/O</td><td>• 8-bit input/output port
• Data direction can be specified for each bit.
• Other pin functions
P10 : SIO0 data output
P11 : SIO0 data input/bus input/output
P12 : SIO0 clock input/output
P13 : SIO1 data output
P14 : SIO1 data input/ bus input/output
P15 : SIO1 clock input/output
P16 : Buzzer output
P17 : Timer 1 output (PWM output)</td><td>Output form : CMOS/
N-channel open-drain</td><td>Data input/output
• D0 to D7</td></tr>
<tr><td>PORT2
P20 to P27</td><td>I/O</td><td>• 8-bit input/output port
• Data direction can be specified for each bit.</td><td>Output form : CMOS/
N-channel open-drain</td><td></td></tr>
<tr><td>PORT3
P30 to P37</td><td>I/O</td><td>• 8-bit input/output port
• Data direction can be specified for each bit.
• 15 V withstand at N-ch open-drain output</td><td>Output form : CMOS/
N-channel open-drain</td><td>Address input
• A7 to A0</td></tr>
<tr><td>PORT4
P40 to P47</td><td>I/O</td><td>• 8-bit input/output port
• Data direction can be specified for each bit.
• 15 V withstand at N-ch open-drain output</td><td>Output form : CMOS/
N-channel open-drain</td><td>Address input
• A14 to A8 (*5)
• P47 : TA (*4)</td></tr>
<tr><td>PORT5
P50 to P51</td><td>I/O</td><td>• 2-bit input/output port.
• Data direction can be specified for each bit.
• 15 V withstand at N-ch open-drain output</td><td>Output form : CMOS/
N-channel open-drain</td><td></td></tr>
<tr><td>PORT7

P70

P71 to $\overline{P74}$</td><td>

I/O

I</td><td>• 5-bit input port
• Other pin functions
P70 : INT0 input/HOLD release/N-channel transistor output for watchdog timer.
P71 : INT 1 input/HOLD release.
P72 : INT 2 input/timer 0 event input.
P73 : INT 3 input with noise filter/timer 0 event input.
$\overline{P74}$: Input pin XT1 for 32.768 kHz crystal oscillation
• Interrupt received format, vector address.</td><td>Pull-up resistor :
Present/Not present
(P70, 71, 72, 73)
* $\overline{P74}$ has no pull-up resistor.</td><td>

Input of PROM control signal
• DASEC (*1)
• $\overline{OE}$ (*2)
• $\overline{CE}$ (*3)</td></tr>
</table>

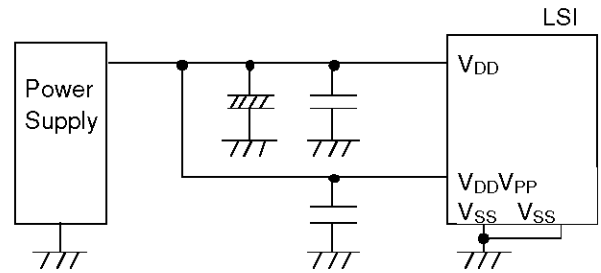
	Rising	Falling	Rising & falling	High level	Low level	Vector
INT0	Enable	Enable	Disable	Enable	Enable	03H
INT1	Enable	Enable	Disable	Enable	Enable	0BH
INT2	Enable	Enable	Enable	Disable	Disable	13H
INT3	Enable	Enable	Enable	Disable	Disable	1BH

Pin name	I/O	Function description	Option	Function in PROM mode
PORT8 P80 to P87	I	• 8-bit input port • Other functions AD input port (8 port pins)		
$\overline{RES}$	I	Reset pin		
TEST1	O	Test pin Should be left open.		
XT1/$\overline{P74}$	I	• Input pin for 32.768 kHz crystal oscillation • Other function : Input port $\overline{P74}$ When not used, connect to V_{DD}.		
XT2	O	Output pin for 32.768 kHz crystal oscillation When not used, should be left open.		
CF1	I	Input pin for ceramic resonator oscillation		
CF2	O	Output pin for ceramic resonator oscillation		

• All port options can be specified in bit units.

*1 Memory select input for data security
*2 Output enable input
*3 Chip enable input
*4 TA → PROM control signal input
*5 A14 → Address input

• Connect as shown in the following figure to reduce noise into V_{DD} pin.
Short-circuit the V_{DD} pin to the $V_{DD}V_{PP}$ pin.
Short-circuit the V_{SS} pin to the V_{SS} pin.



1. Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter		Symbol	Pins	Conditions		Ratings			Unit
					V_{DD}[V]	min	typ	max	
Supply voltage		V_{DD} max	V_{DD},$V_{DD}V_{PP}$	V_{DD} = $V_{DD}V_{PP}$		–0.3		+7.0	V
Input voltage		V_I(1)	• Ports 71, 72, 73, $\overline{74}$ • Port 8 • $\overline{RES}$			–0.3		V_{DD}+0.3	
Input/output voltage		V_{IO}(1)	• Ports 0, 1, 2 • Ports 3, 4, 5 of CMOS output			–0.3		V_{DD}+0.3	
		V_{IO}(2)	• Ports 3, 4, 5 of open-drain output			–0.3		+15	
High-level output current	Peak output current	I_{OPH}(1)	Ports 0, 1, 2, 3, 4, 5	• CMOS output • At each pin		–4			mA
	Total output current	ΣI_{OAH}(1)	Ports 0, 1, 2	Total of all pins		–25			
		ΣI_{OAH}(2)	Ports 3, 4, 5	Total of all pins		–20			
Low-level output current	Peak output current	I_{OPL}(1)	Ports 0, 1, 2, 3, 4, 5	At each pin				20	
		I_{OPL}(2)	Port 70	At each pin				15	
	Total output current	ΣI_{OAL}(1)	Ports 0, 1, 70	Total of all pins				40	
		ΣI_{OAL}(2)	Port 2	Total of all pins				40	
		ΣI_{OAL}(3)	Ports 3, 4, 5	Total of all pins				80	
Power dissipation (max.)		Pd max(1)	DIC64S	Ta = +10°C to +40°C				720	mW
		Pd max(2)	QFC64E	Ta = +10°C to +40°C				420	
Operating temperature range		Topr				10		40	°C
Storage temperature range		Tstg				–65		+150	

2. Recommended Operating Range at Ta = +10°C to +40°C, V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions		Ratings			Unit
				V_{DD}[V]	min	typ	max	
Operating voltage range	V_{DD}(1)	V_{DD}	0.98 µs ≤ tCYC tCYC ≤ 400 µs		4.5		6.0	V
HOLD voltage	V_{HD}	V_{DD}	RAM and registers retain their pre-HOLD mode values.		2.0		6.0	
Input high voltage	V_{IH}(1)	Port 0 (Schmitt)	Output disabled	4.5 to 6.0	0.4V_{DD} +0.9		V_{DD}	
	V_{IH}(2)	• Ports 1, 2 • Ports 72, 73 (Schmitt)	Output disabled	4.5 to 6.0	0.75V_{DD}		V_{DD}	
	V_{IH}(3)	• Port 70 Port input/interrupt. • Port 71 • RES (Schmitt)	Output N-channel transistor OFF	4.5 to 6.0	0.75V_{DD}		V_{DD}	
	V_{IH}(4)	Port 70 Watchdog timer	Output N-channel transistor OFF	4.5 to 6.0	0.9V_{DD}		V_{DD}	
	V_{IH}(5)	• Port $\overline{74}$ • Port 8	Output N-channel transistor OFF	4.5 to 6.0	0.75V_{DD}		V_{DD}	
	V_{IH}(6)	Ports 3, 4, 5 of CMOS output (Schmitt)	Output disabled	4.5 to 6.0	0.75V_{DD}		V_{DD}	
	V_{IH}(7)	Ports 3, 4, 5 of open drain output (Schmitt)	Output disabled	4.5 to 6.0	0.75V_{DD}		13.5	
Input low voltage	V_{IL}(1)	Port 0 (Schmitt)	Output disabled	4.5 to 6.0	V_{SS}		0.2V_{DD}	
	V_{IL}(2)	• Ports 1, 2, 3, 4, 5 • Ports 72, 73 (Schmitt)	Output disabled	4.5 to 6.0	V_{SS}		0.25V_{DD}	
	V_{IL}(3)	• Port 70 Port input/interrupt. • Port 71 • RES (Schmitt)	N-channel transistor OFF	4.5 to 6.0	V_{SS}		0.25V_{DD}	
	V_{IL}(4)	Port 70 Watchdog timer	N-channel transistor OFF	4.5 to 6.0	V_{SS}		0.8V_{DD} –1.0	
	V_{IL}(5)	• Port $\overline{74}$ • Port 8	N-channel transistor OFF	4.5 to 6.0	V_{SS}		0.25V_{DD}	
Operation cycle time	tCYC			4.5 to 6.0	0.98		400	µs

Parameter	Symbol	Pins	Conditions	Ratings				Unit
				V_{DD}[V]	min	typ	max	
Oscillation frequency range (Note 1)	FmCF(1)	CF1, CF2	• 12 MHz (ceramic resonator oscillation). • Refer to Figure 1.	4.5 to 6.0	11.76	12	12.24	MHz
	FmCF(2)	CF1, CF2	• 3 MHz (ceramic resonator oscillation). • Refer to Figure 1.	4.5 to 6.0	2.94	3	3.06	
	FmRC		RC oscillation	4.5 to 6.0	0.4	0.8	2.0	
	FsXtal	XT1, XT2	• 32.768 kHz (crystal oscillation). • Refer to Figure 2.	4.5 to 6.0		32.768		kHz
Oscillation stable time period (Note 1)	tmsCF(1)	CF1, CF2	• 12 MHz (ceramic resonator oscillation). • Refer to Figure 3.	4.5 to 6.0		0.03	0.5	ms
	tmsCF(2)	CF1, CF2	• 3 MHz (ceramic resonator oscillation). • Refer to Figure 3.	4.5 to 6.0		0.2	2	
	tssXtal	XT1, XT2	• 32.768 kHz (crystal oscillation). • Refer to Figure 3.	4.5 to 6.0		1	1.5	s

(Note 1) Refer to Table 1 and Table 2 for the oscillation constants.

3. Electrical Characteristics at Ta= +10°C to +40°C , V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions	Ratings				Unit
				V_{DD} [V]	min	typ	max	
Input high current	$I_{IH}(1)$	• Ports 3, 4, 5 at open-drain output	• Output disabled • V_{IN} = 13.5 V (including off-state leak current of output transistor)	4.5 to 6.0			5	µA
	$I_{IH}(2)$	• Port 0 without pull-up MOS transistor • Ports 1, 2, 3, 4, 5	• Output disabled • Pull-up MOS transistor OFF. V_{IN} = V_{DD} (including off-state leak current of output transistor)	4.5 to 6.0			1	
	$I_{IH}(3)$	• Ports 70, 71, 72, 73 without pull-up MOS transistor • Port 8	V_{IN}= V_{DD}	4.5 to 6.0			1	
	$I_{IH}(4)$	• $\overline{RES}$	V_{IN} = V_{DD}	4.5 to 6.0			1	
Input low current	$I_{IL}(1)$	• Ports 1, 2, 3, 4, 5 • Port 0 without pull-up MOS transistor	• Output disabled • Pull-up MOS transistor OFF. V_{IN} = V_{SS} (including off-state leak current of output transistor)	4.5 to 6.0	–1			
	$I_{IL}(2)$	• Ports 70, 71, 72, 73 without pull-up MOS transistor • Port 8	V_{IN} = V_{SS}	4.5 to 6.0	–1			
	$I_{IL}(3)$	• $\overline{RES}$	V_{IN} = V_{SS}	4.5 to 6.0	–1			
Output high voltage	$V_{OH}(1)$	• Ports 0, 1, 2, 3, 4, 5 at CMOS output	I_{OH} = –1.0 mA	4.5 to 6.0	V_{DD}–1			V
	$V_{OH}(2)$		I_{OH} = –0.1 mA	4.5 to 6.0	V_{DD}–0.5			
Output low voltage	$V_{OL}(1)$	Ports 0, 1, 2, 3, 4, 5	I_{OL} = 10 mA	4.5 to 6.0			1.5	
	$V_{OL}(2)$		I_{OL} = 1.6 mA	4.5 to 6.0			0.4	
	$V_{OL}(3)$	Port 70	I_{OL} = 1 mA	4.5 to 6.0			0.4	
	$V_{OL}(4)$		I_{OL} = 0.5 mA	4.5 to 6.0			0.4	
Pull-up MOS transistor resistance	Rpu	• Ports 0, 1, 2, 3, 4, 5 • Ports 70, 71, 72, 73	V_{OH} = 0.9 V_{DD}	4.5 to 6.0	15	40	70	kΩ
Hysteresis voltage	V_{HIS}	• Ports 0, 1, 2, 3, 4, 5 • Ports 70, 71, 72, 73 • $\overline{RES}$	Output disable	4.5 to 6.0		0.1V_{DD}		V
Pin capacitance	CP	All pins	• f = 1 MHz • Unmeasured input pins are set to V_{SS} level. • Ta = 25°C	4.5 to 6.0		10		pF

4. Serial Input/Output Characteristics at Ta = +10°C to +40°C, V_{SS} = 0 V

Parameter			Symbol	Pins	Conditions	Ratings				Unit
						V_{DD} [V]	min	typ	max	
Serial clock	Input clock	Cycle	tCKCY(1)	SCK0, SCK1	Refer to Figure 5.	4.5 to 6.0	2			tCYC
		Low-level pulse width	tCKL(1)			4.5 to 6.0	1			
		High-level pulse width	tCKH(1)			4.5 to 6.0	1			
	Output clock	Cycle	tCKCY(2)	SCK0, SCK1	• Use pull-up resistor (1 kΩ) when set to open-drain output. • Refer to Figure 5.	4.5 to 6.0	2			
		Low-level pulse width	tCKL(2)			4.5 to 6.0		1/2tCKCY		
		High-level pulse width	tCKH(2)			4.5 to 6.0		1/2tCKCY		
Serial input	Data setup time		tICK	• SI0, SI1 • SB0, SB1	• Data set-up to SCK0, 1	4.5 to 6.0	0.1			µs
	Data hold time		tCKI		• Data hold from SCK0, 1 • Refer to Figure 5.	4.5 to 6.0	0.1			
Serial output	Output delay time (Serial clock is extrnal clock.)		tCKO(1)	• SO0, SO1 • SB0, SB1	• Use pull-up resistor (1 kΩ) when set to open-drain output.	4.5 to 6.0			7/12tCYC +0.2	
	Output delay time (Serial clock is internal clock.)		tCKO(2)		• Data hold from SCK0, 1 • Refer to Figure 5.	4.5 to 6.0			1/3tCYC +0.2	

5. Pulse Input Conditions at Ta = +10°C to +40°C, V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions	Ratings				Unit
				V_{DD} [V]	min	typ	max	
High/low-level pulse width	tPIH(1) tPIL(1)	• INT0, INT1 • INT2/T0IN • INT3	• Interrupt acceptable • Timer 0 pulse countable	4.5 to 6.0	1			tCYC
	tPIH(2) tPIL(2)	INT3 (The noise rejection clock selected to 1/1.)	• Interrupt acceptable • Timer 0 pulse countable	4.5 to 6.0	2			
	tPIH(3) tPIL(3)	INT3 (The noise rejection clock selected to 1/16.)	• Interrupt acceptable • Timer 0 pulse countable	4.5 to 6.0	32			
	tPIL(4)	$\overline{RES}$	Reset acceptable	4.5 to 6.0	200			µs

6. A/D Converter Characteristics at Ta = +10°C to +40°C, V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions	Ratings				Unit
				V_{DD} [V]	min	typ	max	
Resolution	N			4.5 to 6.0		8		bit
Absolute precision (Note 2)	ET			4.5 to 6.0			±1/5	LSB
Conversion time	tCAD		A/D conversion time = 16 x tCYC (ADCR2 = 0) (Note 3)	4.5 to 6.0	15.68 (tCYC = 0.98 µs)		65.28 (tCYC = 4.08 µs)	µs
			A/D conversion time = 32 x tCYC (ADCR2 = 1) (Note 3)		31.36 (tCYC = 0.98 µs)		130.56 (tCYC = 4.08 µs)	
Analog input voltage range	V_{AIN}	AN0 to AN7		4.5 to 5.5	V_{SS}		V_{DD}	V
Analog port input current	I_{AINH}		V_{AIN} = V_{DD}	4.5 to 5.5			+1	µA
	I_{AINL}		V_{AIN} = V_{SS}	4.5 to 5.5	–1			

(Note 2) Absolute precision excepts quantizing error (±1/2 LSB).
(Note 3) The conversion time is the time from execution of the instruction to start conversion to the completion of shifting the A/D converted value to the register.

7. Current Drain Characteristics at Ta = +10°C to +40°C, V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions	Ratings				Unit
				V_{DD} [V]	min	typ	max	
Current drain during basic operation (Note 4)	I_{DDOP}(1)	V_{DD}	• FmCF = 12 MHz for ceramic resonator oscillation. • FsXtal = 32.768 kHz for crystal oscillator. • System clock : CF oscillator. • Internal RC oscillator stopped.	4.5 to 6.0		13	26	mA
	I_{DDOP}(2)		• FmCF = 3 MHz for ceramic resonator oscillation. • FsXtal = 32.768 kHz for crystal oscillator. • System clock : CF oscillator. • Internal RC oscillator stopped.	4.5 to 6.0		7	14	
	I_{DDOP}(3)		• FmCF = 0 Hz (when oscillator stops). • FsXtal = 32.768 kHz for crystal oscillator. • System clock : RC oscillator.	4.5 to 6.0		4	10	
	I_{DDOP}(4)		• FmCF = 0 Hz (when oscillator stops). • FsXtal = 32.768 kHz for crystal oscillator. • System clock : crystal oscillator. • Internal RC oscillator stopped.	4.5 to 6.0		4	8	

Parameter	Symbol	Pins	Conditions		Ratings			Unit
				V_{DD} [V]	min	typ	max	
Current drain at HALT mode (Note 4)	$I_{DDHALT}(1)$	V_{DD}	• HALT mode • FmCF = 12 MHz for ceramic resonator oscillation. • FsXtal = 32.768 kHz for crystal oscillator. • System clock : CF oscillator. • Internal RC oscillator stopped.	4.5 to 6.0		5	10	mA
	$I_{DDHALT}(2)$		• HALT mode • FmCF = 3 MHz for ceramic resonator oscillation. • FsXtal = 32.768 kHz for crystal oscillator. • System clock : CF oscillator. • Internal RC oscillator stopped.	4.5 to 6.0		2.2	4.6	
	$I_{DDHALT}(3)$		• HALT mode • FmCF = 0 Hz (when oscillator stops). • FsXtal = 32.768 kHz for crystal oscillator. • System clock : RC oscillator	4.5 to 6.0		550	1100	µA
	$I_{DDHALT}(4)$		• HALT mode • FmCF = 0 Hz (when oscillator stops). • FsXtal = 32.768 kHz for crystal oscillator. • System clock : crystal oscillator. • Internal RC oscillator stopped.	4.5 to 6.0		25	100	
Current drain at HOLD mode (Note 4)	$I_{DDHOLD}(1)$	V_{DD}	HOLD mode	4.5 to 6.0		0.05	30	
	$I_{DDHOLD}(2)$			2.5 to 4.5		0.02	20	

(Note 4) The currents of output transistors and pull-up transistors are ignored.

Table 1. Ceramic Resonator Oscillation Guaranteed Constants (Main clock)

Oscillation type	Supplier	Oscillator	C1	C2
12 MHz ceramic resonator oscillation	Murata	CSA12.0MTZ	33 pF	33 pF
		CST12.0MTW	on chip	
	Kyocera	KBR-12.0M	33 pF	33 pF
3 MHz ceramic resonator oscillation	Murata	CSA3.00MG040	100 pF	100 pF
		CST3.00MGW040	on chip	
	Kyocera	KBR-3.0MS	47 pF	47 pF

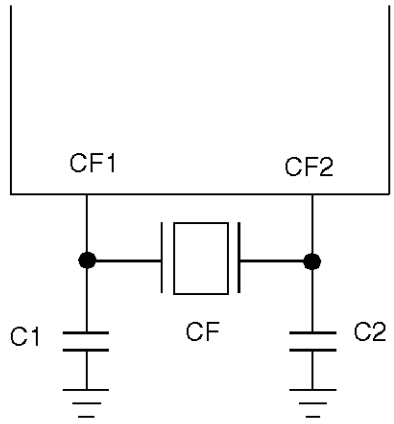
* Both C1 and C2 must use K rank (±10%) and SL characteristics.

Table 2. Crystal Oscillation Guaranteed Constants (Sub-clock)

Oscillation type	Supplier	Oscillator	C3	C4
32.768 kHz crystal oscillation	Dai Sinku	DT-38(1TA252E00)	18 pF	18 pF
	Kyocera	KF-38G-13P0200	18 pF	18 pF

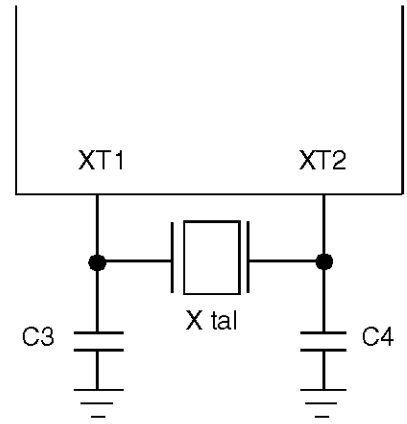
* Use J rank (±5%) and CH characteristics for C3 and C4.
(If high precision is unnecessary, use K rank (±10%) and SL characteristics.)

Notes • Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest pattern length.
• If you use other oscillators herein, we provide no guarantee for the characteristics.



Main-clock circuit

Figure 1 Ceramic Resonator Oscillation



Sub-clock circuit

Figure 2 Crystal Oscillation

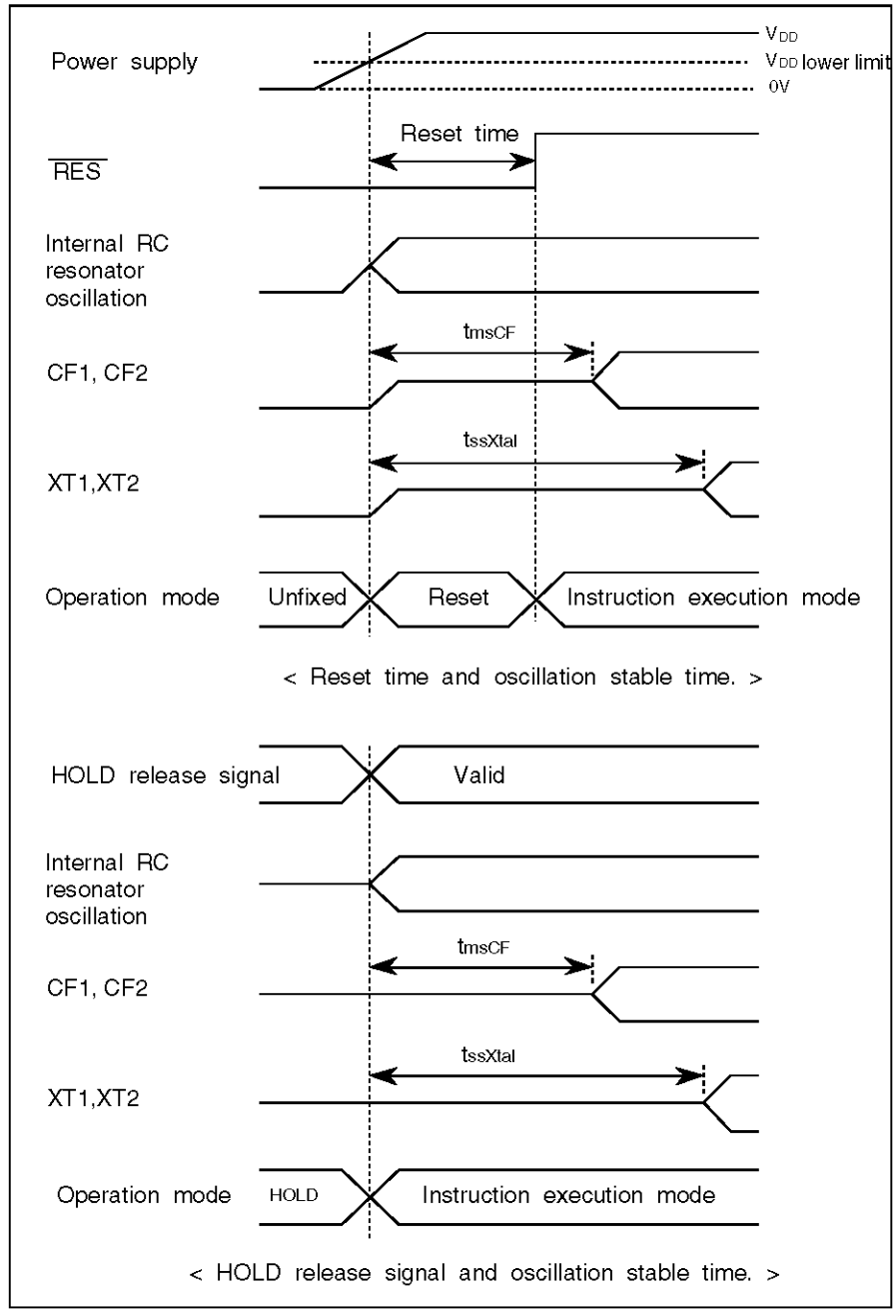
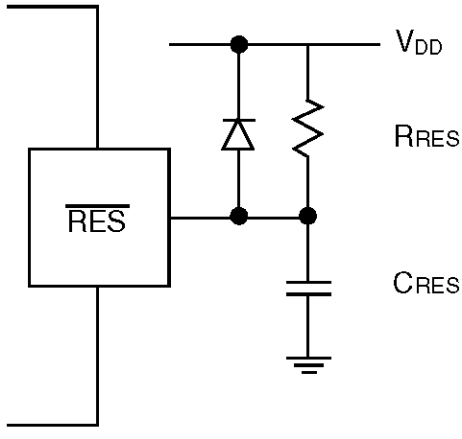
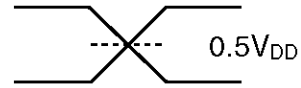


Figure 3 Oscillation Stable Time

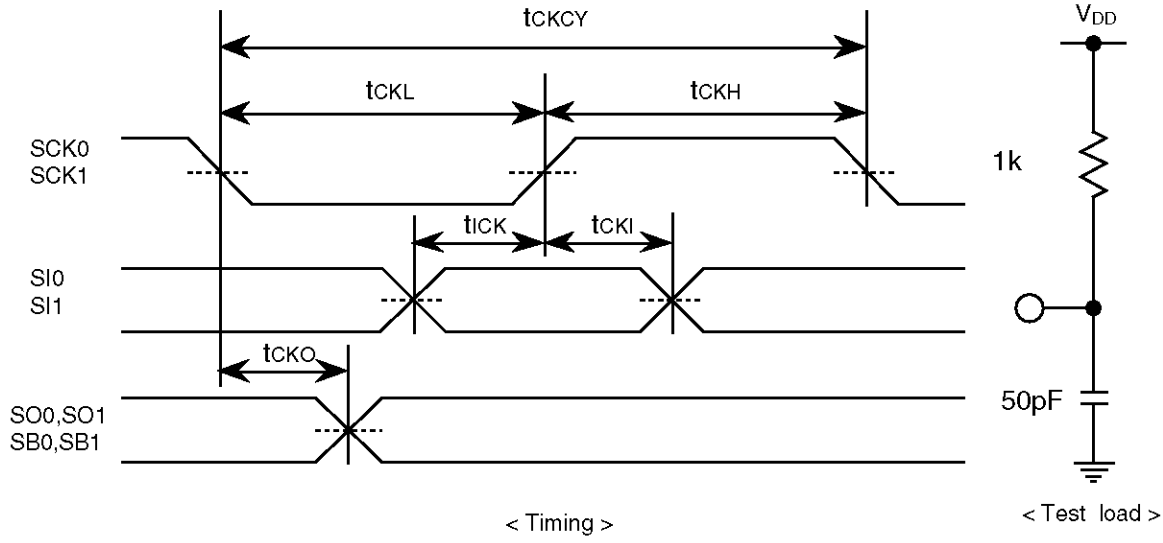


The values of C_{RES} and R_{RES} should be determined such that reset time is at least 200 µs, measured from the moment the power exceeds the V_{DD} lower limit.

Figure 4 Reset Circuit



< AC timing point >



< Timing > < Test load >

Figure 5 Serial Input/Output Test Conditions

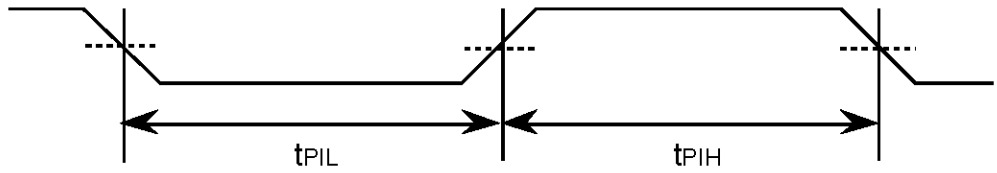


Figure 6 Pulse Input Timing Conditions