Ordering number : EN5476

CMOS LSI

LC78711E

Graphics Display Processor

Overview

The LC78711E is a CMOS LSI that provides graphics display drawing functions. In addition to implementing graphics display for NTSC and PAL signals, it provides two 32 × 32-dot sprite display patterns and can easily implement a wide range of displays.

Features

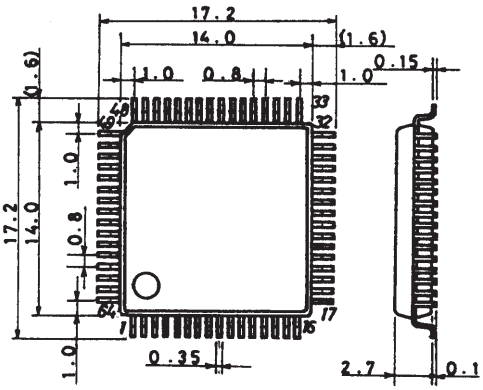
- Two-chip structure consisting of this LSI, the LC78711E, and an external 64-K × 4-bit RAM. (An RGB encoder is built in.)
- Graphics drawing controlled by a microprocessor over a serial interface.
- Includes two crystal oscillator systems, one for NTSC and one for PAL, and these system can be easily switched using the provided control pin.
  The standard clocks and all necessary internal timings can be generated by connecting two crystals, a 14.31818-MHz crystal for NTSC, and a 17.734476-MHz crystal for PAL.
- Two 32 × 32-dot sprite patterns provided. Up to two sprites can be displayed, either two different types or the same pattern in two different locations.
- 16 colors from a palette of 4096 colors can be displayed in graphics screens, and seven colors can be displayed in sprite patterns.
- Y/C signal outputs (two 8-bit D/A converter outputs)
- Supports the superimpose function, and provides a timing signal output.
- Provides a color bar signal output function.
- Adopts an 8-bit serial data input format for the external control input.

Package Dimensions

unit: mm

3159-QFP64E

[LC78711E]



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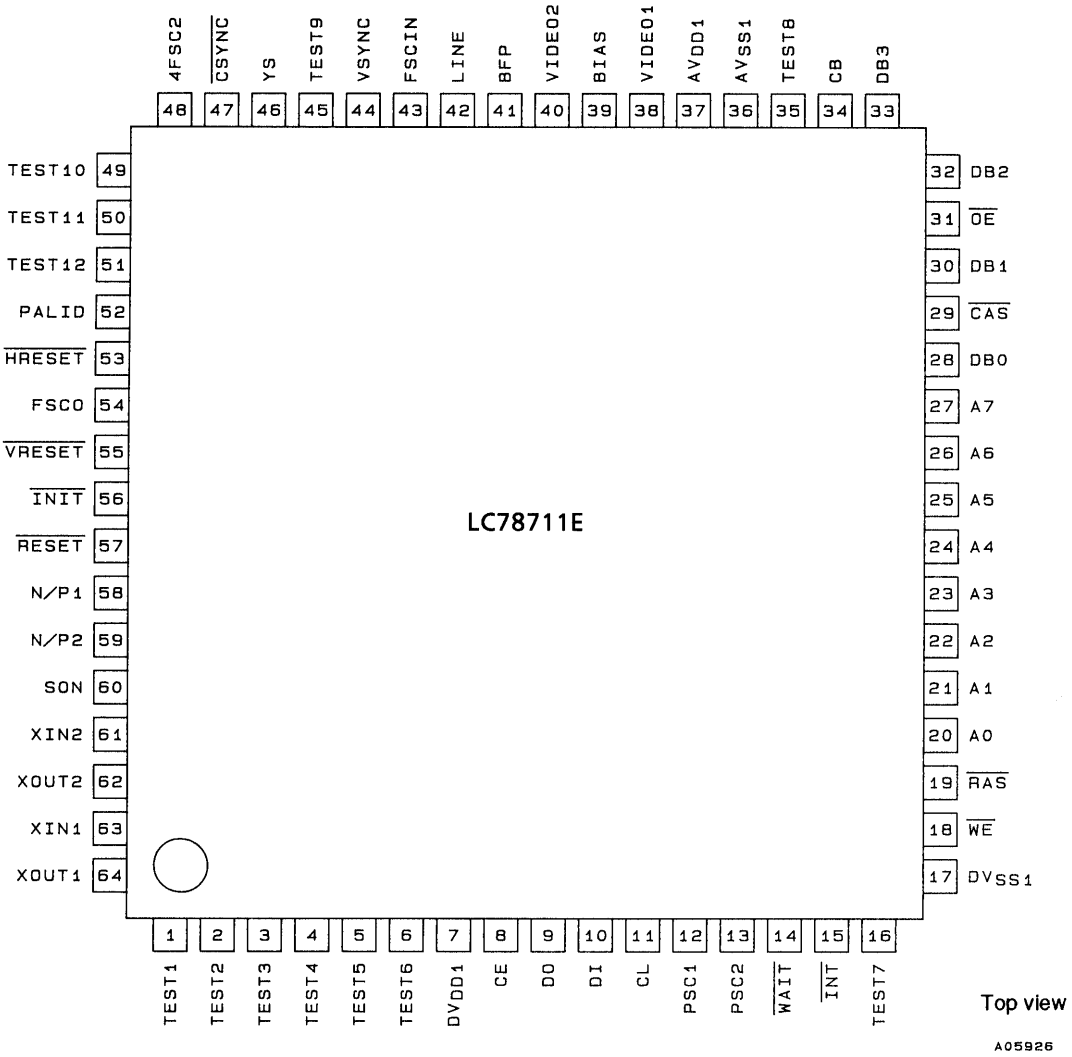
Pin Assignment



Specifications

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	$AV_{DD}1$, $DV_{DD}1$	V_{SS} – 0.3 to V_{SS} + 7.0	V
Maximum input voltage	V_{IN} max	TEST1, TEST2, TEST4, TEST5, TEST6, CE, DI, CL, TEST7, DB0 to DB3, CB, LINE, FSCIN, TEST9, 4FSC2, TEST12, PALID, HRESET, VRESET, INIT, RESET, N/P1, N/P2, SON, XIN1, XIN2	V_{SS} – 0.3 to V_{DD} + 0.3	V
Maximum output voltage	V_{OUT} max	TEST3, DO, PSC1, PSC2, WAIT, INT, WE, RAS, A0 to A7, DB0 to DB3, CAS, OE, TEST8, BFP, VSYNC, YS, CSYNC, TEST10, TEST11, FSC0, XOUT1, XOUT2	V_{SS} – 0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max	Ta = 25°C	500	mW
Operating temperature	Topr		–30 to +85	°C
Storage temperature	Tstg		–40 to +125	°C

Allowable Operating Ranges at Ta = –30 to +85°C, V_{SS} = 0 V

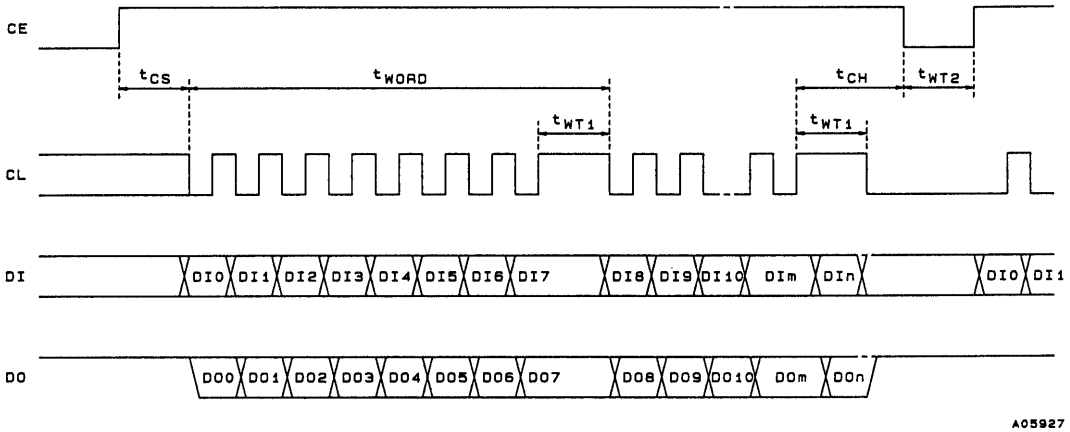
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}	$AV_{DD}1$, $DV_{DD}1$	4.5	5.0	5.5	V
Input high-level voltage	$V_{IH}1$	TEST1, TEST2, TEST4, TEST5, TEST6, CE, DI, TEST7, CB, LINE, TEST9, TEST12, PALID, $\overline{HRESET}$, $\overline{VRESET}$, N/P1, N/P2, SON	0.7 $V_{DD}1$		$V_{DD}1$ + 0.3	V
	$V_{IH}2$	CL, $\overline{INIT}$, $\overline{RESET}$	0.8 $V_{DD}1$		$V_{DD}1$ + 0.3	V
	$V_{IH}3$	DB0 to DB3	2.2		$V_{DD}1$ + 0.3	V
Input low-level voltage	$V_{IL}1$	TEST1, TEST2, TEST4, TEST5, TEST6, CE, DI, TEST7, CB, LINE, TEST9, TEST12, PALID, $\overline{HRESET}$, $\overline{VRESET}$, N/P1, N/P2, SON	$V_{SS}1$ – 0.3		0.3 $V_{DD}1$	V
	$V_{IL}2$	CL, $\overline{INIT}$, $\overline{RESET}$	$V_{SS}1$ – 0.3		0.2 $V_{DD}1$	V
	$V_{IL}3$	DB0 to DB3	$V_{SS}1$ – 0.3		0.8	V
Input frequency	$F_{SCIN}1$	XIN1		14.31818		MHz
	$F_{SCIN}2$	XIN2		17.73447		MHz
	$F_{SCIN}3$	4FSC2: NTSC mode		14.31818		MHz
		4FSC2: PAL mode		17.73447		MHz
	$F_{SCIN}4$	FSCIN: NTSC mode		3.57954		MHz
		FSCIN: PAL mode		4.43361		MHz
Input amplitude	$V_{IN}1$	FSCIN, 4FCS2	0.5		$V_{DD}1$	Vp-p
	$V_{IN}2$	XIN1, XIN2	0.5		$V_{DD}1$	Vp-p

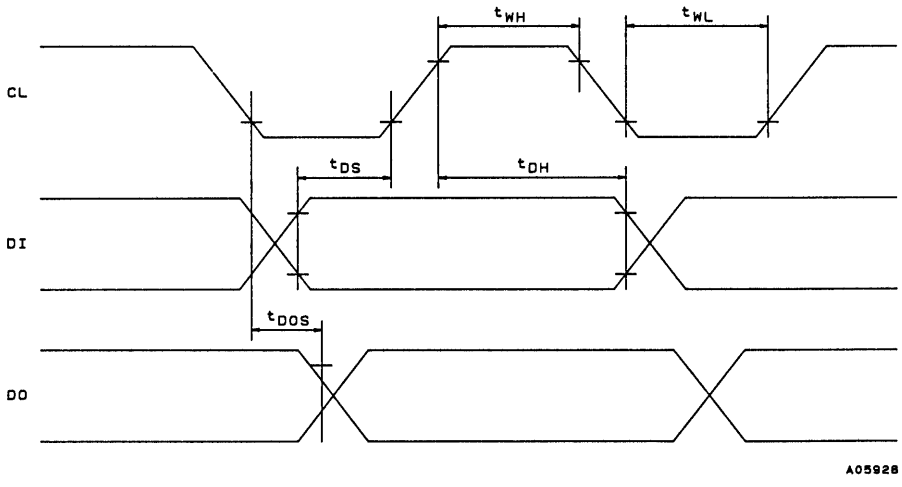
Electrical Characteristics at Ta = –30 to +85°C, $DV_{DD}1 = AV_{DD}1$ = 5 V unless otherwise specified.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high-level current	$I_{IH}1$	TEST1, TEST2, TEST4, TEST5, TEST6, CE, DI, CL, TEST7, DB0 to DB3, LINE, PALID, $\overline{HRESET}$, $\overline{VRESET}$, $\overline{INIT}$, $\overline{RESET}$, N/P1, N/P2, SON: $V_{IN} = DV_{DD}1$			5	µA
	$I_{IH}2$	CB, TEST9, TEST12: $V_{IN} = DV_{DD}1$	30	100	200	µA
Input low-level current	$I_{IL}1$	TEST1, TEST2, TEST4, TEST5, TEST6, CE, DI, CL, TEST7, DB0 to DB3, CB, LINE, TEST9, TEST12, $\overline{HRESET}$, $\overline{VRESET}$, $\overline{INIT}$, $\overline{RESET}$, N/P1, N/P2, SON: $V_{IN} = DV_{SS}1$	–5			µA
	$I_{IL}2$	PALID: $V_{IN} = DV_{SS}1$	–200	–100	–30	µA
Output high-level voltage	V_{OH}	TEST3, DO, PSC1, PSC2, $\overline{WAIT}$, $\overline{INT}$, BFP, $\overline{WE}$, $\overline{RAS}$, A0 to A7, $\overline{CAS}$, $\overline{OE}$, DB0 to DB3, TEST8, VSYNC, YS, $\overline{CSYNC}$, TEST10, TEST11, FSCO: I_{OH} = –0.5 mA	$V_{DD}1$ – 1		$V_{DD}1$	V
Output low-level voltage	V_{OL}	TEST3, DO, PSC1, PSC2, $\overline{WAIT}$, $\overline{INT}$, BFP, $\overline{WE}$, $\overline{RAS}$, A0 to A7, $\overline{CAS}$, $\overline{OE}$, DB0 to DB3, TEST8, VSYNC, YS, $\overline{CSYNC}$, TEST10, TEST11, FSCO: I_{OL} = 2.0 mA	V_{SS}		0.4	V
Output off leakage current	I_{OFF}	DB0 to DB3	–5		+5	µA
Internal feedback resistance	R_X	XIN1, XIN2, FSCIN, 4FSC2		1		MΩ
Clock duty	fduty	FSCIN, 4FSC2	40		60	%
8-bit D/A converter reference voltage	V_{REF}	VIDEO1, VIDEO2	2.30		2.50	V
8-bit D/A converter output resistance	R_{DA}	VIDEO1, VIDEO2		300		Ω
Operating current drain	$I_{DD}1$	$AV_{DD}1$		26	40	mA
	$I_{DD}2$	$DV_{DD}1$		26	40	mA

Electrical Characteristics at Ta = 25°C, V_{DD} = 5.0 V, Fscp = 15.625 kHz

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Minimum input pulse width	t_{WH}	CL, high-level pulse width	75			ns
	t_{WL}	CL, low-level pulse width	75			ns
Data setup time	t_{DS}	DI, CL	20			ns
Data hold time	t_{DH}	DI, CL	20			ns
CE setup time	t_{CS}	CE, CL	0			ns
CE hold time	t_{CH}	CE, CL	300			ns
DO setup time	t_{DOS}	DO, CL		30		ns
Data acquisition time	$t_{WT}1$	Serial data acquisition time	150			ns
Data restart time	$t_{WT}2$	Serial data restart time	1.0			µs
Single word write time	t_{WORD}	DI, CL (1 word = 8 bits)	1.35			µs





Basic Specifications

Pin no.	Pin	Pin type	I/O	Polarity	Pin function
1	TEST1	Test input	I	Positive	Test input. Must be connected to ground during normal operation.
2	TEST2	Test input	I	Positive	Test input. Must be connected to ground during normal operation.
3	TEST3	Test output	O	Positive	Test output
4	TEST4	Test input	I	Positive	Test input. Must be connected to ground during normal operation.
5	TEST5	Test input	I	Positive	Test input. Must be connected to ground during normal operation.
6	TEST6	Test input	I	Positive	Test input. Must be connected to ground during normal operation.
7	$DV_{DD}1$	Power supply (+5 V)	—	—	Digital system power supply
8	CE	Enable input	I	Positive	Serial I/O data control input
9	DO	Data output	O	Positive	Serial data output
10	DI	Data input	I	Positive	Serial data input
11	CL	Clock input	I	Positive	Serial data I/O clock input
12	PSC1	Monitor 1 output	O	Positive	Serial input monitor signal output
13	PSC2	Monitor 2 output	O	Positive	Command monitor signal output
14	$\overline{WAIT}$	Wait signal output	O	Negative	Serial input wait signal output (for use with bit maps)
15	$\overline{INT}$	Wait signal output	O	Negative	Serial input wait signal output (for use with the sprite function)
16	TEST7	Test input	I	Positive	Test input. Must be connected to ground during normal operation.
17	$DV_{SS}1$	Ground	—	—	Digital system ground
18	$\overline{WE}$	DRAM output	O	Negative	DRAM write enable signal output
19	$\overline{RAS}$	DRAM output	O	Negative	DRAM row address strobe signal output
20	A0	DRAM output	I/O	Positive	DRAM address (A0) output (Functions as an input in test mode.)
21	A1	DRAM output	I/O	Positive	DRAM address (A1) output (Functions as an input in test mode.)
22	A2	DRAM output	I/O	Positive	DRAM address (A2) output (Functions as an input in test mode.)
23	A3	DRAM output	I/O	Positive	DRAM address (A3) output (Functions as an input in test mode.)
24	A4	DRAM output	I/O	Positive	DRAM address (A4) output (Functions as an input in test mode.)
25	A5	DRAM output	I/O	Positive	DRAM address (A5) output (Functions as an input in test mode.)
26	A6	DRAM output	I/O	Positive	DRAM address (A6) output (Functions as an input in test mode.)
27	A7	DRAM output	I/O	Positive	DRAM address (A7) output (Functions as an input in test mode.)
28	DB0	DRAM input and output	I/O	Positive	DRAM data (D0) input and output
29	$\overline{CAS}$	DRAM output	O	Negative	DRAM column address strobe signal output
30	DB1	DRAM input and output	I/O	Positive	DRAM data (D1) input and output
31	$\overline{OE}$	DRAM output	O	Negative	DRAM read enable signal output
32	DB2	DRAM input and output	I/O	Positive	DRAM data (D2) input and output
33	DB3	DRAM input and output	I/O	Positive	DRAM data (D3) input and output
34	CB	Color bar selection	I	Positive	Low: normal mode, high: color bar output (A pull-down resistor is built in.)
35	TEST8	Test output	O	Positive	Test output
36	$AV_{SS}1$	Ground	—	—	Analog system ground
37	$AV_{DD}1$	Power supply (+5 V)	—	—	Analog system power supply
38	VIDEO1	Video signal (Y) output	O	—	Video (luminance) signal (analog) output (D/A converter output)
39	BIAS	Capacitor connection	O	—	Connections for a ripple exclusion capacitor
40	VIDEO2	Video signal (C) output	O	—	Video (chrominance) signal (analog) output (D/A converter output)
41	BFP	Burst flag signal output	O	Positive	Burst signal output timing flag output
42	LINE	Line count selection	I	—	Line count selection NTSC mode - Low: 263H, high: 262H PAL mode - Low: 314H, high: 312H
43	FSCIN	Clock input	I	Positive	Superimpose subcarrier clock input (A feedback resistor is built in.)
44	VSYNC	Vertical synchronization output	O	Negative	Vertical synchronizing signal output
45	TEST9	Test input	I	Positive	Test input. Must be connected to ground during normal operation. (A pull-down resistor is built in.)
46	YS	Superimpose output	O	Negative	Superimpose control output
47	$\overline{CSYNC}$	Composite synchronization output	O	Negative	Composite synchronizing signal output
48	4FSC2	Clock input	I	Positive	External clock input for the superimpose function (A feedback resistor is built in.)
49	TEST10	Test output	O	Positive	Test output
50	TEST11	Test output	O	Positive	Test output

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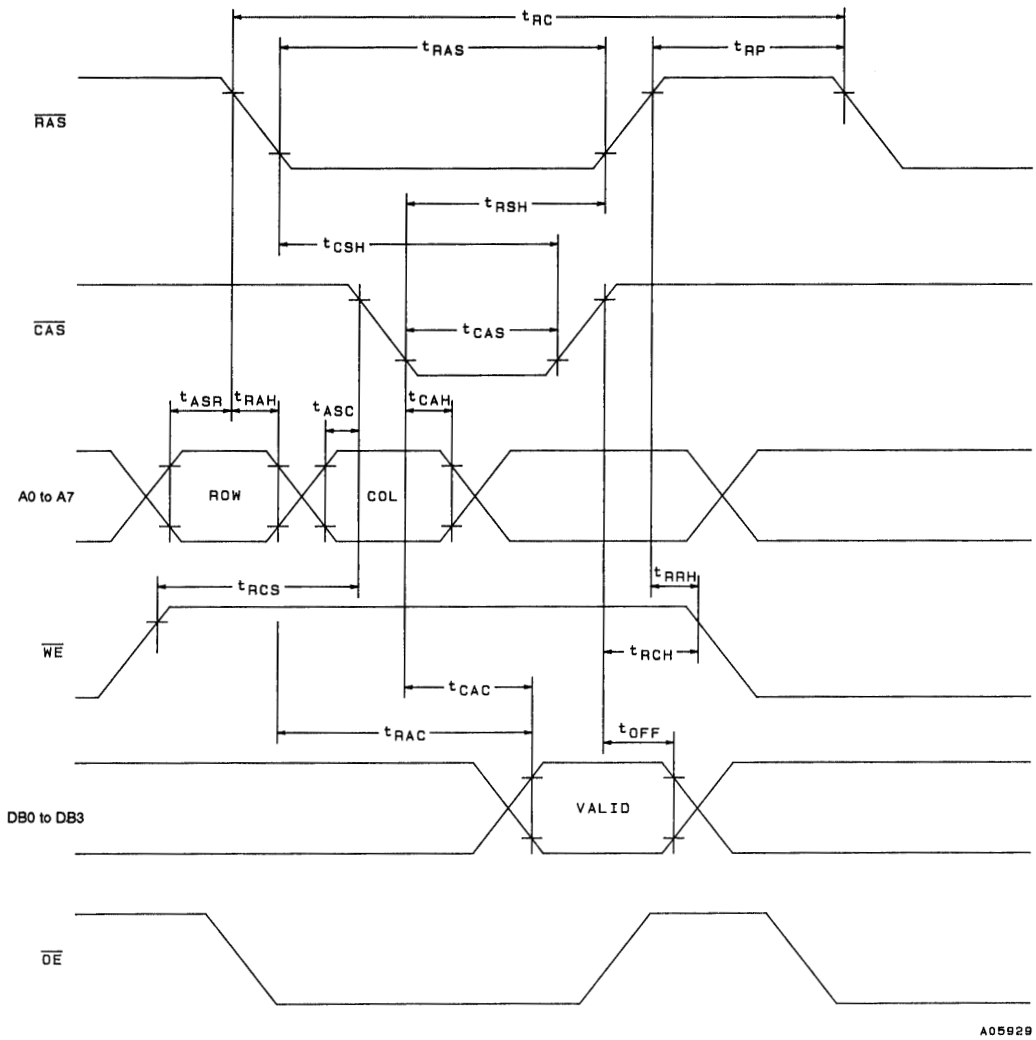
Pin no.	Pin	Pin type	I/O	Polarity	Pin function
51	TEST12	Test input	I	Positive	Test input. Must be connected to ground during normal operation.
52	PALID	PAL mode external control input	I	Positive	External superimpose function control input for PAL mode (A pull-up resistor is built in.)
53	$\overline{\text{HRESET}}$	External horizontal synchronization input	I	Negative	External horizontal synchronization timing control input
54	FSCO	Clock output	O	Positive	Subcarrier clock output NTSC mode: 3.579545 MHz PAL mode: 4.433619 MHz
55	$\overline{\text{VRESET}}$	External vertical synchronization input	I	Negative	External vertical synchronization timing control input
56	$\overline{\text{INIT}}$	Initialization input	I	Negative	System initialization signal input
57	$\overline{\text{RESET}}$	Reset input	I	Negative	System reset signal input
58	N/P1	NTSC/PAL selection	I	Positive	NTSC/PAL selection input (RGB encoder block) High: NTSC, low: PAL
59	N/P2	NTSC/PAL selection	I	Positive	NTSC/PAL selection input (decoder block) High: NTSC, low: PAL
60	SON	Superimpose control	I	Positive	Superimpose function on/off control input High: superimpose on
61	XIN2	Crystal oscillator element connections	I	—	Connections for the PAL crystal oscillator element (4·fsc = 17.734476 MHz)
62	XOUT2		O	—	
63	XIN1	Crystal oscillator element connections	I	—	Connections for the NTSC crystal oscillator element (4·fsc = 14.31818 MHz)
64	XOUT1		O	—	

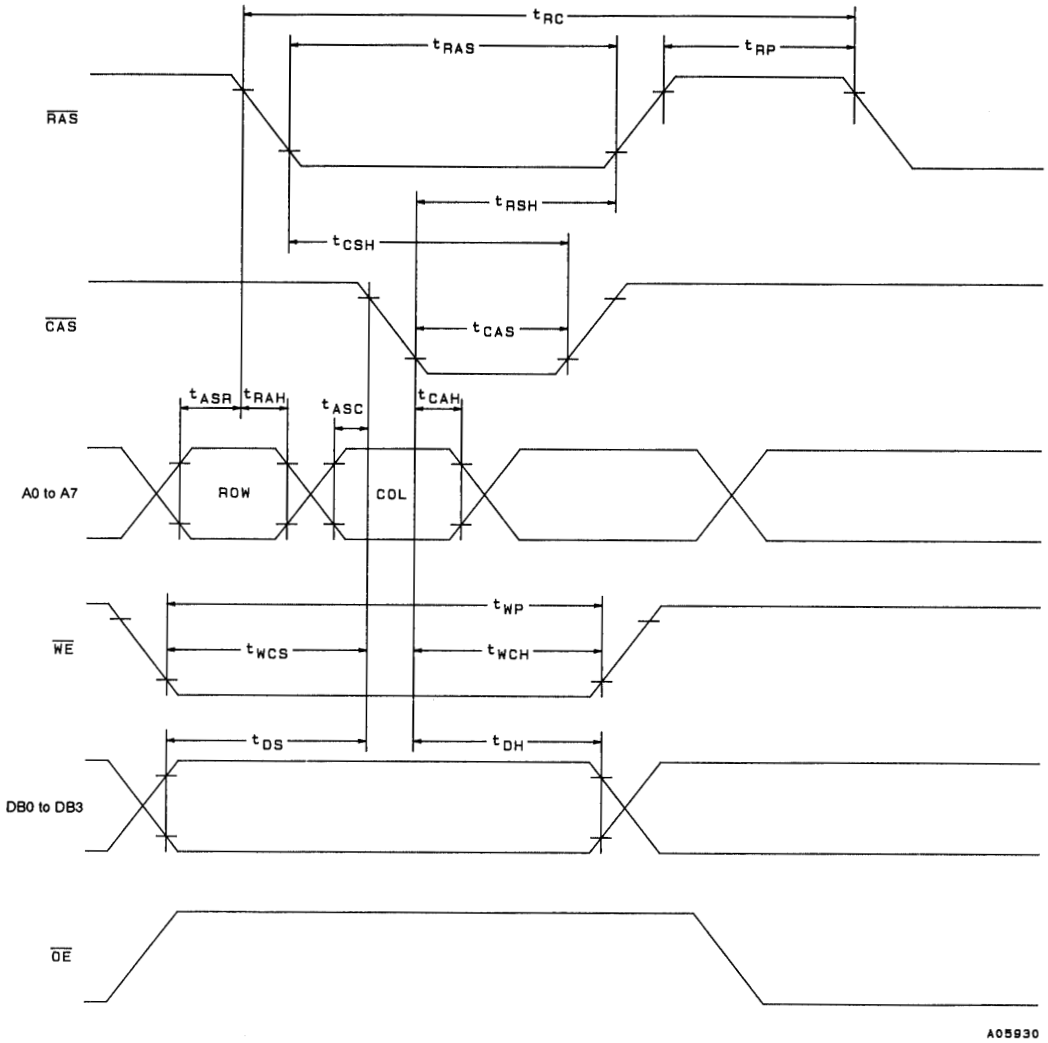
Timing Characteristics (DRAM access timing) at Ta = +25°C, $DV_{DD}1$ = 5 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Random read/write cycle	t_{RC}		250			ns
Page mode cycle	t_{PC}		130			ns
$\overline{\text{RAS}}$ access time	t_{RAC}				210	ns
$\overline{\text{CAS}}$ access time	t_{CAC}				10	ns
Output turn off delay	t_{OFF}				20	ns
$\overline{\text{RAS}}$ precharge time	t_{RP}		100			ns
$\overline{\text{RAS}}$ pulse width	t_{RAS}		120			ns
$\overline{\text{RAS}}$ pulse width (page mode)	t_{RASP}				18000	ns
$\overline{\text{RAS}}$ hold time	t_{RSH}		60			ns
$\overline{\text{CAS}}$ hold time	t_{CSH}		120			ns
$\overline{\text{CAS}}$ pulse width	t_{CAS}		60			ns
$\overline{\text{CAS}}$ precharge time	t_{CPN}		50			ns
$\overline{\text{CAS}}$ precharge time	t_{CP}	Page mode	50			ns
Row address setup time	t_{ASR}		100			ns
Row address hold time	t_{RAH}		50			ns
Column address setup time	t_{ASC}		0			ns
Column address hold time	t_{CAH}		50			ns
Read command setup time	t_{RCS}		150			ns
Read command hold time	t_{RCH}	Referenced to $\overline{\text{CAS}}$	120			ns
Read command hold time	t_{RRH}	Referenced to $\overline{\text{RAS}}$	120			ns
Write command setup time	t_{WCS}		100			ns
Write command hold time	t_{WCH}		50			ns
Write command pulse width	t_{WP}		150			ns
Write data setup time	t_{DS}		100			ns
Write data setup time	t_{DH}		100			ns
$\overline{\text{CAS}}$ setup time	t_{CSR}	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$	50			ns
$\overline{\text{CAS}}$ hold time	t_{CHR}	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$	50			ns
$\overline{\text{RAS}}$ precharge $\overline{\text{CAS}}$ active time	t_{RPC}		50			ns
Refresh time	t_{REF}				3.5	ms

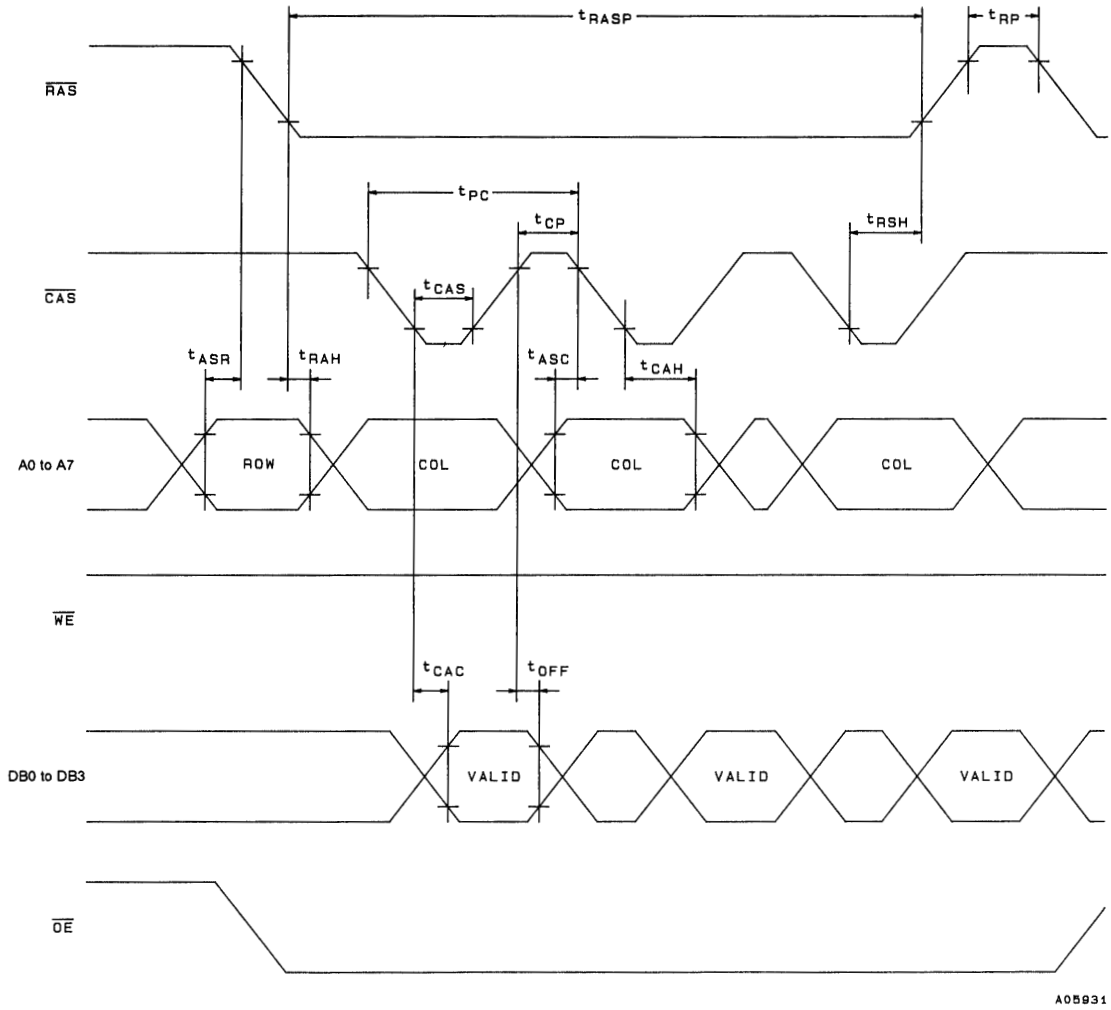
1. DRAM read cycle



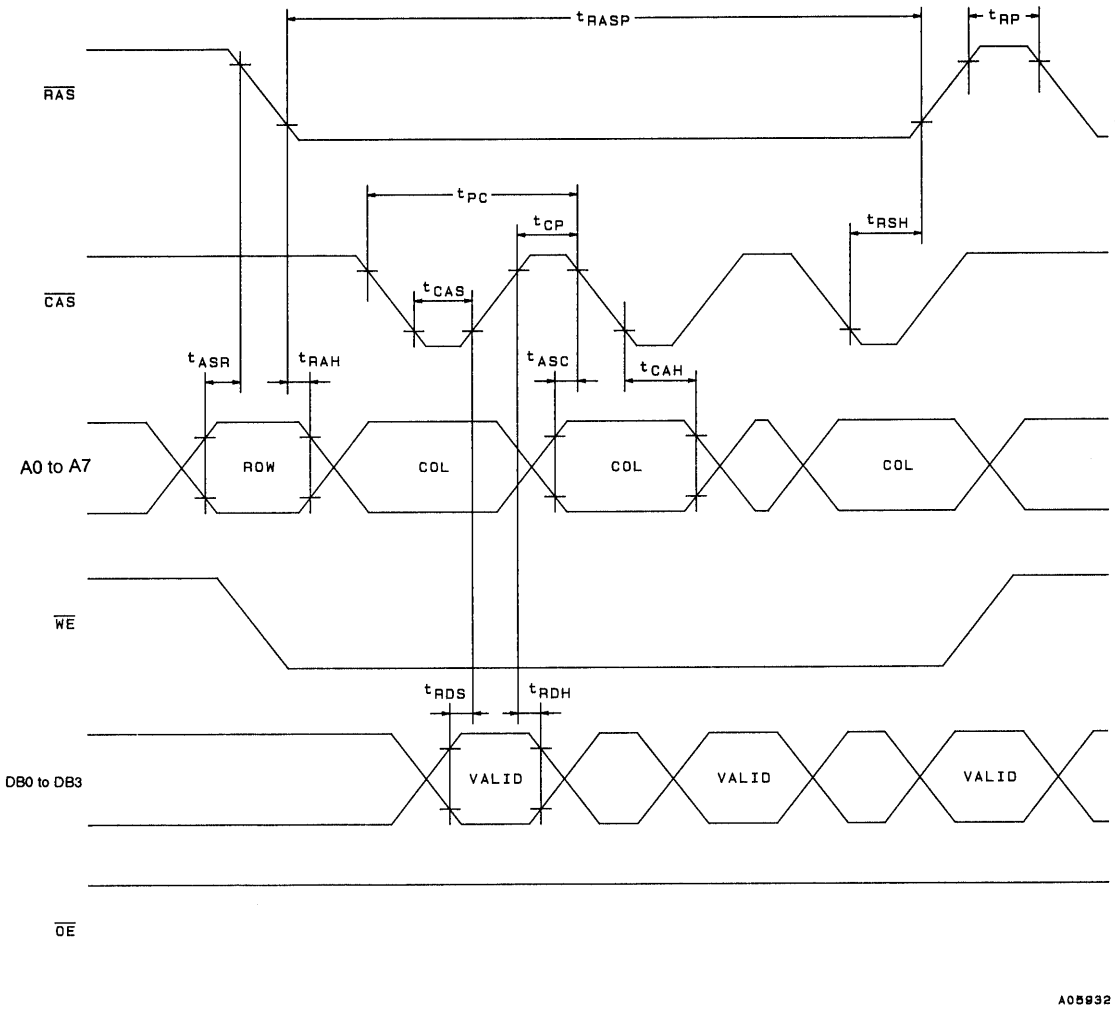
2. DRAM Early write cycle



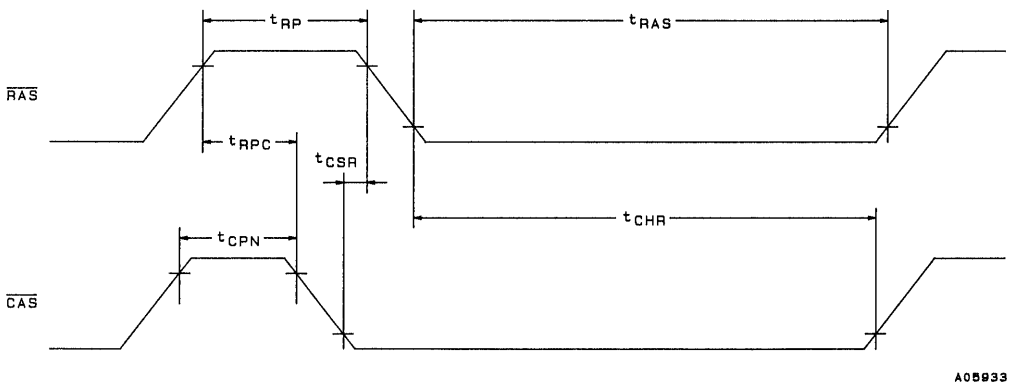
3. DRAM page mode read cycle



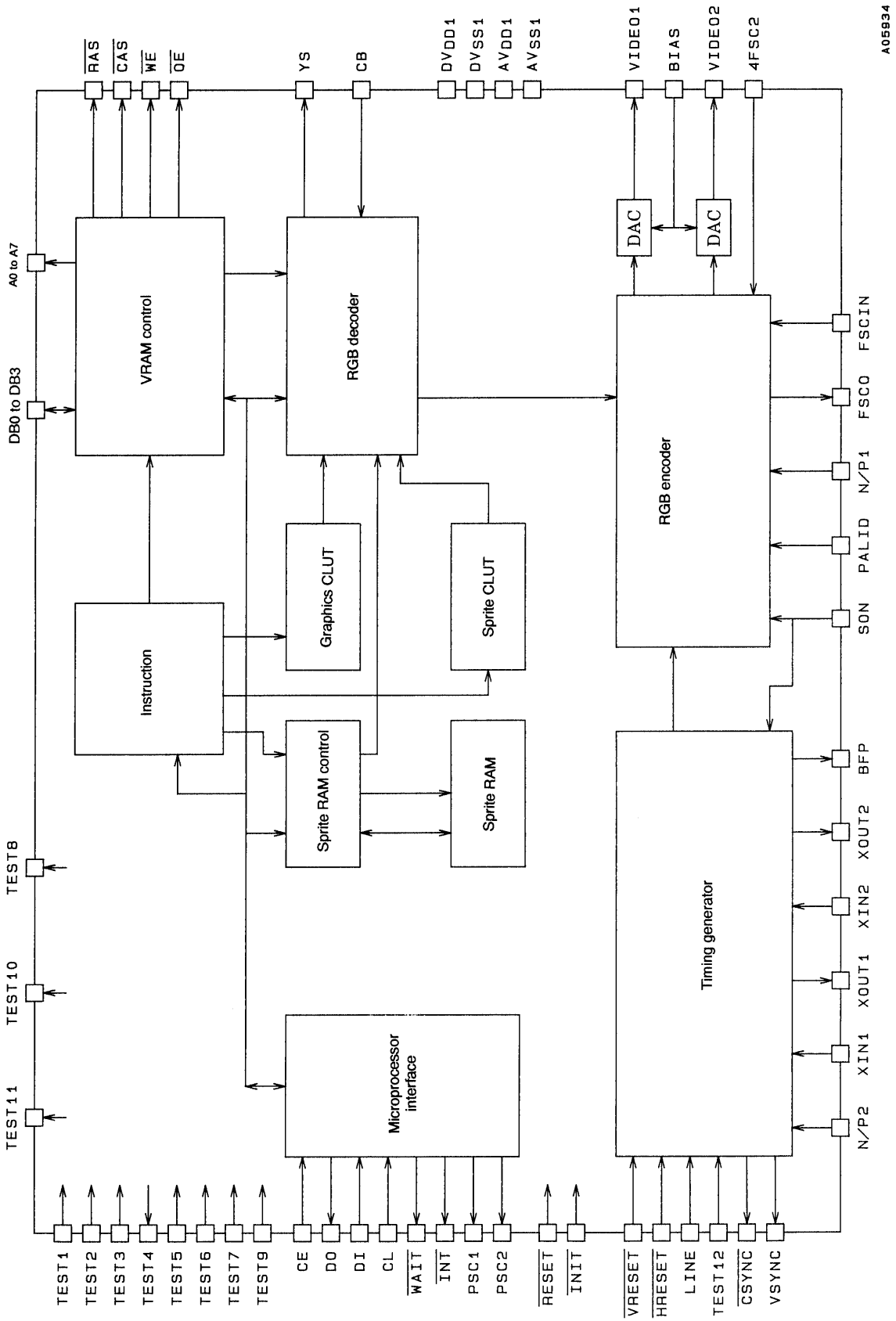
4. DRAM page mode write cycle



5. DRAM $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle



Block Diagram

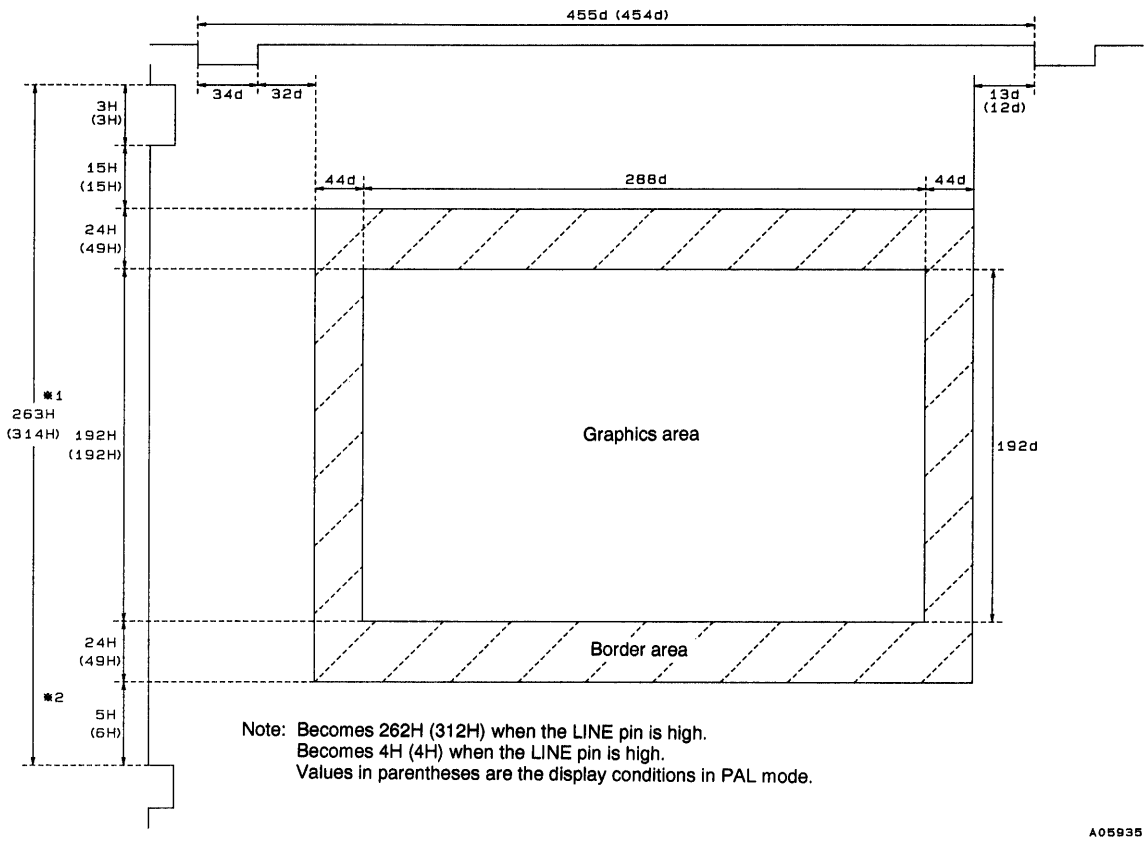


Function Overview

1. Crystal clock oscillator; XIN1, XOUT1, XIN2, XOUT2, N/P1, N/P2, FSCO
   The XIN1 and XOUT1 pins are connections for an NTSC 14.31818-MHz crystal element, and the XIN2 and XOUT2 pins are connections for a PAL 17.734476-MHz crystal element. The N/P1 pin switches the LC78711E RGB encoder block between NTSC and PAL modes, and the N/P2 pin switches the decoder block between NTSC and PAL modes. The FSCO pin outputs a clock signal that is the crystal oscillator frequency divided by 4. The table below enumerates the pin states vs. the LC78711E operating modes.

XIN1, XOUT1	XIN2, XOUT2	N/P1	N/P2	TV format	FSCO
14.31818 MHz	*	H	H	NTSC/M	3.579545 MHz
*	17.734476 MHz	L	L	PAL/GBIDH	4.433619 MHz
14.30244 MHz	*	L	H	PAL/M	3.575611 MHz

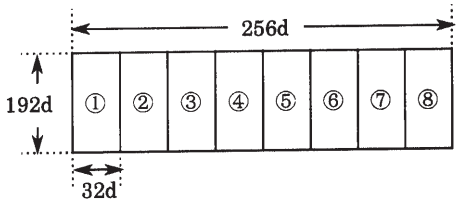
2. Display format; N/P1, N/P2, LINE, $\overline{\text{CSYNC}}$, SON, 4FSC2, FSCIN, $\overline{\text{VRESET}}$, $\overline{\text{HRESET}}$, YS, PALID
   - The LC78711E supports both NTSC and PAL modes, with the N/P1 and N/P2 pins being used to set the mode. See item (1) above for the pin states in the NTSC and PAL modes. The LINE pin switches the number of scan lines in a 1-V period.
   - The SON, 4FSC2, FSCIN, $\overline{\text{VRESET}}$, $\overline{\text{HRESET}}$, YS, and PALID pins are used with the superimpose function. The 4FSC2 pin inputs a 4 × fsc frequency, and the FSCIN pin inputs the fsc frequency. The $\overline{\text{VRESET}}$ and $\overline{\text{HRESET}}$ pins input the external video signal $\overline{\text{VSYNC}}$ and $\overline{\text{HSYNC}}$. The internal V and H counters are reset on the falling edges of these signals, respectively. The image may be disrupted if the 4FSC2 signal is not locked with the $\overline{\text{VRESET}}$ and $\overline{\text{HRESET}}$ signals. The YS pin is used to switch the video signal. The PALID pin is used for burst waveform phase matching in PAL mode.



3. DRAM interface
   Interface pins: A0 to A7, DB0 to DB3, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$
   An external 64k × 4-bit DRAM must be used.
4. Video outputs: VIDEO1, VIDEO2
   The luminance signal can be acquired from the VIDEO1 pin.
   The chrominance signal can be acquired from the VIDEO2 pin.

5. Color bar output; CB

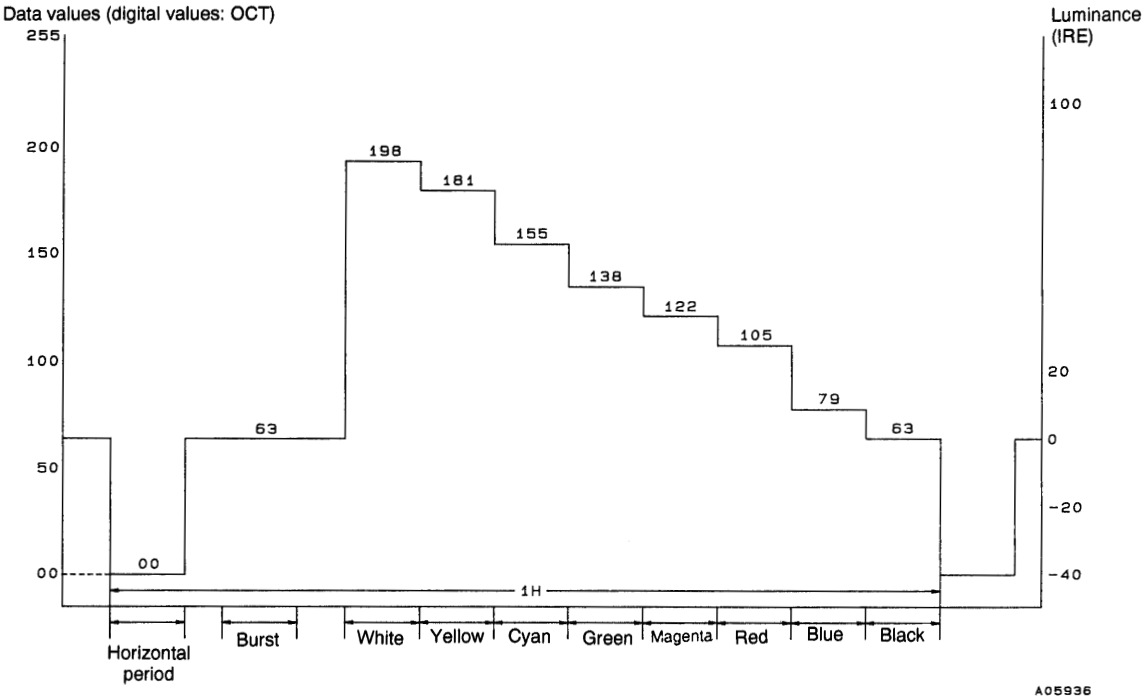
If the CB input pin is set high, a color bar signal will be output from the VIDEO1 and VIDEO2 pins. The table below lists the content of the color bar signal.



	R	G	B
① White	F	F	F
② Gray	B	B	B
③ Yellow	F	F	O
④ Cyan	O	F	F
⑤ Green	O	F	O
⑥ Magenta	F	O	F
⑦ Red	F	O	O
⑧ Blue	O	O	F
Border (black)	O	O	O

6. Color bar signal output level

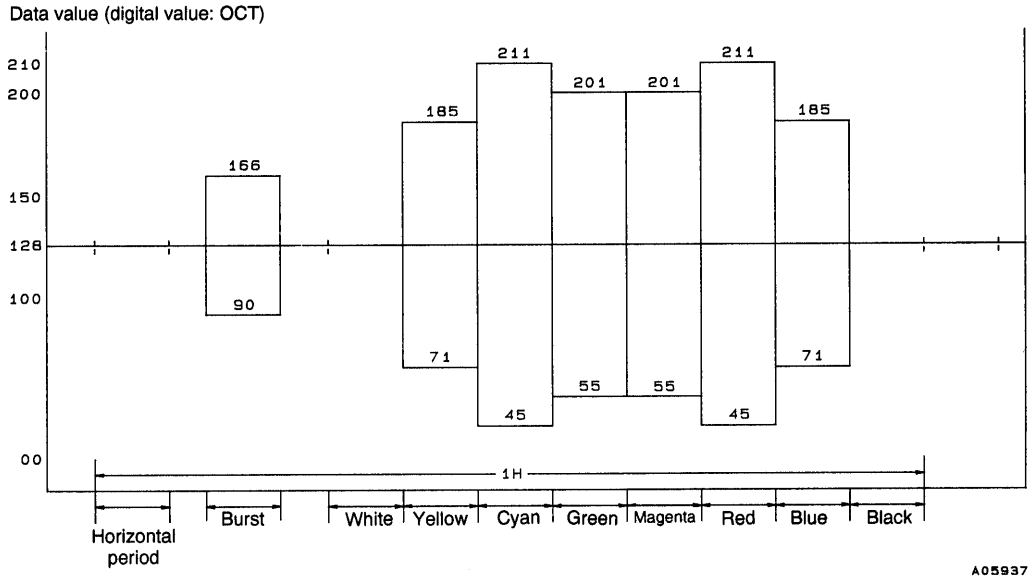
- Luminance signal output level (Y signal: VIDEO1, pin 38)



Data value	Output voltage (V)	Luminance level (IRE)
255	4.990	121.9
220	4.648	100
198	4.434	85.7
181	4.268	74.9
155	4.014	58.4
138	3.848	47.6
122	3.691	37.5
105	3.525	26.7
79	3.271	10.2
63	3.125	0
0	2.500	–40

Note: $AV_{DD}1$ = 5.00 V

- Chrominance signal output level (C signal: VIDEO2, pin 40)



Data value	Output voltage (V)	Luminance level (IRE)
255	4.990	81.2
211	4.560	52.7
201	4.463	46.3
185	4.306	36.2
166	4.121	24.1
128	3.750	0
90	3.379	–24.1
71	3.193	–36.2
55	3.037	–46.3
45	2.939	–52.7
0	2.500	–81.2

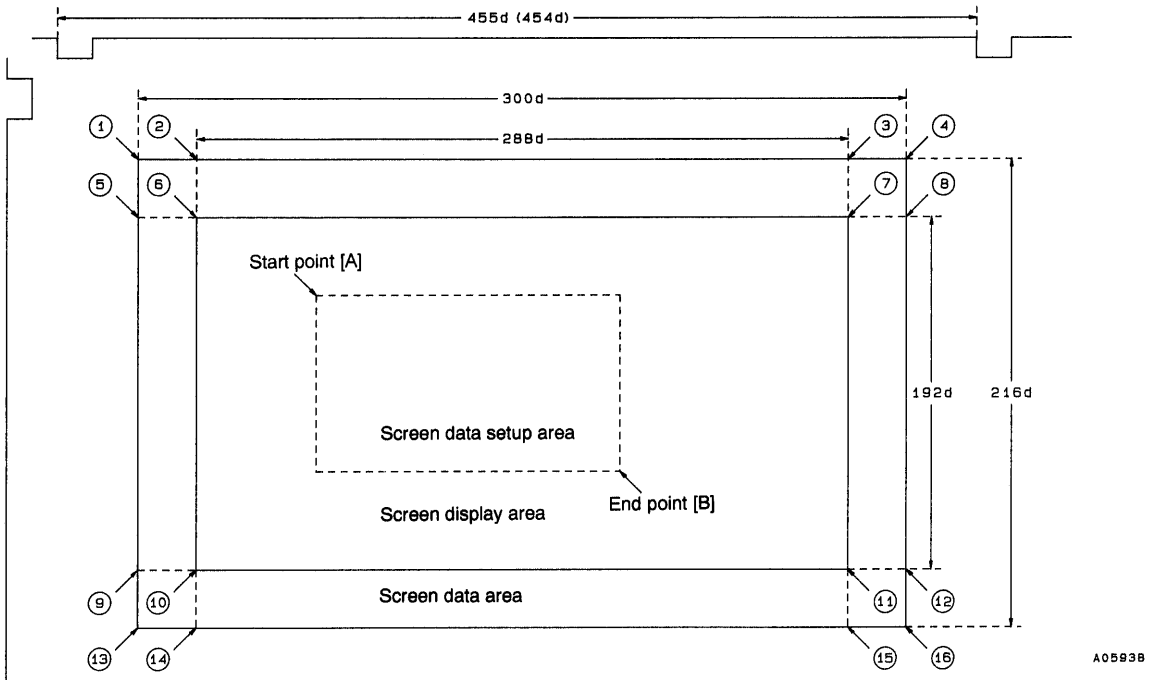
Note: $AV_{DD}1$ = 5.00 V

Drawing Display Functions

1. Operating mode (scan operation, display operation)
   NTSC mode:
   - Non-interlaced 60 Hz (262 or 263 lines)
   - Dot clock 2fsc: 7.15909 MHz (T = 139.67 ns)
   - System clock 4fsc: 14.31818 MHz

   PAL mode:
   - Non-interlaced 50 Hz (312 or 314 lines)
   - Dot clock 4fsc × 2/5: 7.09379 MHz (T = 140.97 ns)
   - System clock 4fsc: 17.734476 MHz
2. Display functions
   - Display resolution 288 dots × 192 H
   - Screen data area 300 dots × 216 H
   - 16-color display 16 colors selected from a palette of 4096 colors

3. Sprite screen (cursor display)
   - Sprite screen: Two types, 32 dots × 32 H
   - Sprite color: Seven display colors plus transparent display (7 colors selected from 4096 colors)
     This color setting selects colors that are independent of the bit-mapped screens.
4. Cross cursor display
   - The X and Y coordinates are set.
     A cross cursor is displayed at the point corresponding to the specified coordinates.
5. Display window area function
   - A rectangular window is specified by specifying the X and Y coordinates for two points.
     Either the area within the display window, or the area outside the display window can be specified to be transparent (border color display).
6. Scrolling display function
   - Scrolling in the vertical and horizontal directions
   - The scroll amount can be set.
     The scroll amount is set in units of 1 to 6 dots in the horizontal direction and 1 to 12 dots in the vertical direction.
     Text with 50 characters in the horizontal direction and 18 characters in the vertical direction can be set up in single character units.
7. Graphics display format



Graphics coordinates

	X direction (horizontal direction)	Y direction (vertical direction)		X direction (horizontal direction)	Y direction (vertical direction)
1	000hex (000oct)	00hex (00oct)	9	000hex (000oct)	CBhex (203oct)
2	006hex (006oct)	00hex (00oct)	10	006hex (006oct)	CBhex (203oct)
3	125hex (293oct)	00hex (00oct)	11	125hex (293oct)	CBhex (203oct)
4	12Bhex (299oct)	00hex (00oct)	12	12Bhex (299oct)	CBhex (203oct)
5	000hex (000oct)	0Chex (12oct)	13	000hex (000oct)	D7hex (215oct)
6	006hex (006oct)	0Chex (12oct)	14	006hex (006oct)	D7hex (215oct)
7	125hex (293oct)	0Chex (12oct)	15	125hex (293oct)	D7hex (215oct)
8	12Bhex (299oct)	0Chex (12oct)	16	12Bhex (299oct)	D7hex (215oct)

Writing graphics data

[A] Set up point (Xs, Ys): X is a 9-bit address.
[B] Set up point (Xe, Ye): Y is an 8-bit address.

1. Begin writing color codes from the origin coordinate address (Xs, Ys).
2. If the X direction address (Xs) matches the endpoint address (Xe), reset the X address to the origin address (Xs). At the same time, increment the Y address by one count.
3. Terminate writing when the endpoint address (Xe, Ye) is reached.
   - At termination, reset the address to the origin address (Xs, Ys) and exit.
   - Terminate writing even if the CE pin has gone low. In this case, the address will be set to the endpoint address plus one and the algorithm will exit.
   - The address manipulations described above, are for the case where automatic address incrementing has been set up by command.

1. When writing to the graphics display area, specify the address of the origin [A] to be 6 and the address of the endpoint [B] to be 11.
2. When writing to a rectangular area, the origin [A] and the endpoint [B] can be set to arbitrary values.
   When filling is specified by command, RAM data will be set to the first specified color code.
   In this case, it suffices to write the color code that was specified at that point. However, add the condition that the color code setting must not be changed during the fill operation.
3. When writing a straight line, set either the X (horizontal) values or Y (vertical) values of the origin [A] and endpoint [B] to the same value.
   For example, to draw a straight line in the vertical direction, set the origin [A] to (Xs, Ys) and set the endpoint [B] to (Xs, Ye).
   To draw a straight line in the horizontal direction, set the origin [A] to (Xs, Ys) and set the endpoint [B] to (Xe, Ys).
   Filling must be specified by command to write straight lines.
4. Set up the addresses as follows to write scroll data.
   For example,
   To scroll down, specify 2 as the origin [A] and 7 as the endpoint [B].
   To scroll right, specify 5 as the origin [A] and 9 as the endpoint [B].
   To scroll left, specify 7 as the origin [A] and 12 as the endpoint [B].
   To scroll up, specify 10 as the origin [A] and 15 as the endpoint [B].

Reading out color codes for specific bits

It is possible to read out (not write) the color code for a given dot by using a command to set the origin address (Xs, Ys). Executing the read out command latches the data into the serial output shift register. The command manipulation terminates when the data for a single dot has been read out. (The command register is reset.)

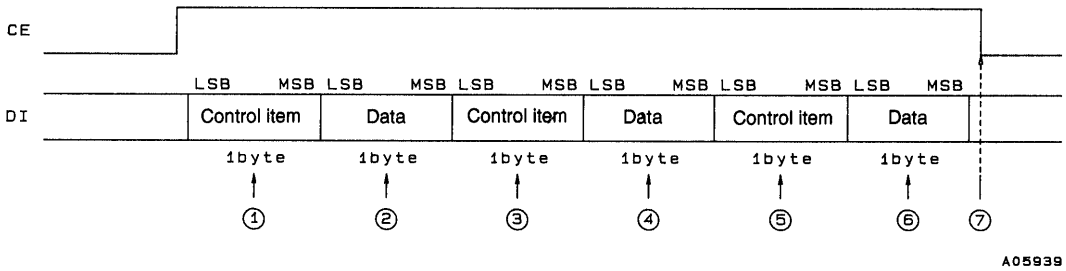
Graphics display priority order

1. Cross cursor
2. Sprite A pattern
3. Sprite B pattern
4. Graphics screen
5. Border screen
6. Background screen (not displayed during graphics display)

Note: There are cases where the same pattern is displayed for sprite patterns A and B. Thus the LC78711E may be in a state of accessing the same sprite RAM. Therefore, a time difference must be set up for the sprite pattern accesses (reads) for the A and B patterns.

Microprocessor Interface

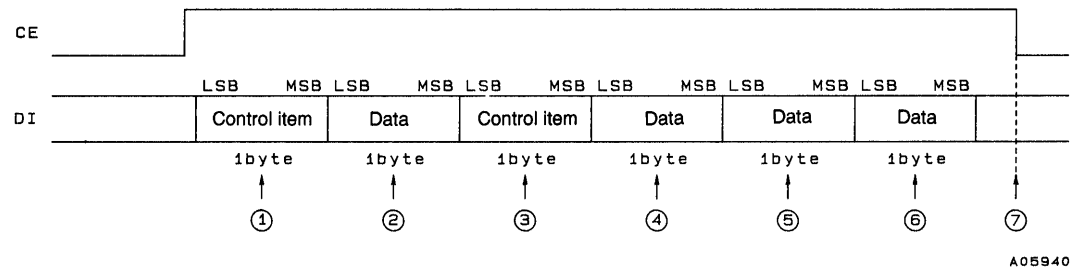
1. Data transfer format (for command transfers)
   - A command identification code (control item) must be transferred before the data is transferred when setting up commands, positions (coordinates), or color codes (color table).
   - If continuous data transfer mode is not set up, then data transfers of bit map data and sprite (cursor) data also require that a command identifier code (control item) be transferred before the data is transferred.
   - Transfer format (example)



①, ③, ⑤: Command identification code (control item)
②, ④, ⑥: Command register setup data
⑦: Serial transfer completes

2. Transfer format (when continuous data transfer mode has been set up)
   - Continuous data transfer mode must be set up by the data (1 byte) that follows a command identification code (control item). When a RAM data transfer command is set up and the data transfer started, the data that follows (in byte units) is all acquired as RAM data.

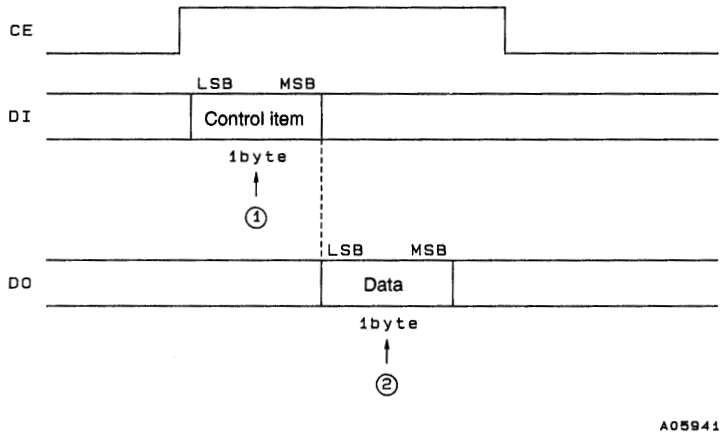
     Note: If continuous data transfer mode is set up, the RAM write address must be set (by command) to automatic increment mode.
   - Transfer format (example)



①, ③: Command identification code (control item)
②: Command register setup data
④, ⑤, ⑥: RAM data
⑦: Serial transfer completes and continuous data transfer mode is cleared.

Note: When continuous data transfer mode is cleared, the command register setting is not reset. If the control microprocessor immediately issues a RAM data transfer command and starts the data transfer, the LC78711E will switch to continuous data transfer mode once again.

3. Transfer format (when a check command is issued)
   • Transfer format (example)



①: Control item (address = first byte: 11hex)
②: Data (check flags)

Control Commands

Command	First byte								Second byte							
	MSB		Control item code					LSB	MSB			Data				LSB
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Register 00hex (Mode setup)	0	0	0	0	0	0	0	0	INIT	SCP2	SCP1	SCP0	CB	1	0	VRAM/ BG
Register 01hex (Screen position fine adjustment)	0	0	0	0	0	0	0	1	VP3	VP2	VP1	VP0	HP3	HP2	HP1	HP0
Register 04hex (Color: RG settings)	0	0	0	0	0	1	0	0	CRG3	CRG2	CRG1	CRG0	CRR3	CRR2	CRR1	CRR0
Register 05hex (Color: B settings)	0	0	0	0	0	1	0	1	CROS	CRKY	BGCL	0	CRB3	CRB2	CRB1	CRB0
Register 06hex (Burst phase setting; when SON = 1)	0	0	0	0	0	1	1	0	R/F	0	0	0	0	BST ON	PH1	PH0
Register 07hex (YS output phase adjustment)	0	0	0	0	0	1	1	1	0	0	0	0	YT3	YT2	YT1	YT0
Register 08hex (External synchronization on/off)	0	0	0	0	1	0	0	0	MVMD	EXSN	0	0	TST3	TST2	TST1	TST0
Register 09hex (Subtitle scrolling: up/down)	0	0	0	0	1	0	0	1	0	0	0	SCV4	SCV3	SCV2	SCV1	SCV0
Register 0Ahex (Subtitle scrolling: left/right)	0	0	0	0	1	0	1	0	0	0	SCH5	SCH4	SCH3	SCH2	SCH1	SCH0
Register 8Bhex (Scrolling control: vertical direction)	1	0	0	0	1	0	1	1	SCRV 1	SCRV 0	0	0	SRFV 3	SRFV 2	SRFV 1	SRFV 0
Register 8Chex (Scrolling control: horizontal direction)	1	0	0	0	1	1	0	0	SCRH 1	SCRH 0	0	0	0	SRFH 2	SRFH 1	SRFH 0
Register 0Dhex (Graphics mode setup)	0	0	0	0	1	1	0	1	0	0	0	0	0	DCRS	DSPB	DSPA
Register 0Ehex (Pin PSC1 output control)	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	SRO ENM
Register 0Fhex (Pin PSC2 output control)	0	0	0	0	1	1	1	1	0	0	0	0	CRSM	SPBM	SPAM	GPHM
Register 11hex	0	0	0	1	0	0	0	1	0	0	0	0	0	VBLK	EXEC	1

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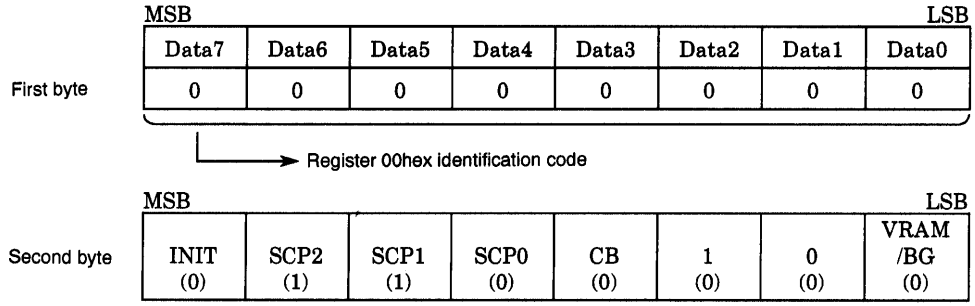
Command	First byte								Second byte							
	MSB Control item code LSB								MSB Data LSB							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Register 20hex (Color data settings: R, G)	0	0	1	0	0	0	0	0	SGCG3	SGCG2	SGCG1	SGCG0	SGCR3	SGCR2	SGCR1	SGCR0
Register 21hex (Color data settings: B)	0	0	1	0	0	0	0	1	0	0	0	0	SGCB3	SGCB2	SGCB1	SGCB0
Register A2hex (Color data settings)	1	0	1	0	0	0	1	0	0	0	0	0	SCPC3	SCPC2	SCPC1	SCPC0
Register A3hex (Border color setting)	1	0	1	0	0	0	1	1	0	0	0	0	SBDC3	SBDC2	SBDC1	SBDC0
Register 24hex (Bit map address setting)	0	0	1	0	0	1	0	0	BMAY7	BMAY6	BMAY5	BMAY4	BMAY3	BMAY2	BMAY1	BMAY0
Register 25hex (Bit map address setting)	0	0	1	0	0	1	0	1	BMAX7	BMAX6	BMAX5	BMAX4	BMAX3	BMAX2	BMAX1	BMAX0
Register 26hex (Write control setting)	0	0	1	0	0	1	1	0	0	R/W	0	STRP/ ENDP	FILL COLR	BMAI	BMDF	BMAX8
Register A7hex (Bit map data setting)	1	0	1	0	0	1	1	1	BMD7	BMD6	BMD5	BMD4	BMD3	BMD2	BMD1	BMD0
Register 28hex (Color data settings: R, G)	0	0	1	0	1	0	0	0	SSPG3	SSPG2	SSPG1	SSPG0	SSPR3	SSPR2	SSPR1	SSPR0
Register 29hex (Color data settings: B)	0	0	1	0	1	0	0	1	0	0	0	0	SSPB3	SSPB2	SSPB1	SSPB0
Register AAhex (Sprite settings)	1	0	1	0	1	0	1	0	0	0	0	0	0	SSPC2	SSPC1	SSPC0
Register 2Bhex (Sprite address Y setting)	0	0	1	0	1	0	1	1	0	0	0	SPARY4	SPARY3	SPARY2	SPARY1	SPARY0
Register 2Chex (Sprite address X setting)	0	0	1	0	1	1	0	0	0	0	0	SPARX4	SPARX3	SPARX2	SPARX1	SPARX0
Register 2Dhex (Write control settings)	0	0	1	0	1	1	0	1	0	0	0	0	WSP2	WSP1	SPAI	SPDF
Register AEhex (Sprite data setting)	1	0	1	0	1	1	1	0	0	SPD6	SPD5	SPD4	0	SPD2	SPD1	SPD0
Register 2Fhex (Sprite A and B settings)	0	0	1	0	1	1	1	1	0	0	0	0	0	SPRT ARA	SPSB	SPSA
Register 30hex (Sprite display address Y setting)	0	0	1	1	0	0	0	0	SPDA Y7	SPDA Y6	SPDA Y5	SPDA Y4	SPDA Y3	SPDA Y2	SPDA Y1	SPDA Y0
Register 31hex (Sprite display address X setting)	0	0	1	1	0	0	0	1	SPDA X7	SPDA X6	SPDA X5	SPDA X4	SPDA X3	SPDA X2	SPDA X1	SPDA X0
Register 32hex (Sprite display address setting control)	0	0	1	1	0	0	1	0	0	0	0	0	WSPB	WSPA	0	SPDA X8
Register 33hex (Display window setting: Y)	0	0	1	1	0	0	1	1	WDYS7	WDYS6	WDYS5	WDYS4	WDYS3	WDYS2	WDYS1	WDYS0
Register 34hex (Display window setting: X)	0	0	1	1	0	1	0	0	WDXS7	WDXS6	WDXS5	WDXS4	WDXS3	WDXS2	WDXS1	WDXS0
Register 35hex (Display window: X; display area settings)	0	0	1	1	0	1	0	1	0	0	WDEN	WDAR	PAL 60	SADR/ EADR	0	WDXS8
Register 36hex (Cross cursor display position setting: X)	0	0	1	1	0	1	1	0	CRAX7	CRAX6	CRAX5	CRAX4	CRAX3	CRAX2	CRAX1	CRAX0
Register 37hex (Cross cursor display position setting: Y)	0	0	1	1	0	1	1	1	CRAY7	CRAY6	CRAY5	CRAY4	CRAY3	CRAY2	CRAY1	CRAY0

Command Descriptions

Note: 1. After a hardware reset, always first send register 00 command, and only then issue the various commands. The LC78711E may operate incorrectly if a register 00 command is not issued.
2. All data transfers must be performed LSB first.
3. The (0) and (1) notations in the second byte indicate the default values.

1. Register 00hex

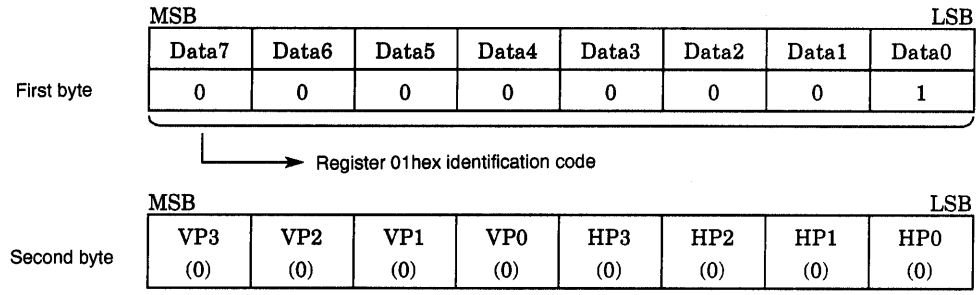


- Data7: INIT
  - — Function: System reset
  - — Operation: INIT = 0: The LC78711E internal state is not reset (normal operation continues)
    INIT = 1: The internal state is reset (The display is set to a blue background screen.)
- Data6: SCP2
  Data5: SCP1
  Data4: SCP0
  - — Function: YS output (pin 46) control
  - — Operation: SCP2 = 0: When (SCP0, SCP1) is (0,0) or (0,1), the whole screen is set to low (transparent) if the comparison condition did not hold.
    SCP2 = 1: When (SCP0, SCP1) is (0,0) or (0,1), the whole screen is set to high (display) if the comparison condition did not hold.
    The superimpose mode comparison condition is determined by the SCP1 and SCP2 setting.
    (Only valid when pin 60, SON, is 1)

SCP1	SCP0	Comparison condition (YS pin output operation setting)
0	0	No comparison performed
1	0	If the border color was not black, YS is set to high (display) for sections that do not match the border color, and set to low (transparent) for all other sections.
1	1	Sets YS high for sections that do not match the chroma key color, and low for all other sections.

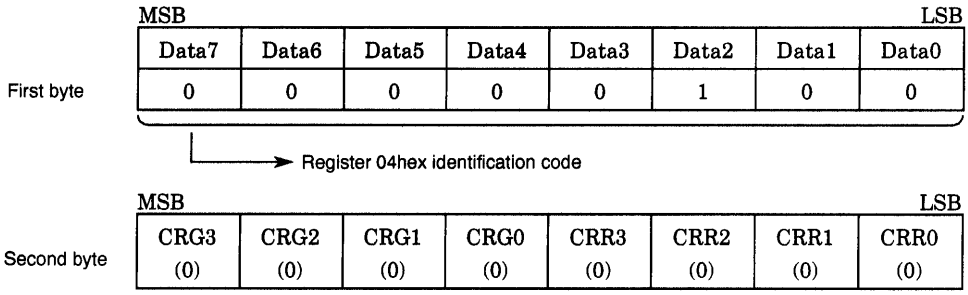
- Data3: CB
  - — Function: Color bar screen output setting
  - — Operation: CB = 0: The graphics signal is output.
    CB = 1: A color bar signal is output.
- Data2: 1
  - — Operation: This bit must always be set to 1. The LC78711E may not operate correctly if this bit is not set to 1.
- Data1: 0
  - — Operation: This bit must always be set to 0. The LC78711E may not operate correctly if this bit is not set to 0.
- Data0: VRAM/BG
  - — Function: Switches the displayed screen
  - — Operation: VRAM/BG = 0: Displays the contents of VRAM
    VRAM/BG = 1: Displays the background color

2. Register 01hex



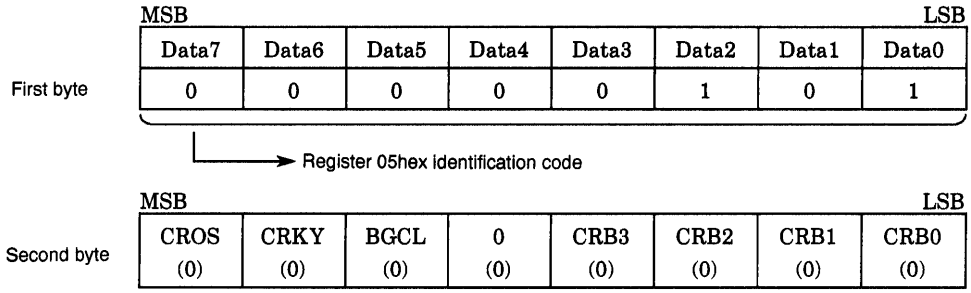
- Data7: VP3
  Data6: VP2
  Data5: VP1
  Data4: VP0
  — Function: These bits set the vertical direction display start position.
  — Operation: Sets the display position as a two's complement value with positive indicating up in the vertical direction. The position is set in two dot units, supporting a range of from –16 to +14 dots from the center position.
- Data3: HP3
  Data2: HP2
  Data1: HP1
  Data0: HP0
  — Function: These bits set the horizontal direction display start position.
  — Operation: Sets the display position as a two's complement value with positive indicating left in the horizontal direction. The position is set in two dot units, supporting a range of from –16 to +14 dots from the center position.

3. Register 04hex



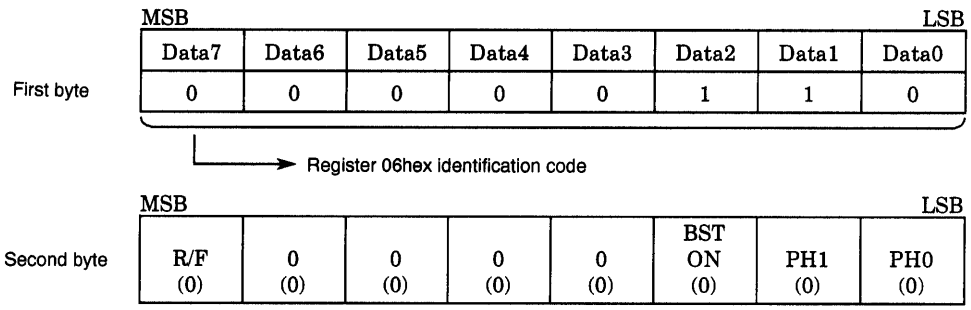
- Data7: CRG3
  Data6: CRG2
  Data5: CRG1
  Data4: CRG0
  — Function: The green color data setting
  — Operation: Specifies the green color data. There are 16 values in the range 0 to F (hexadecimal).
- Data3: CRR3
  Data2: CRR2
  Data1: CRR1
  Data0: CRR0
  — Function: The red color data setting
  — Operation: Specifies the red color data. There are 16 values in the range 0 to F (hexadecimal).

4. Register 05hex



- Data7: CROS
  — Function: Cross cursor display color setting
  — Operation: Acquires the color set in bits CRR3:0, CRG3:0, and CRB3:0 as the cross cursor display color.
- Data6: CRKY
  — Function: Chroma key color setting
  — Operation: Acquires the color set in bits CRR3:0, CRG3:0, and CRB3:0 as the chroma key color.
- Data5: BGCL
  — Function: Background color setting
  — Operation: Acquires the color set in bits CRR3:0, CRG3:0, and CRB3:0 as the background color.
- Data4: Unused (Must be set to 0.)
- Data3: CRB3
  Data2: CRB2
  Data1: CRB1
  Data0: CRB0
  — Function: The blue color data setting
  — Operation: Specifies the blue color data. There are 16 values in the range 0 to F (hexadecimal).

5. Register 06hex

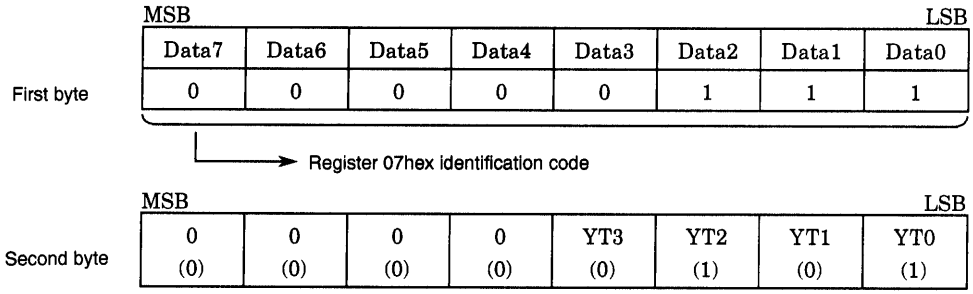


- Data7: R/F
  — Function: Color burst phase timing setting during superimpose operation
  — Operation: R/F = 0: Set to the rising edge of the 4fsc clock
  R/F = 1: Set to the falling edge of the 4fsc clock
- Data6: Unused (Must be set to 0.)
  Data5: Unused (Must be set to 0.)
  Data4: Unused (Must be set to 0.)
  Data3: Unused (Must be set to 0.)
- Data2: BSTON
  — Function: Color burst signal output control setting during superimpose operation
  — Operation: BSTON = 0: Burst signal output is turned off
  BSTON = 1: Burst signal output is turned on

- Data1: PH1
  Data0: PH0
  — Function: Color burst signal phase setting during superimpose operation
  — Operation:

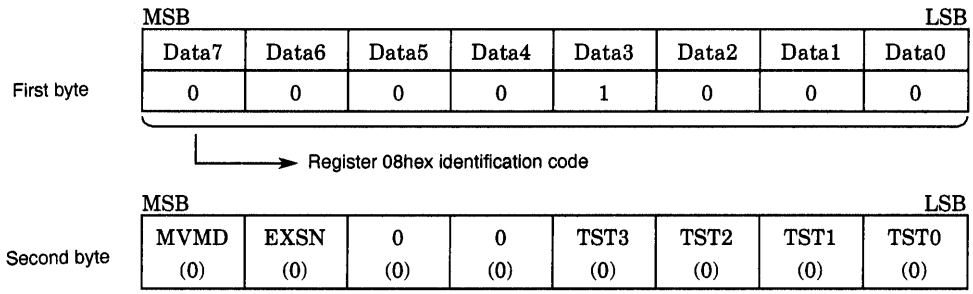
PH1	PH0	Phase
0	0	0°
0	1	90°
1	0	180°
1	1	270°

6. Register 07hex



- Data7: Unused (Must be set to 0.)
  Data6: Unused (Must be set to 0.)
  Data5: Unused (Must be set to 0.)
  Data4: Unused (Must be set to 0.)
- Data3: YT3
  Data2: YT2
  Data1: YT1
  Data0: YT0
  — Function: YS (pin 46) output phase adjustment setting
  — Operation: Sets the YS output timing in single 4fsc clock units. The default is a phase setting identical to that of the video output.

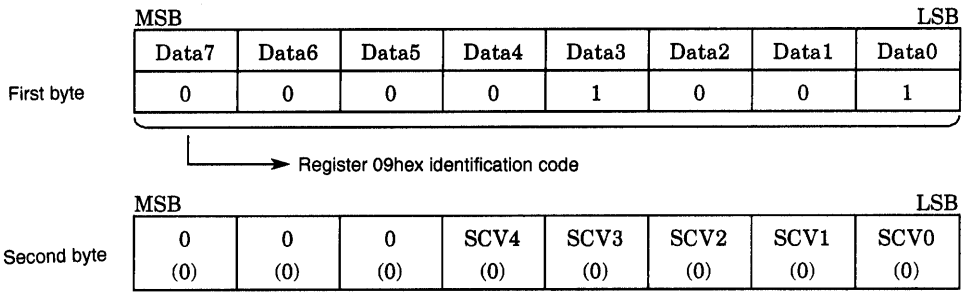
7. Register 08hex



- Data7: MVMD
  — Function: Moving display area setting during superimpose operation
  — Operation: MVMD = 0: Only the display area moves
  MVMD = 1: The area including the border area moves (only left and right motion is possible with this setting.)

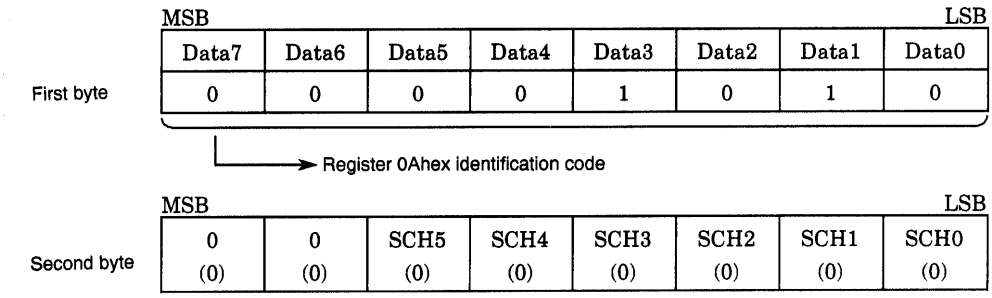
- Data6: EXSN
  — Function: Synchronizing signal reset control setting for external synchronization mode, i.e., when SON = 1.
  — Operation: EXSN = 0: Reset is executed on the falling edge of the $\overline{\text{HRESET}}$ (pin 54) and $\overline{\text{VRESET}}$ (pin 56) signals.
  EXSN = 1: Reset is executed on the falling edge of the $\overline{\text{VRESET}}$ (pin 56) signal. (The $\overline{\text{HRESET}}$ signal is not required.)
- Data5: Unused (Must be set to 0.)
  Data4: Unused (Must be set to 0.)
- Data3: TST3
  Data2: TST2
  Data1: TST1
  Data0: TST0
  — Function: Test mode settings
  — Operation: These bits must be set to 0 during normal operation.

8. Register 09hex



- Data7: Unused (Must be set to 0.)
  Data6: Unused (Must be set to 0.)
  Data5: Unused (Must be set to 0.)
- Data4: SCV4
  Data3: SCV3
  Data2: SCV2
  Data1: SCV1
  Data0: SCV0
  — Function: Subtitle scrolling amount (vertical direction setting in character units)
  — Operation: Scrolls the screen display position up in character units. The scrolling amount can be set to a value in the range 0 to 17 characters, where a single character is 12 vertical dots (12 H).

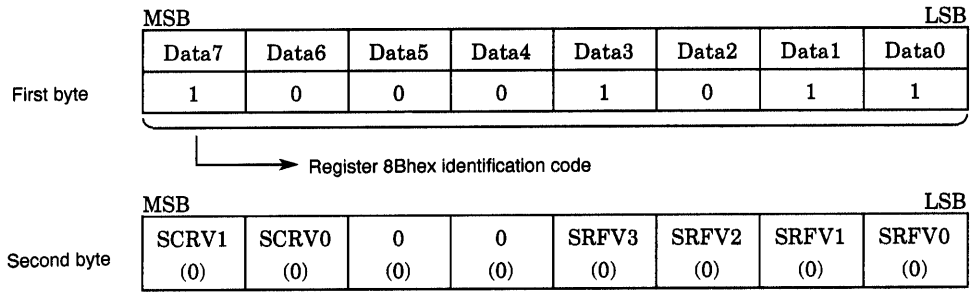
9. Register 0Ahex



- Data7: Unused (Must be set to 0.)
  Data6: Unused (Must be set to 0.)

- Data5: SCH5
  Data4: SCH4
  Data3: SCH3
  Data2: SCH2
  Data1: SCH1
  Data0: SCH0
  — Function: Subtitle scrolling horizontal direction setting
  — Operation: Scrolls the screen display position to the left in character units. The scrolling amount can be set to a value in the range 0 to 49 characters, where a single character is 6 horizontal dots.

10. Register 8Bhex



- Data7: SCRV1
  Data6: SCRV0
  — Function: Scrolling function vertical direction setting
  — Operation:

SCRV0	SCRV1	Scroll direction
0	0	Do not scroll
0	1	Scroll down
1	0	Scroll up
1	1	Illegal value

- Data5: Unused (Must be set to 0.)
  Data4: Unused (Must be set to 0.)
- Data3: SRFV3
  Data2: SRFV2
  Data1: SRFV1
  Data0: SRFV0
  — Function: Scrolling adjustment setting in dot units
  — Operation: Scrolls the screen display position up or down in dot units. The amount of the scrolling is 0 to 12 dots.

11. Register 8Chex

	MSB							LSB
	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0
First byte	1	0	0	0	1	1	0	0

→ Register 8Chex identification code

	MSB							LSB
	SCRH1	SCRH0	0	0	0	SRFH2	SRFH1	SRFH0
Second byte	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

- Data7: SCRH1
  Data6: SCRH0
  — Function: Scrolling left/right motion in dot units
  — Operation:

SCRH0	SCRH1	Scroll direction
0	0	Do not scroll
0	1	Scroll right
1	0	Scroll left
1	1	Illegal value

- Data5: Unused (Must be set to 0.)
  Data4: Unused (Must be set to 0.)
  Data3: Unused (Must be set to 0.)
- Data2: SRFH2
  Data1: SRFH1
  Data0: SRFH0
  — Function: Scroll adjustment setting (in dot units)
  — Operation: Scrolls the screen display position to the left or right in dot units. The amount of the scrolling is 0 to 6 dots.

12. Register 0Dhex

	MSB							LSB
	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0
First byte	0	0	0	0	1	1	0	1

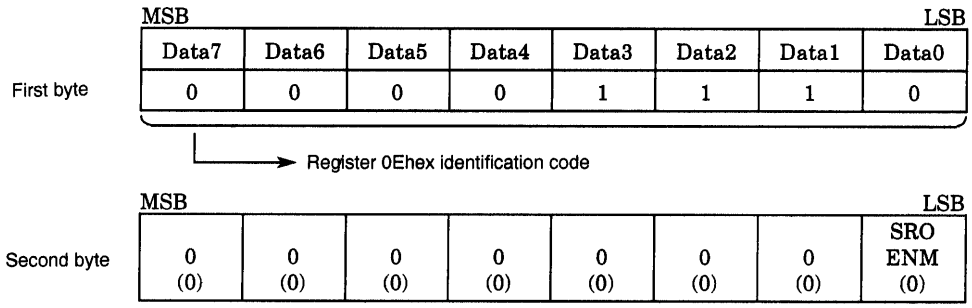
→ Register 0Dhex identification code

	MSB							LSB
	0	0	0	0	0	DCRS	DSPB	DSPA
Second byte	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

- Data7: Unused (Must be set to 0.)
  Data6: Unused (Must be set to 0.)
  Data5: Unused (Must be set to 0.)
  Data4: Unused (Must be set to 0.)
  Data3: Unused (Must be set to 0.)
- Data2: DCRS
  — Function: Cross cursor display control setting
  — Operation: DCRS = 0: Cursor display off
  DCRS = 1: Cursor display on

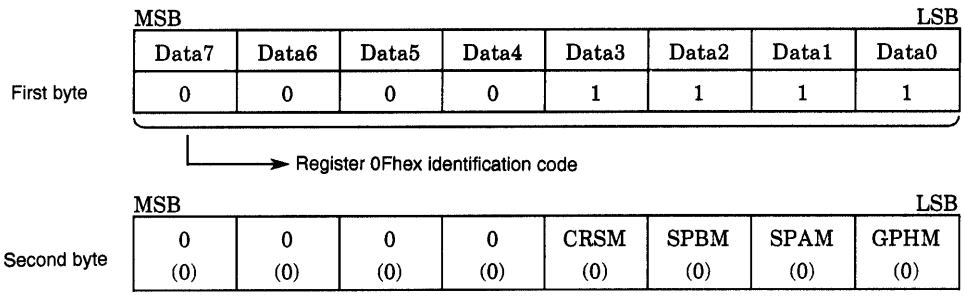
- Data1: DSPB
  — Function: Sprite pattern B display control setting
  — Operation: DSPB = 0: Sprite B display off
  DSPB = 1: Sprite B display on
- Data0: DSPA
  — Function: Sprite pattern A display control setting
  — Operation: DSPA = 0: Sprite A display off
  DSPA = 1: Sprite A display on

13. Register 0Ehex



- Data7: Unused (Must be set to 0.)
  Data6: Unused (Must be set to 0.)
  Data5: Unused (Must be set to 0.)
  Data4: Unused (Must be set to 0.)
  Data3: Unused (Must be set to 0.)
  Data2: Unused (Must be set to 0.)
  Data1: Unused (Must be set to 0.)
- Data0: SROENM
  — Function: Output signal setting for the PSC1 pin (pin 12)
  — Operation: Controls whether or not the serial output data setup complete flag is output from the PCS1 pin.
  SROENM = 0: The flag is not output.
  SROENM = 1: The flag is output.

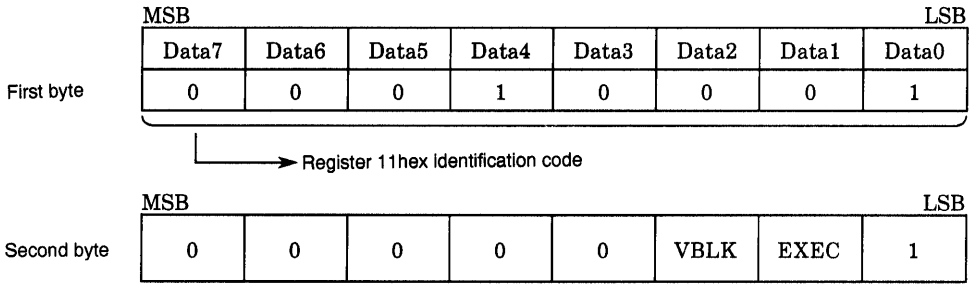
14. Register 0Fhex



- Data7: Unused (Must be set to 0.)
  Data6: Unused (Must be set to 0.)
  Data5: Unused (Must be set to 0.)
  Data4: Unused (Must be set to 0.)
- Data3: CRSM
  — Function: Output signal setting for the PSC2 pin (pin 13)
  — Operation: Controls whether or not the PSC2 pin output monitors the cross cursor display state.
  CRSM = 0: The cursor state is not monitored.
  CRSM = 1: The cross cursor display state is monitored.
  A high level is output when the cross cursor is displayed.

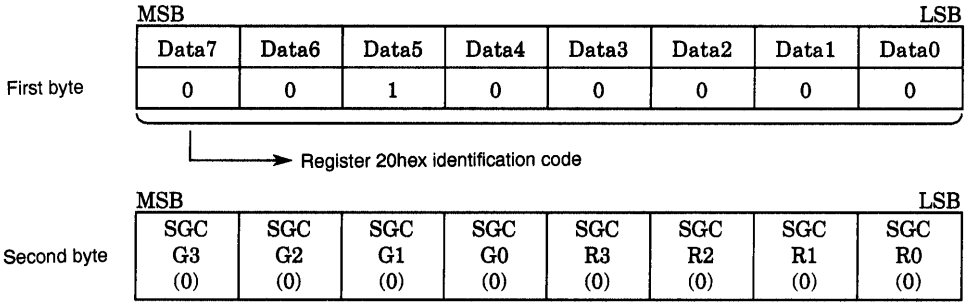
- Data2: SPBM
  — Function: Output signal setting for the PSC2 pin (pin 13)
  — Operation: Controls whether or not the PSC2 pin output monitors the sprite pattern B display state.
  SPBM = 0: The sprite state is not monitored.
  SPBM = 1: The sprite B display state is monitored.
  A high level is output when the sprite B pattern is displayed.
- Data1: SPAM
  — Function: Output signal setting for the PSC2 pin (pin 13)
  — Operation: Controls whether or not the PSC2 pin output monitors the sprite pattern A display state.
  SPAM = 0: The sprite state is not monitored.
  SPAM = 1: The sprite A display state is monitored.
  A high level is output when the sprite A pattern is displayed.
- Data0: GPHM
  — Function: Output signal setting for the PSC2 pin (pin 13)
  — Operation: Controls whether or not the PSC2 pin output monitors the state of the graphics display mode setting.
  GPHM = 0: The display state is not monitored.
  GPHM = 1: The graphics display mode setting state is monitored.
  A high level is output when the LC78711E is operating in graphics display mode.

15. Register 11hex



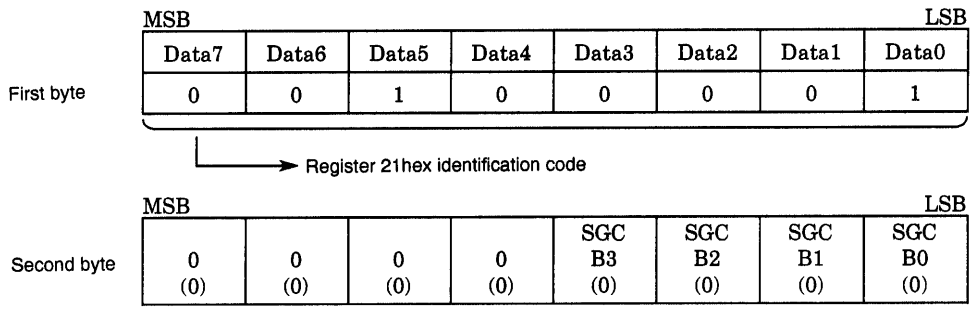
- Data7: 0
  Data6: 0
  Data5: 0
  Data4: 0
  Data3: 0
- Data2: VBLK
  — Function: Vertical blanking (vertical return) period indicator
  — Operation: Outputs a 1 during the vertical blanking period.
  VBLK = 0: Not a vertical blanking period.
  VBLK = 1: Display is in a vertical blanking period.
  NTSC mode: A 19H period
  PAL mode: A 25H period
- Data1: EXEC
  — Function: Command execution state
  — Operation: Outputs the LC78711E command execution state.
  EXEC = 0: Command execution in progress
  EXEC = 1: Command wait state
- Data0: 1

16. Register 20hex



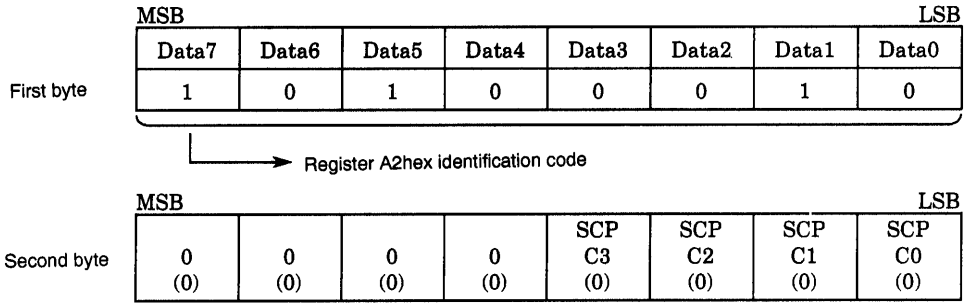
- Data7: SGCG3
  Data6: SGCG2
  Data5: SGCG1
  Data4: SGCG0
  — Function: Drawing color setting (Green level setting for the color palette specified color)
  — Operation: These 4 bits specify the green level. (0hex to Fhex)
- Data3: SGCR3
  Data2: SGCR2
  Data1: SGCR1
  Data0: SGCR0
  — Function: Drawing color setting (Red level setting for the color palette specified color)
  — Operation: These 4 bits specify the red level. (0hex to Fhex)

17. Register 21hex



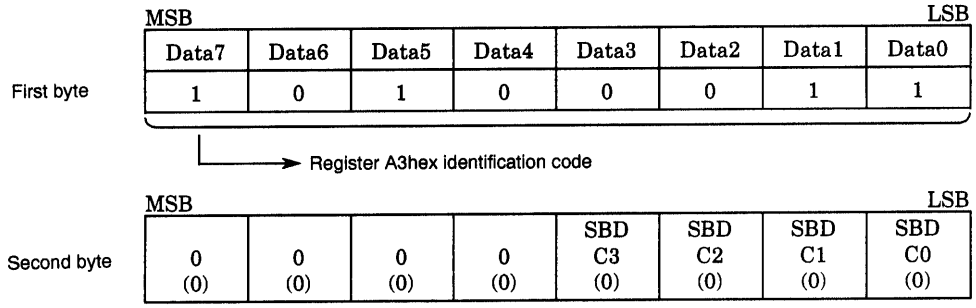
- Data7: Unused (Must be set to 0.)
  Data6: Unused (Must be set to 0.)
  Data5: Unused (Must be set to 0.)
  Data4: Unused (Must be set to 0.)
- Data3: SGCB3
  Data2: SGCB2
  Data1: SGCB1
  Data0: SGCB0
  — Function: Drawing color setting (Blue level setting for the color palette specified color)
  — Operation: These 4 bits specify the blue level. (0hex to Fhex)

18. Register A2hex



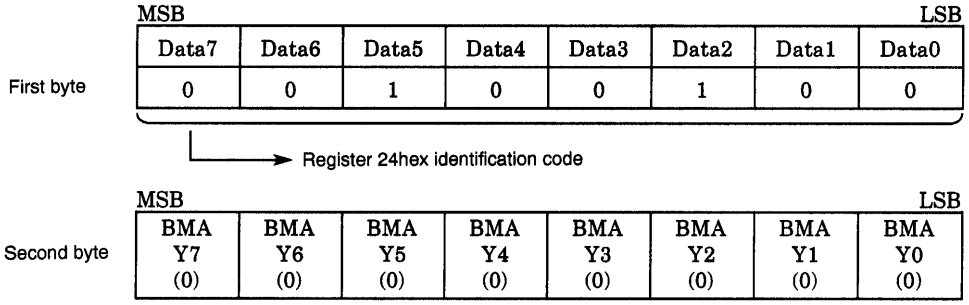
- Data7: Unused (Must be set to 0.)
  Data6: Unused (Must be set to 0.)
  Data5: Unused (Must be set to 0.)
  Data4: Unused (Must be set to 0.)
- Data3: SCPC3
  Data2: SCPC2
  Data1: SCPC1
  Data0: SCPC0
  — Function: Color palette color setting
  — Operation: Sets up the color specified in registers 20 and 21 at the color palette address specified by these 4 bits.

19. Register A3hex



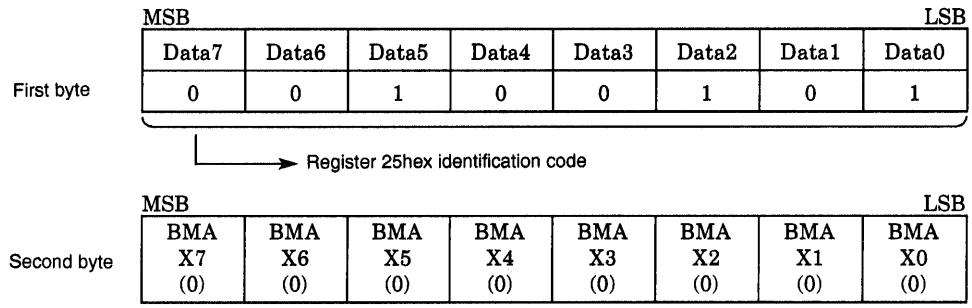
- Data7: Unused (Must be set to 0.)
  Data6: Unused (Must be set to 0.)
  Data5: Unused (Must be set to 0.)
  Data4: Unused (Must be set to 0.)
- Data3: SBDC3
  Data2: SBDC2
  Data1: SBDC1
  Data0: SBDC0
  — Function: Border color specification
  — Operation: Selects the border color from the 16 colors in the color palette.

20. Register 24hex



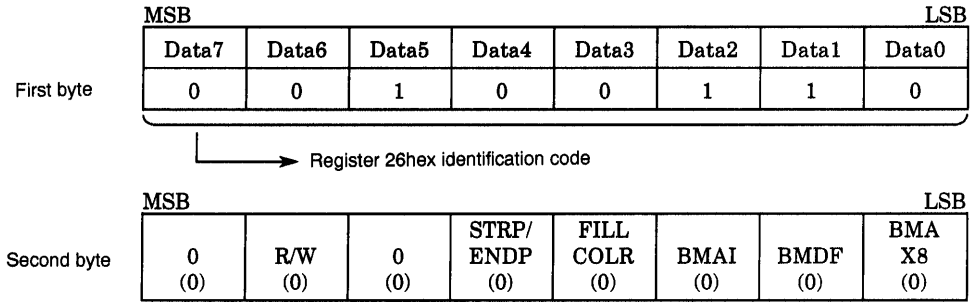
- Data7: BMAY7
  Data6: BMAY6
  Data5: BMAY5
  Data4: BMAY4
  Data3: BMAY3
  Data2: BMAY2
  Data1: BMAY1
  Data0: BMAY0
  — Function: Bit map address specification
  — Operation: Specifies the bit map vertical direction (Y coordinate). The range of valid settings is from 00hex to B7hex (00oct to 215oct). Values of B8hex or larger are illegal.

21. Register 25hex



- Data7: BMAX7
  Data6: BMAX6
  Data5: BMAX5
  Data4: BMAX4
  Data3: BMAX3
  Data2: BMAX2
  Data1: BMAX1
  Data0: BMAX0
  — Function: Bit map address specification
  — Operation: These 8 bits plus the Data0 bit (BMAX8) of register 26hex (for a total of 9 bits), specify the bit map horizontal direction (X coordinate). The range of valid settings is from 000hex to 12Bhex (000oct to 299oct). Values of 12Chex or larger are illegal.

22. Register 26hex

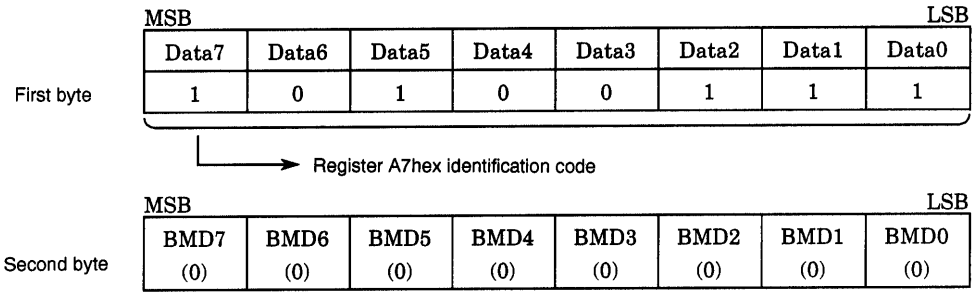


- Data7: Unused (Must be set to 0.)
- Data6: R/W
  - — Function: Bit map data area read/write mode setting
  - — Operation: Sets the bit map data to read or write mode.
    R/W = 0: Bit map data area set to write mode
    R/W = 1: Bit map data area set to read mode
- Data5: Unused (Must be set to 0.)
- Data4: STRP/ENDP
  - — Function: Bit map data setup area start or stop coordinate selection
  - — Operation: Loads the coordinates set up by registers 24hex, 25hex, and the Data0 bit (BMAX8) of this register into the bit map data setup area start or stop address.
    STRP/ENDP = 0: Sets the start coordinates.
    STRP/ENDP = 1: Sets the stop coordinates.
- Data3: FILLCOLR
  - — Function: Bit map area color palette color fill operation setup
  - — Operation: Fills the bit map area specified with STRP/ENDP with the color palette color specified by the 4 bits Data3 to Data0 (BMD3 to BMD0) in register A7hex.
    The execution of the fill operation starts after the color palette is set with register A7hex.
    FILLCOLR = 0: Fill operation not set up.
    FILLCOLR = 1: Sets up a fill operation.
- Data2: BMAI
  - — Function: Automatic bit map address increment during bit map data write setting
  - — Operation: Specifies whether or not the bit map address is automatically incremented during bit map data write operations.
    If automatic incrementing is not specified, the application must specify the address in registers 24hex, 25hex, and 26hex after every data transfer.
    BMAI = 0: The address is not automatically incremented.
    BMAI = 1: The address is automatically incremented.
- Data1: BMDF
  - — Function: Bit map data transfer item count setting
  - — Operation: Specifies whether data is transferred in dot units or in two-dot units during bit map data transfers.
    This is a setting that determines whether only the lower 4 bits or all 8 bits are transferred in register A7hex data transfers.
    BMDF = 0: Takes only the lower 4 bits as data.
    BMDF = 1: Takes all 8 bits as data.
    Here, the lower 4 bits of data are taken as the first data item, and the upper 4 bits are taken as the next data item.

Note: BMDF must be set to 0 when BMAI is set to 0, i.e. when automatic address incrementing is not used.

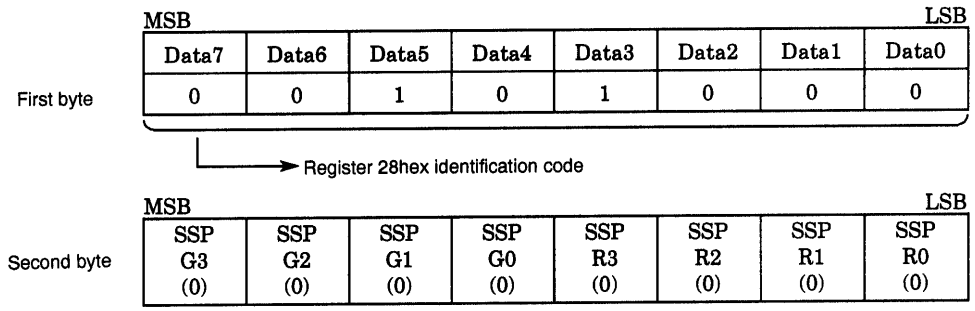
- Data0: BMAX8
  - — Function: Bit map address specification
  - — Operation: This bit plus the Data0 to Data7 bits (BMAX0 to BMAX7) of register 25hex (for a total of 9 bits), specify the bit map horizontal direction (X coordinate). The range of valid settings is from 000hex to 12Bhex (000oct to 299oct). Values of 12Chex or larger are illegal.

23. Register A7hex



- Data7: BMD7
  Data6: BMD6
  Data5: BMD5
  Data4: BMD4
  - — Function: Bit map data setting
  - — Operation: The color palette color specified by these 4 bits is loaded into the specified bit map coordinate, i.e., is written to VRAM.
    This data is valid when BMAI is 1 and BMDF is 1.
- Data3: BMD3
  Data2: BMD2
  Data1: BMD1
  Data0: BMD0
  - — Function: Bit map data setting
  - — Operation: The color palette color specified by these 4 bits is loaded into the specified bit map coordinates, i.e., is written to VRAM.

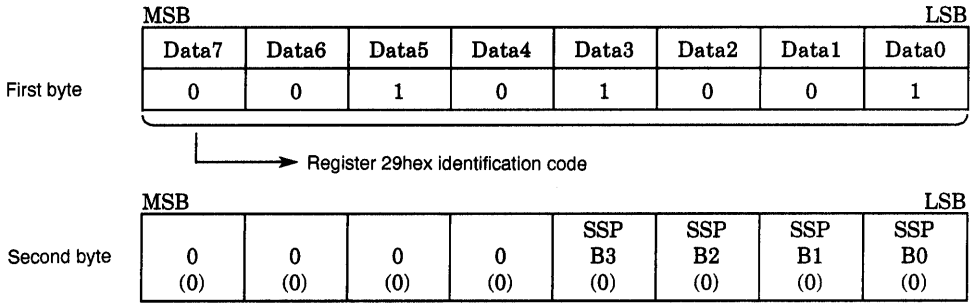
24. Register 28hex



- Data7: SSPG3
  Data6: SSPG2
  Data5: SSPG1
  Data4: SSPG0
  - — Function: Sprite color setting (Sets the green level for the specified color in the sprite color palette.)
  - — Operation: These 4 bits specify the green level. (0hex to Fhex)

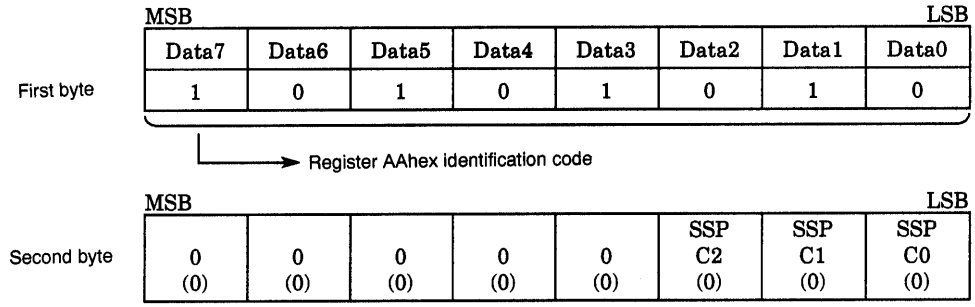
- Data3: SSPR3
  Data2: SSPR2
  Data1: SSPR1
  Data0: SSPR0
  — Function: Sprite color setting (Sets the red level for the specified color in the sprite color palette.)
  — Operation: These 4 bits specify the red level. (0hex to Fhex)

25. Register 29hex



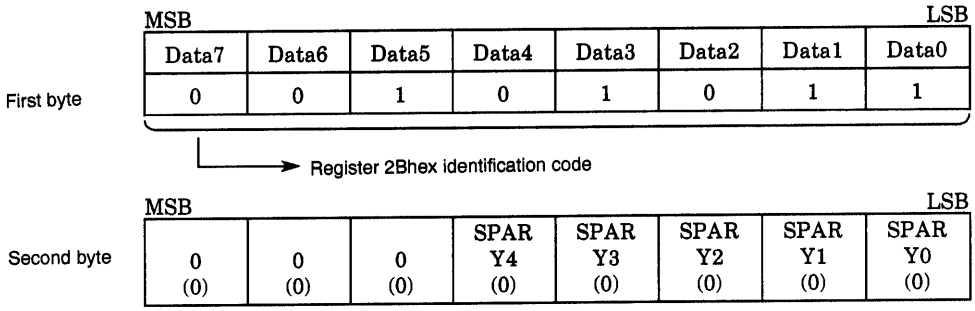
- Data7: Unused (Must be set to 0.)
  Data6: Unused (Must be set to 0.)
  Data5: Unused (Must be set to 0.)
  Data4: Unused (Must be set to 0.)
- Data3: SSPB3
  Data2: SSPB2
  Data1: SSPB1
  Data0: SSPB0
  — Function: Sprite color setting (Sets the blue level for the specified color in the sprite color palette.)
  — Operation: These 4 bits specify the blue level. (0hex to Fhex)

26. Register AAhex



- Data7: Unused (Must be set to 0.)
  Data6: Unused (Must be set to 0.)
  Data5: Unused (Must be set to 0.)
  Data4: Unused (Must be set to 0.)
  Data3: Unused (Must be set to 0.)
- Data2: SSPC2
  Data1: SSPC1
  Data0: SSPC0
  — Function: Sprite color palette color setting
  — Operation: The color specified by registers 28 and 29 is stored at the color palette address specified by these 3 bits.

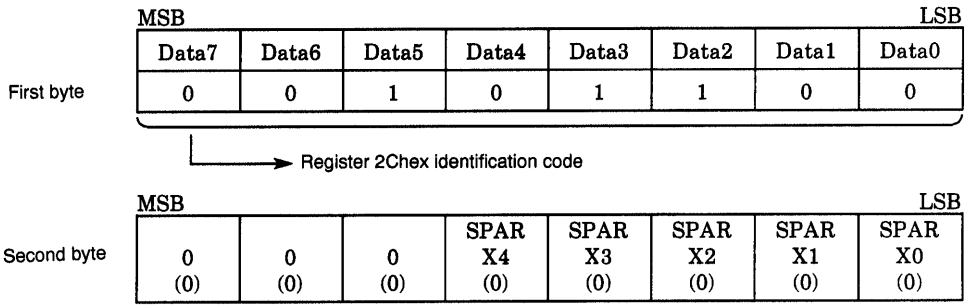
27. Register 2Bhex



	MSB							LSB
	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0
First byte	0	0	1	0	1	0	1	1
	→ Register 2Bhex identification code							
	MSB							LSB
Second byte	0 (0)	0 (0)	0 (0)	SPAR Y4 (0)	SPAR Y3 (0)	SPAR Y2 (0)	SPAR Y1 (0)	SPAR Y0 (0)

- Data7: Unused (Must be set to 0.)
  Data6: Unused (Must be set to 0.)
  Data5: Unused (Must be set to 0.)
- Data4: SPARY4
  Data3: SPARY3
  Data2: SPARY2
  Data1: SPARY1
  Data0: SPARY0
  — Function: Sprite pattern address specification
  — Operation: Specifies the sprite pattern vertical direction (Y coordinate). The range of valid settings is from 00hex to 1Fhex (00oct to 31oct).

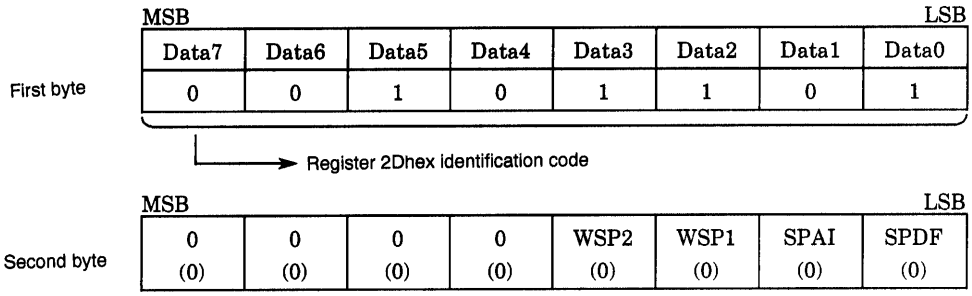
28. Register 2Chex



	MSB							LSB
	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0
First byte	0	0	1	0	1	1	0	0
	→ Register 2Chex identification code							
	MSB							LSB
Second byte	0 (0)	0 (0)	0 (0)	SPAR X4 (0)	SPAR X3 (0)	SPAR X2 (0)	SPAR X1 (0)	SPAR X0 (0)

- Data7: Unused (Must be set to 0.)
  Data6: Unused (Must be set to 0.)
  Data5: Unused (Must be set to 0.)
- Data4: SPARX4
  Data3: SPARX3
  Data2: SPARX2
  Data1: SPARX1
  Data0: SPARX0
  — Function: Sprite pattern address specification
  — Operation: Specifies the sprite pattern horizontal direction (X coordinate). The range of valid settings is from 00hex to 1Fhex (00oct to 31oct).

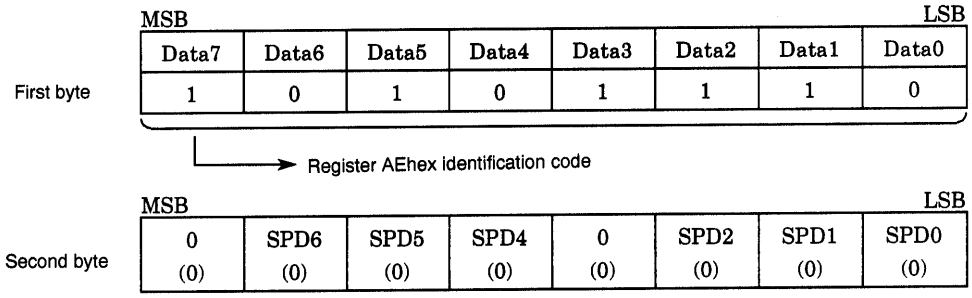
29. Register 2Dhex



- Data7: Unused (Must be set to 0.)
  Data6: Unused (Must be set to 0.)
  Data5: Unused (Must be set to 0.)
  Data4: Unused (Must be set to 0.)
- Data3: WSP2
  — Function: Data write to sprite pattern 2 setup.
  — Operation: Sets up data writes to sprite pattern 2.
  WSP2 = 0: Does not set up data writes to sprite pattern 2.
  WSP2 = 1: Sets up data writes to sprite pattern 2.
- Data2: WSP1
  — Function: Data write to sprite pattern 1 setup
  — Operation: Sets up data writes to sprite pattern 1.
  WSP1 = 0: Does not set up data writes to sprite pattern 1.
  WSP1 = 1: Sets up data writes to sprite pattern 1.
- Data1: SPAI
  — Function: Automatic increment setting for the sprite address during sprite data writes
  — Operation: Specifies whether or not the sprite address is automatically incremented during sprite data writes. If automatic incrementing is not specified, the application must specify the address in registers 2Bhex and 2Chex after every data transfer.
  SPAI = 0: The address is not automatically incremented.
  SPAI = 1: The address is automatically incremented.
- Data0: SPDF
  — Function: Setting for the number of data items transferred during sprite data transfers
  — Operation: Specifies whether data is transferred in dot units or in two dot units during sprite data transfers. This is a setting that determines whether only the lower 3 bits or the lower 3 bits and the upper 3 bits are transferred in register AEhex data transfers.
  SPDF = 0: Takes only the lower 3 bits as data.
  SPDF = 1: Also process the 3 bits Data6 to Data4 as data.
  Here, the lower 3 bits of data are processed as the first data item, and the upper 3 bits become the data for the next bit map address.

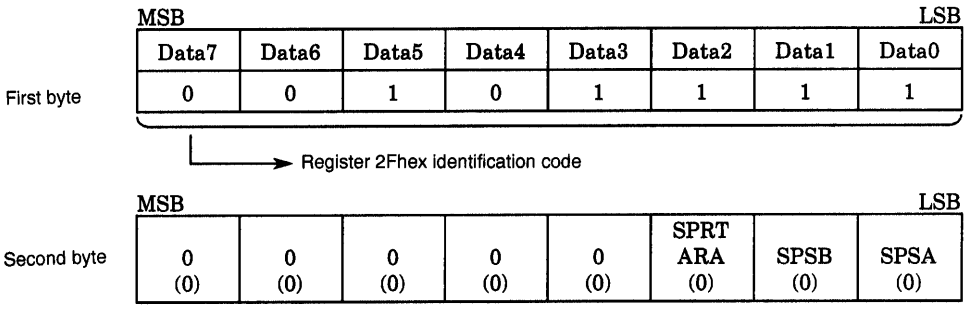
  Note: SPDF must be set to 0 when SPAI is set to 0, i.e. when automatic address incrementing is not used.

30. Register AEhex



- Data7: Unused (Must be set to 0.)
- Data6: SPD6
  Data5: SPD5
  Data4: SPD4
  — Function: Bit map data settings
  — Operation: The color palette color specified by these 3 bits is loaded at the specified sprite coordinate. This data is valid when SPAI is 1 and SPDF is 1.
- Data3: Unused (Must be set to 0.)
- Data2: SPD2
  Data1: SPD1
  Data0: SPD0
  — Function: Bit map data settings
  — Operation: The color palette color specified by these 3 bits is loaded at the specified sprite coordinate.

31. Register 2Fhex



- Data7: Unused (Must be set to 0.)
  Data6: Unused (Must be set to 0.)
  Data5: Unused (Must be set to 0.)
  Data4: Unused (Must be set to 0.)
  Data3: Unused (Must be set to 0.)
- Data2: SPRTARA
  — Function: Sprite pattern display area setting
  — Operation: Sets whether the sprite pattern display area is limited to the drawing area or is set to the whole image area, i.e., the sprite pattern can also be displayed outside the drawing area.
  SPRTARA = 0: Display only in the drawing area.
  SPRTARA = 1: Display outside the drawing area also allowed.
- Data1: SPSB
  — Function: Selection of sprite pattern 1 or 2 as the sprite B display pattern
  — Operation: Selects whether sprite pattern 1 or 2 is displayed as the sprite B display pattern. This is selection of the pattern whose display is turned on by the Data1 (DSPB) bit in register 0Dhex.
  SPSB = 0: Sprite pattern 1 is displayed.
  SPSB = 1: Sprite pattern 2 is displayed.

- Data0: SPSA
  — Function: Selection of sprite pattern 1 or 2 as the sprite A display pattern
  — Operation: Selects whether sprite pattern 1 or 2 is displayed as the sprite A display pattern. This is selection of the pattern whose display is turned on by the Data0 (DSPA) bit in register 0Dhex.
  SPSA = 0: Sprite pattern 1 is displayed.
  SPSA = 1: Sprite pattern 2 is displayed.

Note: When the same pattern is selected for both sprites A and B, two instances of the same pattern are displayed.

32. Register 30hex

	MSB							LSB
	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0
First byte	0	0	1	1	0	0	0	0

Register 30hex identification code

	MSB							LSB
Second byte	SPD AY7 (0)	SPD AY6 (0)	SPD AY5 (0)	SPD AY4 (0)	SPD AY3 (0)	SPD AY2 (0)	SPD AY1 (0)	SPD AY0 (0)

- Data7: SPDAY7
  Data6: SPDAY6
  Data5: SPDAY5
  Data4: SPDAY4
  Data3: SPDAY3
  Data2: SPDAY2
  Data1: SPDAY1
  Data0: SPDAY0
  — Function: Sprite display address setting
  — Operation: Specifies the sprite display vertical direction (Y coordinate). The range of valid settings is from 00hex to B7hex (00oct to 215oct). Values of B8hex or larger are illegal.

33. Register 31hex

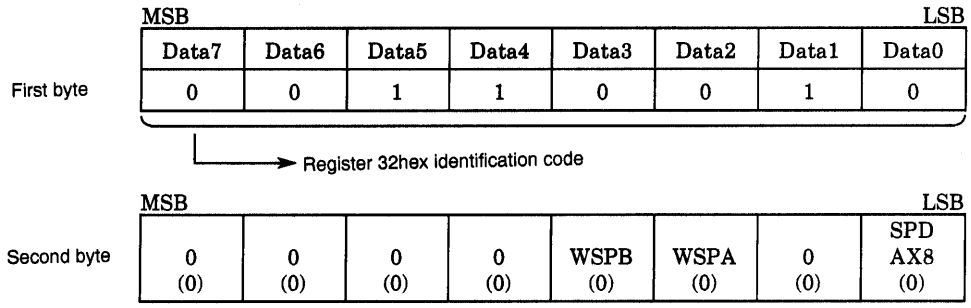
	MSB							LSB
	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0
First byte	0	0	1	1	0	0	0	1

Register 31hex identification code

	MSB							LSB
Second byte	SPD AX7 (0)	SPD AX6 (0)	SPD AX5 (0)	SPD AX4 (0)	SPD AX3 (0)	SPD AX2 (0)	SPD AX1 (0)	SPD AX0 (0)

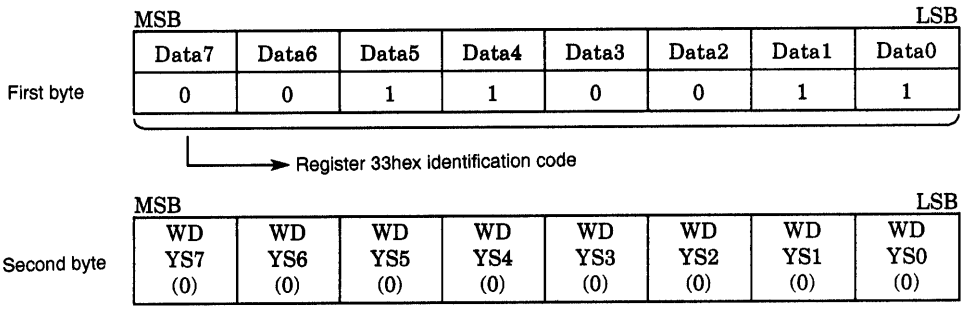
- Data7: SPDAX7
  Data6: SPDAX6
  Data5: SPDAX5
  Data4: SPDAX4
  Data3: SPDAX3
  Data2: SPDAX2
  Data1: SPDAX1
  Data0: SPDAX0
  — Function: Sprite display address setting
  — Operation: These 8 bits plus the Data0 bit (SPDAX8) of register 32hex (for a total of 9 bits), specify the sprite display horizontal direction (X coordinate). The range of valid settings is from 000hex to 12Bhex (000oct to 299oct). Values of 12Chex or larger are illegal.

34. Register 32hex



- Data7: Unused (Must be set to 0.)
  Data6: Unused (Must be set to 0.)
  Data5: Unused (Must be set to 0.)
  Data4: Unused (Must be set to 0.)
- Data3: WSPB
  — Function: Sprite B display start address write control
  — Operation: Sets the address specified as the sprite display address as the sprite B display start address.
  WSPB = 0: No setting performed.
  WSPB = 1: Sets the address.
- Data2: WSPA
  — Function: Sprite A display start address write control
  — Operation: Sets the address specified as the sprite display address as the sprite A display start address.
  WSPA = 0: No setting performed.
  WSPA = 1: Sets the address.
- Data1: Unused (Must be set to 0.)
- Data0: SPDAX8
  — Function: Sprite address specification
  — Operation: The Data0 to Data7 bits (SPDAX0 to SPDAX7) in register 31 and this bit of this register (for a total of 9 bits) specify the sprite horizontal direction (X coordinate). The range of valid settings is from 000hex to 12Bhex (000oct to 299oct). Values of 12Chex or larger are illegal.

35. Register 33hex



- Data7: WDYS7
  Data6: WDYS6
  Data5: WDYS5
  Data4: WDYS4
  Data3: WDYS3
  Data2: WDYS2
  Data1: WDYS1
  Data0: WDYS0
  — Function: Display window address specification
  — Operation: Specifies the display window vertical direction (Y coordinate). The range of valid settings is from 00hex to B7hex (00oct to 215oct). Values of B8hex or larger are illegal.

36. Register 34hex

	MSB							LSB
	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0
First byte	0	0	1	1	0	1	0	0

→ Register 34hex identification code

	MSB							LSB
Second byte	WD XS7 (0)	WD XS6 (0)	WD XS5 (0)	WD XS4 (0)	WD XS3 (0)	WD XS2 (0)	WD XS1 (0)	WD XS0 (0)

- Data7: WDXS7
  Data6: WDXS6
  Data5: WDXS5
  Data4: WDXS4
  Data3: WDXS3
  Data2: WDXS2
  Data1: WDXS1
  Data0: WDXS0
  — Function: Sprite display address specification
  — Operation: These 8 bits plus the Data0 bit (WDXS8) of register 35hex (for a total of 9 bits), specify the bit map horizontal direction (X coordinate). The range of valid settings is from 000hex to 12Bhex (000oct to 299oct). Values of 12Chex or larger are illegal.

37. Register 35hex

	MSB							LSB
	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0
First byte	0	0	1	1	0	1	0	1

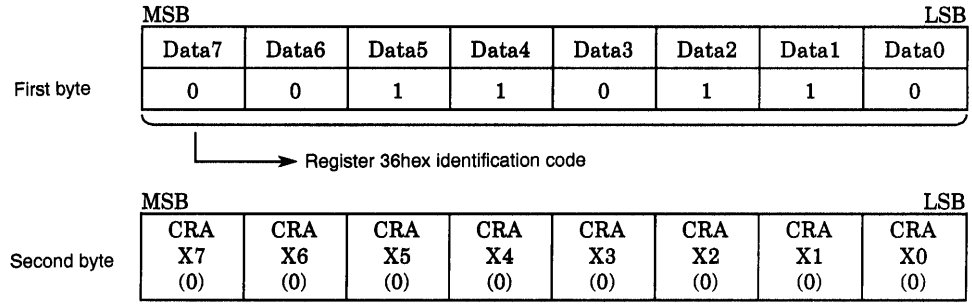
→ Register 35hex identification code

	MSB							LSB
Second byte	0 (0)	0 (0)	WD EN (0)	WD AR (0)	PAL 60 (0)	SADR/ EADR (0)	0 (0)	WD XS8 (0)

- Data7: Unused (Must be set to 0.)
  Data6: Unused (Must be set to 0.)
- Data5: WDEN
  — Function: Display window display setting
  — Operation: Sets display window display.
  WDEN = 0: The display window is not displayed.
  WDEN = 1: The display window is displayed.
- Data4: WDAR
  — Function: Display window display area setting
  — Operation: Sets the display window display area.
  WDAR = 0: Displays the inside of the display window
  WDAR = 1: Displays the outside of the display window
- Data3: PAL60
  — Function: PAL60 mode setting (Valid only when N/P1 and N/P2 are 0.)
  — Operation: PAL60 = 0: PAL mode
  PAL60 = 1: PAL60 mode

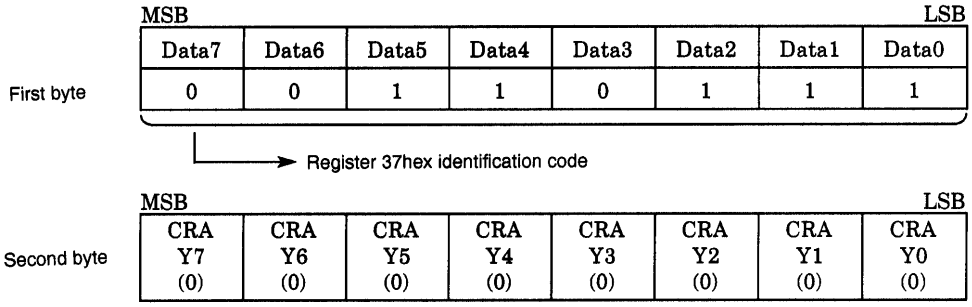
- Data2: SADR/EADR
  — Function: Display window display coordinates setting
  — Operation: Sets the display window display area.
  SADR/EADR = 0: Sets the display window start address.
  SADR/EADR = 1: Sets the display window end address.
- Data1: Unused (Must be set to 0.)
- Data0: WDXS8
  — Function: Display window address setting
  — Operation: The Data0 to Data7 bits (WDXS0 to WDXS7) in register 34 and this bit of this register (for a total of 9 bits) specify the sprite horizontal direction (X coordinate). The range of valid settings is from 000hex to 12Bhex (000oct to 299oct). Values of 12Chex or larger are illegal.

38. Register 36hex



- Data7: CRAX7
  Data6: CRAX6
  Data5: CRAX5
  Data4: CRAX4
  Data3: CRAX3
  Data2: CRAX2
  Data1: CRAX1
  Data0: CRAX0
  — Function: Cross cursor position setting
  — Operation: Specifies the horizontal direction (X coordinate) for the cross cursor intersection point. This setting sets the position in 2-dot units.

39. Register 37hex



- Data7: CRAY7
  Data6: CRAY6
  Data5: CRAY5
  Data4: CRAY4
  Data3: CRAY3
  Data2: CRAY2
  Data1: CRAY1
  Data0: CRAY0
  — Function: Cross cursor position setting
  — Operation: Specifies the vertical direction (Y coordinate) for the cross cursor intersection point. This setting sets the position in 2-dot units.

  Note: The register 0Dhex Data 3 bit (DCRS) setting is required for execution of the cross cursor display function.

NTSC Sample Application Circuit