Ordering number : EN5348

CMOS LSI

LC75371M

Car Stereo Electronic Tone and Volume Control

Overview

The LC75371M is an electronic tone/volume control LSI that can implement, with minimal external components, volume, balance, fader, bass and treble, loudness, input switching, and input level controls.

Functions

- Volume control: From 0 to –79 dB in 1-dB steps plus –∞ for a total of 81 settings. Since the left and right levels can be set independently, this function can also be used to implement a balance function.
- Fader: Attenuates either the rear or front channels to one of 16 levels. (Provides 16 settings, namely, from 0 to –20 dB in 2-dB steps, from –20 to –25 dB in one 5-dB step, from –25 to –45 dB in 10-dB steps, –60 dB, and –∞.)
- Bass and treble controls: Forms an NF-type tone control circuit (LUX type) using external capacitors. Provides 15 settings each for the bass and treble controls.
- Loudness control: A loudness function can be implemented by attaching external RC circuits at the taps provided from the volume control resistor ladder starting at the –20-dB position.
- The input signal can be selected from one of three inputs for each of the left and right channels. The input signal can be amplified by between 0 and +18 dB in 6-dB steps.
- Serial data input: Supports CCB* format communication with the system controller.

Features

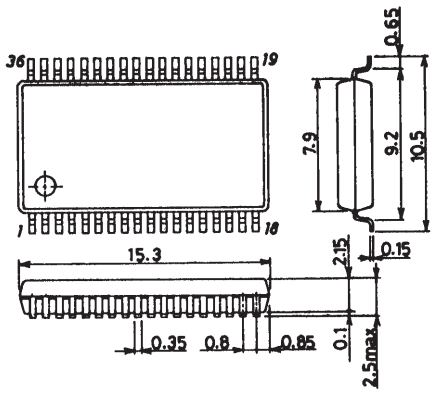
- Built-in buffer amplifiers allow applications to be implemented with few external components.
- A $V_{DD}/2$ reference voltage generation circuit is provided on chip.

Package Dimensions

unit: mm

3204-MFP36S

[LC75371M]



SANYO: MFP36S

- **CCB is a trademark of SANYO ELECTRIC CO., LTD.**
- **CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.**

SANYO Electric Co.,Ltd. Semiconductor Bussiness Headquarters

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	12	V
Maximum input voltage	V_{IN} max	CL, DI, CE, LIN, RIN, LFIN, RFIN, L1 to L3, R1 to R3	V_{SS} – 0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max	Ta ≤ 85°C	230	mW
Operating temperature	Topr		–40 to +85	°C
Storage temperature	Tstg		–50 to +125	°C

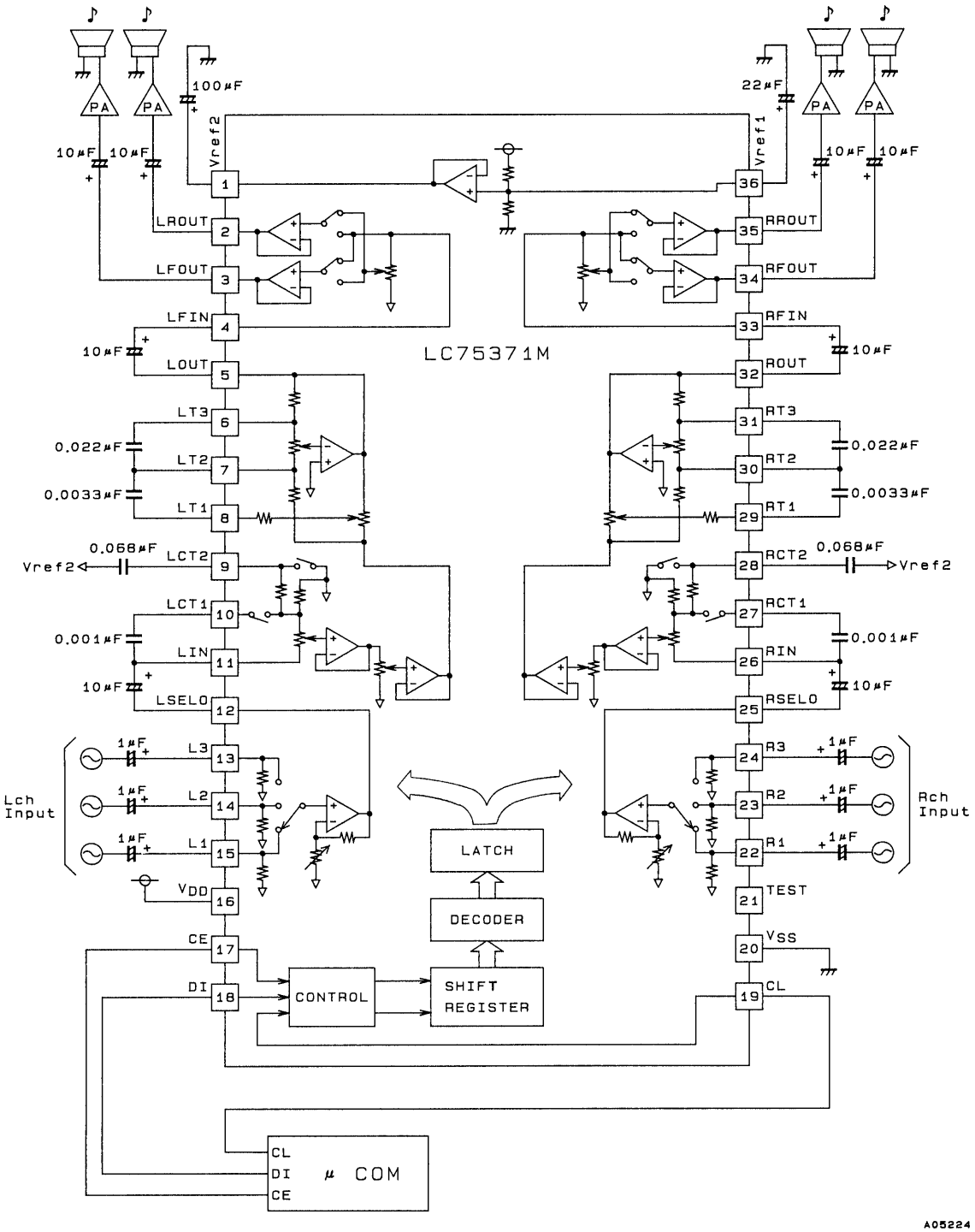
Allowable Operating Ranges at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}	V_{DD}	6.0		11.0	V
Input high-level voltage	V_{IH}	CL, DI, CE	4.0		V_{DD}	V
Input low-level voltage	V_{IL}	CL, DI, CE	V_{SS}		1.0	V
Input voltage amplitude	V_{IN}	CL, DI, CE, LIN, RIN, LFIN, RFIN, L1 to L3, R1 to R3	V_{SS}		V_{DD}	Vp-p
Input pulse width	$t_{øW}$	CL	1			µs
Setup time	tsetup	CL, DI, CE	1			µs
Hold time	thold	CL, DI, CE	1			µs
Operating frequency	fopg	CL			500	kHz

Electrical Characteristics at Ta = 25°C, V_{DD} = 9 V, V_{SS} = 0 V

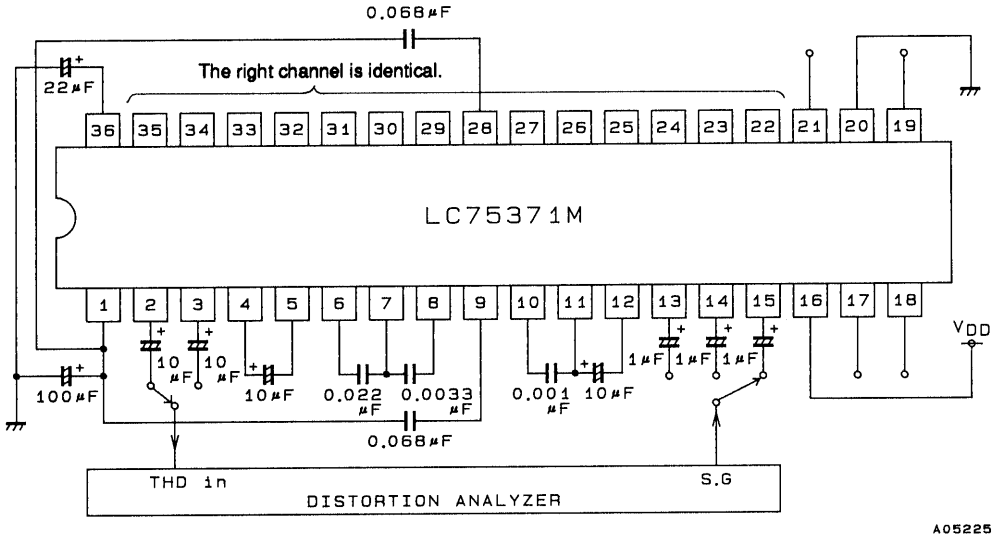
Parameter	Symbol	Conditions	min	typ	max	Unit
[Input Block]						
Input resistance	Rin	L1 to L3, R1 to R3	30	50	70	kΩ
Minimum input gain	Gin min		–2	0	+2	dB
Maximum input gain	Gin max		+16.0	+18.0	+20.0	dB
Step resolution	Gstep			+6.0		dB
[Volume Control Block]						
Input resistance	Rv10	LIN, RIN: 10-dB steps, loudness off	30	50	70	kΩ
	Rv1	1-dB steps	6	10	14	kΩ
Step resolution	ATstep			1		dB
Step error	ATerr	step = 0 to –20 dB	–1	0	+1	dB
		step = –20 to –50 dB	–3	0	+3	dB
[Fader Block]						
Input resistance	Rfed	LFIN, RFIN	12	20	28	kΩ
Step resolution	ATstep	step = 0 to –20 dB		2		dB
		step = –20 to –25 dB		5		dB
		step = –25 to –45 dB		10		dB
Step error	ATerr	step = 0 to –45 dB	–2	0	+2	dB
		step = –45 dB	–3	0	+3	dB
Output load resistance	R_L	LFOUT, LROUT, RFOUT, RROUT	20			kΩ
[Bass and Treble Control Block]						
Bass control range	Gbass	Max. boost/cut	±9	±10.5	±12	dB
Treble control range	Gtre	Max. boost/cut	±8	±10.5	±13	dB
[Overall Characteristics]						
Total harmonic distortion	THD1	V_{IN} = 1 Vrms, f = 1 kHz, all settings flat overall		0.045		%
	THD2	V_{IN} = 1 Vrms, f = 20 kHz, all settings flat overall		0.045		%
Crosstalk	CT	V_{IN} = 1 Vrms, f = 1 kHz, all settings flat overall, Rg = 1 kΩ		70		dB
Output at maximum attenuation	V_O min	V_{IN} = 1 Vrms, f = 1 kHz, main volume control at –∞		–76		dB
		V_{IN} = 1 Vrms, f = 1 kHz, main volume control at –∞, INMUTE		–80		dB
Output noise voltage	V_N1	All settings flat overall (IHF-A), Rg = 1 kΩ		12	30	μV
	V_N2	All settings flat overall (DIN-AUDIO), Rg = 1 kΩ		16	40	μV
Current drain	I_{DD}	V_{DD} – V_{SS} = 11 V		19	22.8	mA
Input high-level current	I_{IH}	CL, DI, CE: V_{IN} = 9 V			10	μA
Input low-level current	I_{IL}	CL, DI, CE: V_{IN} = 0 V	–10			μA
Maximum input level	V_{CL}	THD = 1%, R_L = 20 kΩ, all tsettings flat overall, test point = fader output.		2		Vrms

Equivalent Circuit Block Diagram and Sample Application Circuit

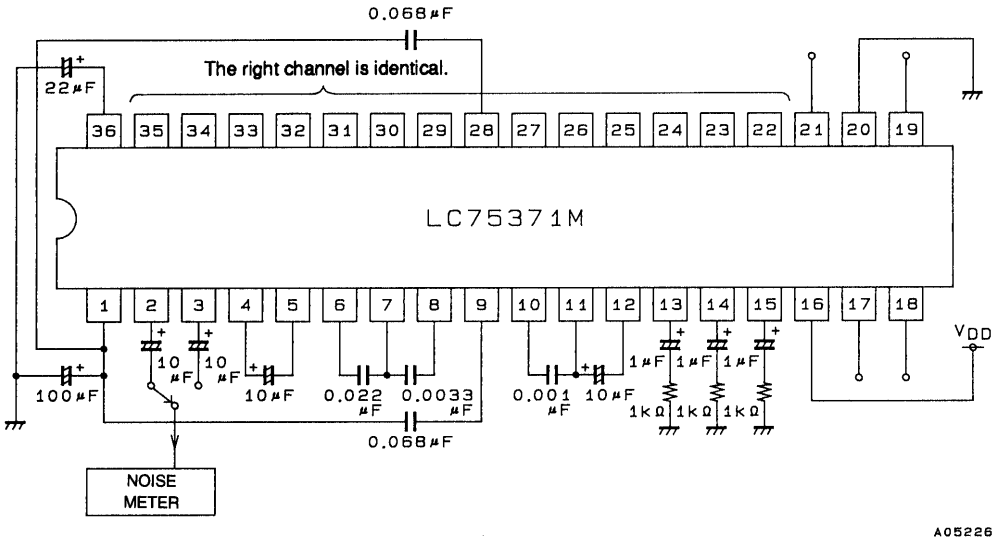


Test Circuits

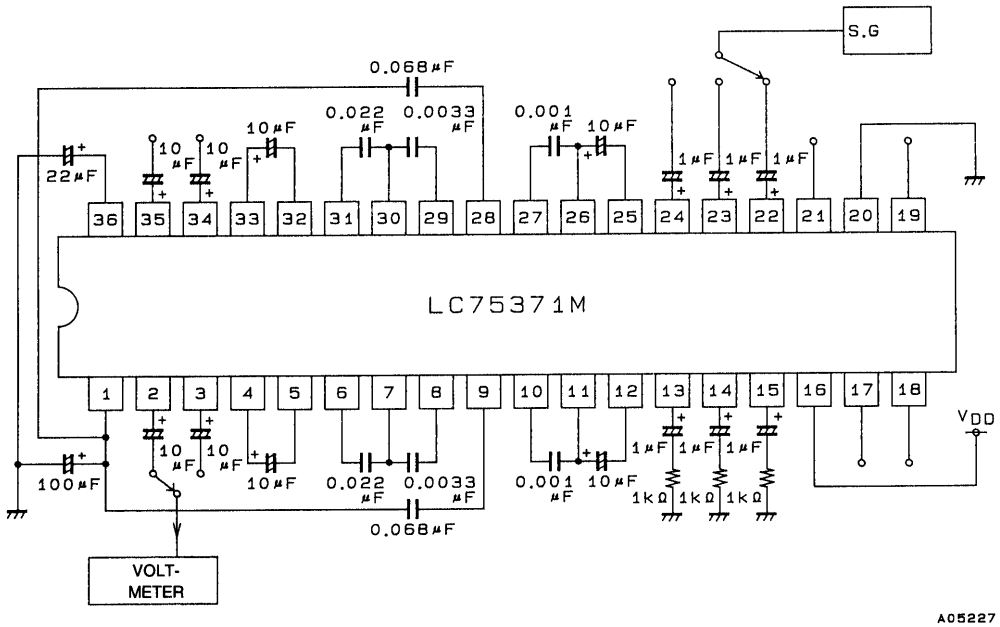
1. Total harmonic distortion



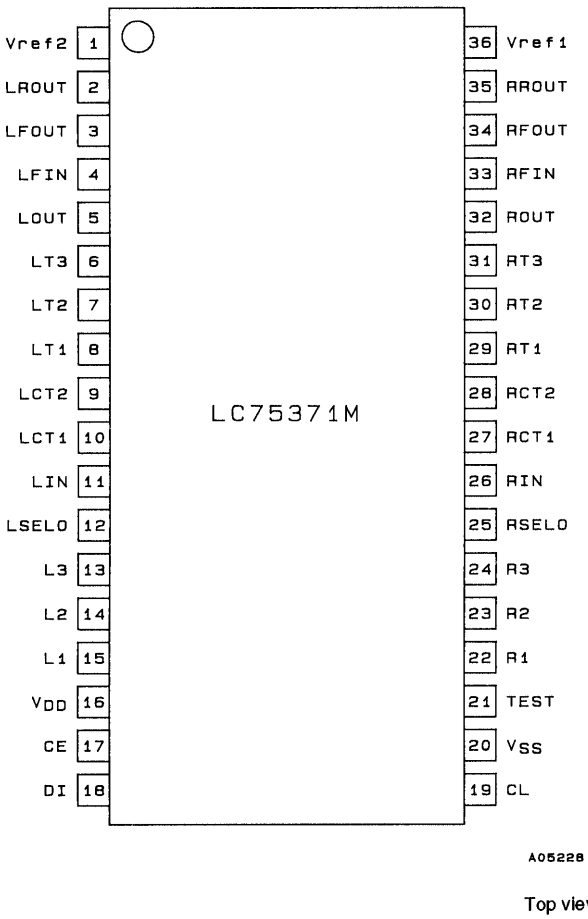
2. Output noise voltage



3. Crosstalk

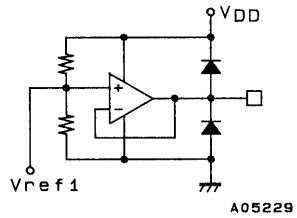
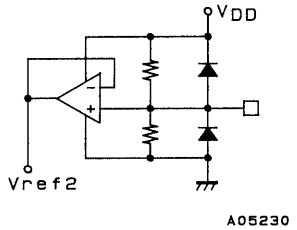
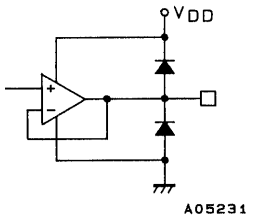
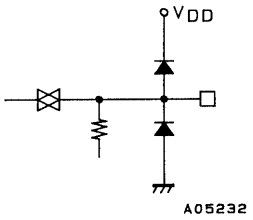
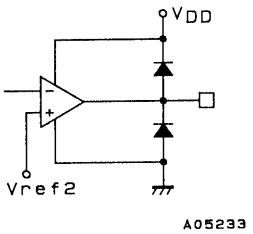
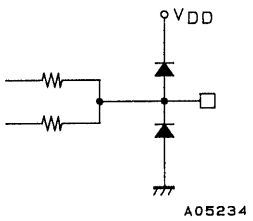


Pin Assignment



Top view

Pin Functions

Pin No.	Symbol	Function	Notes
1	Vref2	• Common pin for the main volume control block, fader block, tone control block, gain control block, and input switching block. • Since the capacitor connected between Vref2 and V_{SS} becomes the residual resistance when the volume control is set to maximum attenuation, the value of this capacitor must be selected carefully. • The voltage applied to this pin must never exceed V_{DD}.	
36	Vref1	V_{DD}/2 voltage generation block. A capacitor must be connected between Vref1 and V_{SS} to suppress power supply ripple.	
2 3 35 34	LROUT LFOUT RROUT RFOUT	• Fader outputs. The front and rear can be attenuated independently. The left and right attenuation levels are identical. • These are low-impedance outputs, since they have built-in operational amplifiers.	
4 33	LFIN RFIN	• Fader inputs • These inputs must be driven by low-impedance outputs.	
5 32	LOUT ROUT	Tone control outputs	
8 7 6 29 30 31	LT1 LT2 LT3 RT1 RT2 RT3	Connections for the bass and treble supplementary capacitors for the tone control circuit Connect high-frequency compensation capacitors between the T1/T2 pairs. Connect low-frequency compensation capacitors between the T2/T3 pairs.	
10 9 27 28	LCT1 LCT2 RCT1 RCT2	Loudness circuit connections. Connect high-frequency compensation capacitors between the LCT1/RCT1 and LIN/RIN pins, and connect low-frequency compensation capacitors between LCT2/RCT2 and Vref2.	

Continued on next page.

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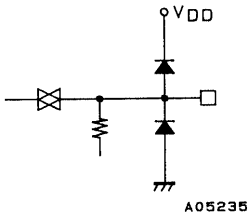
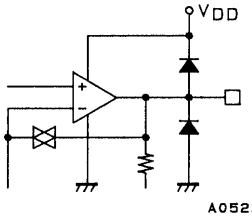
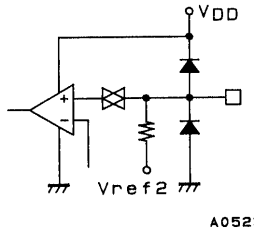
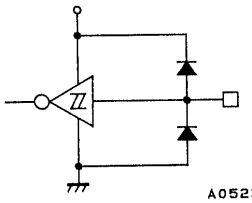
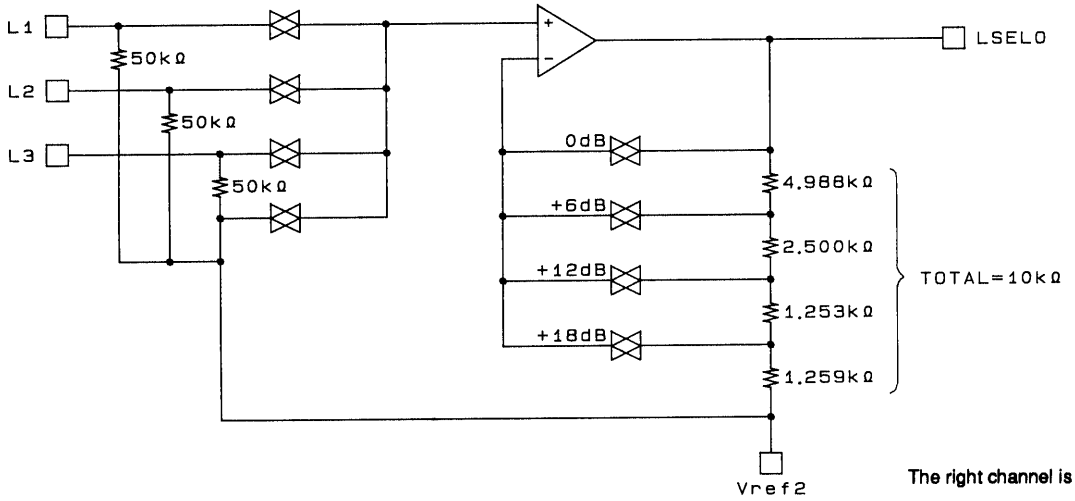
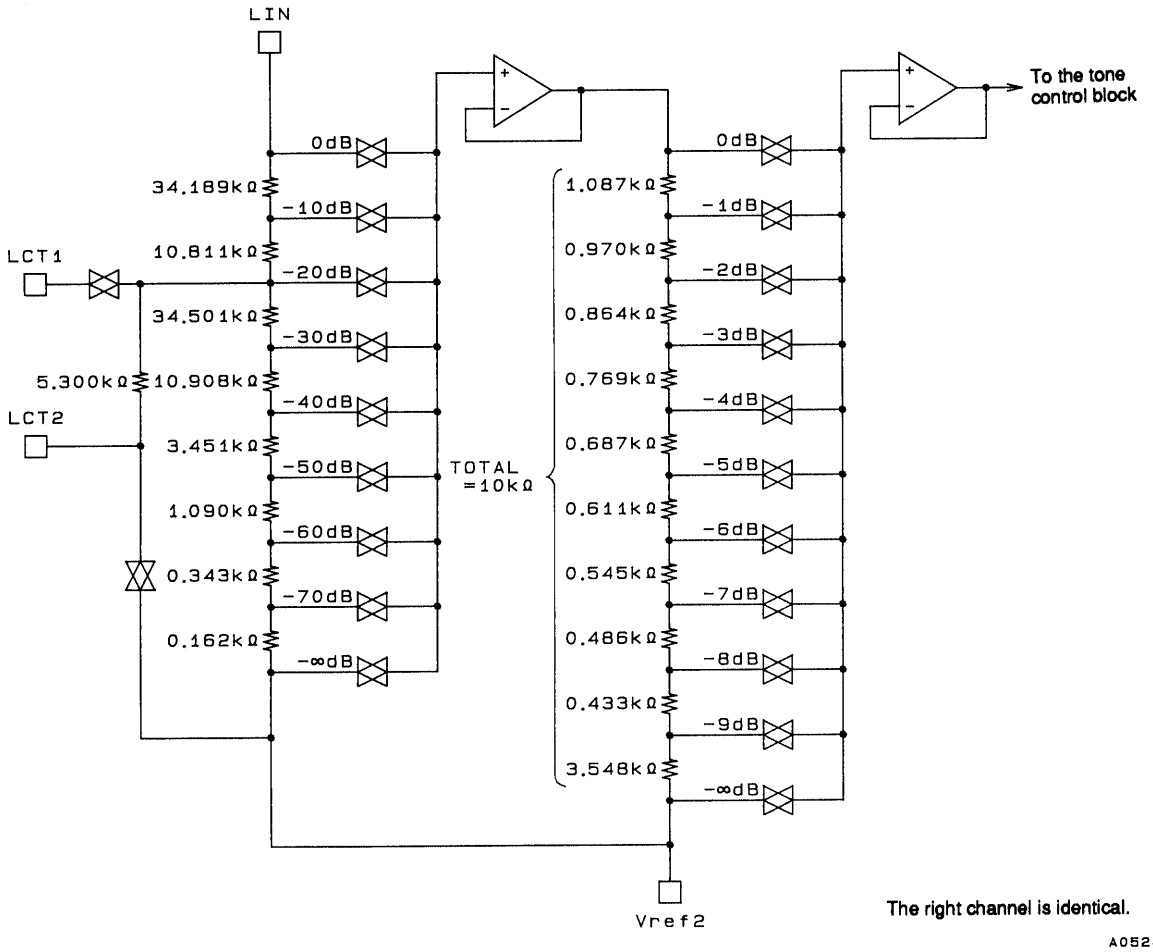
Pin No.	Symbol	Function	Notes
11 26	LIN RIN	• Main volume control inputs • These inputs must be driven by low-impedance outputs.	
12 25	LSELO RSELO	Input selector outputs	
15 14 13 22 23 24	L1 L2 L3 R1 R2 R3	Signal inputs	
16	V_{DD}	Power supply	
20	V_{SS}	Ground	
17	CE	Chip enable. Data is loaded into the internal latch when this pin goes from high to low, and all analog switches operate at that time. Data transfers are enabled when this pin is high.	
18 19	DI CL	Serial data and clock inputs for LSI control.	
21	TEST	Test pin. This pin must be left open.	

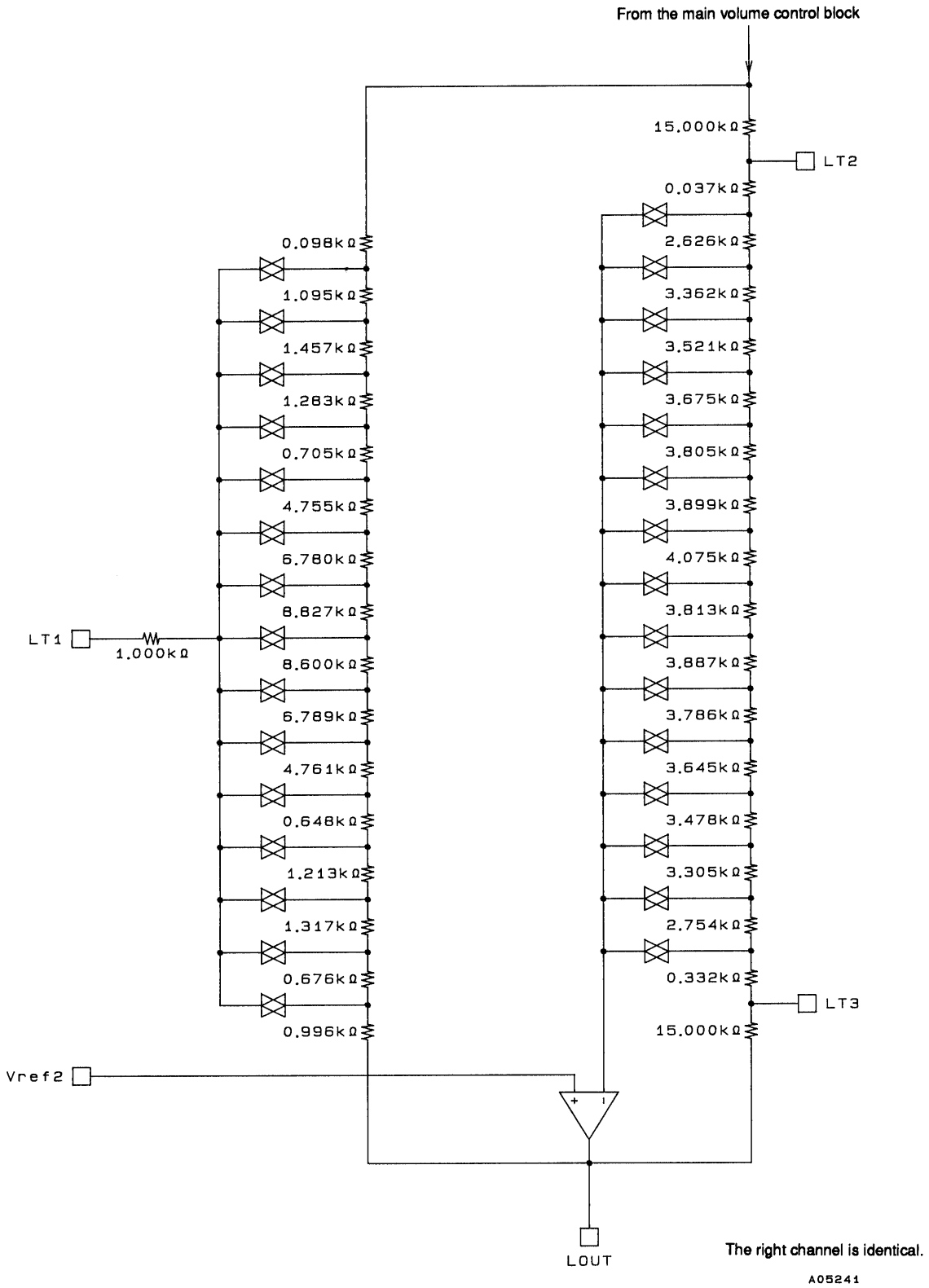
Input Block Equivalent Circuit Diagram



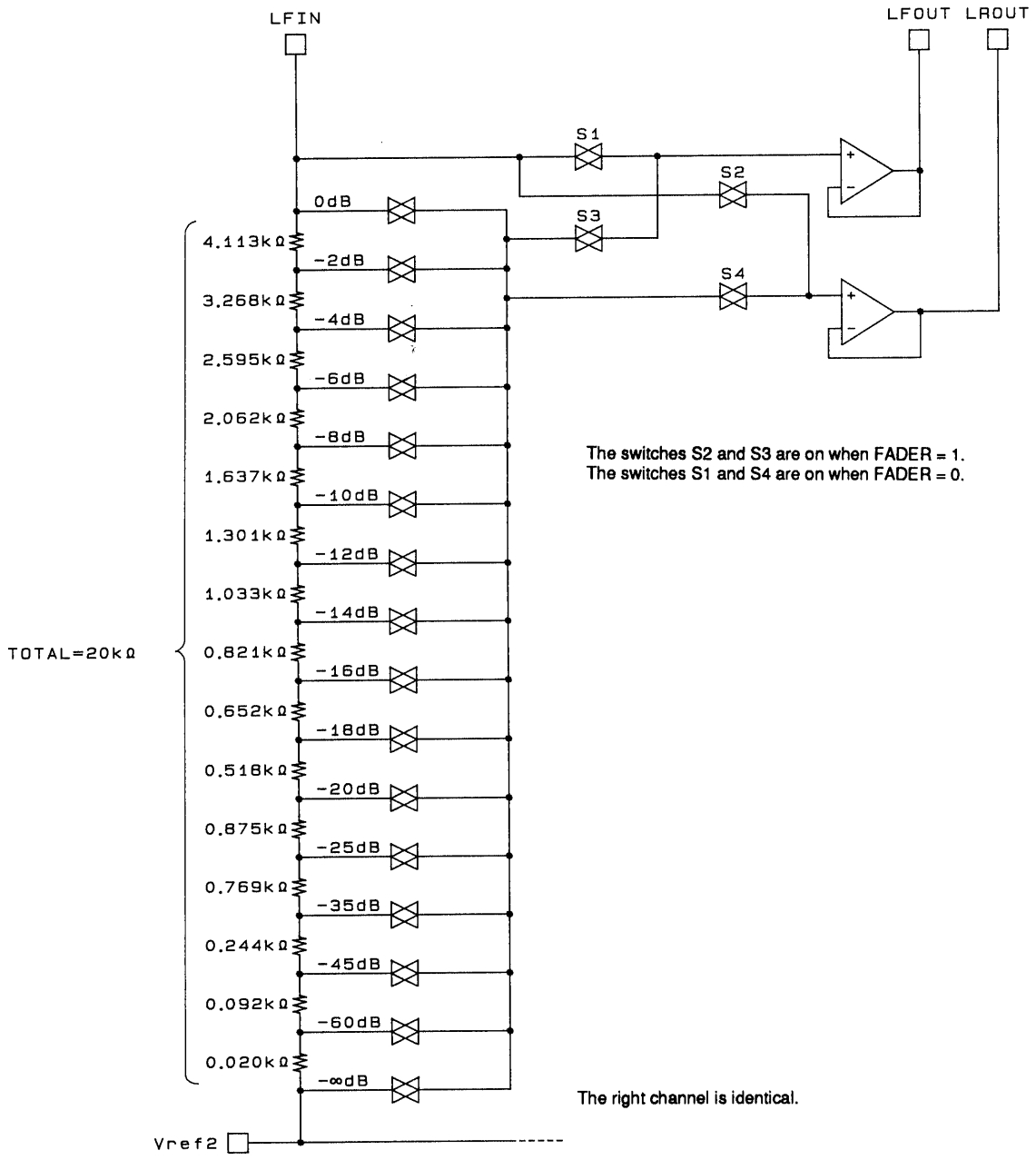
Main Volume Control Block Equivalent Circuit Diagram



Tone Control Block Equivalent Circuit Diagram



Fader Block Equivalent Circuit Diagram



If data setting the main volume control 1-dB step to –∞ is sent to the LSI, the S1 and S2 switches will be opened and the S3 and S4 switches will be turned on (closed).

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Sample Calculation of the Loudness Circuit External Constants

First, see the LC75371M 10-dB step internal equivalent circuit shown on page 9. Figure 1 below shows a version of that circuit to which the loudness circuit external components have been added, and which has been simplified for this calculation. The sample calculation below uses this circuit diagram to acquire a 5-dB boost at f = 100 Hz.

(f = 100 Hz, 5-dB boost)

Assuming that the resistors and capacitors in Figure 1 have the following values:

R1 = R2 = 50 kΩ

R3 = 5 kΩ

And C1 = Z1 and C2 = Z2.

Then:

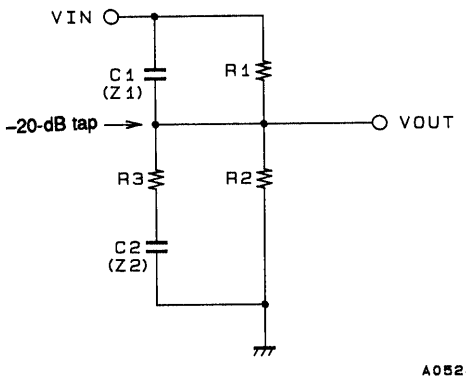
$$V_{OUT} \text{ (at = 1 kHz)} = \frac{\dfrac{R2\,(R3 + Z2)}{R2 + R3 + Z2}}{\dfrac{R1 \cdot Z1}{R1 + Z1} + \dfrac{R2\,(R3 + Z2)}{R2 + R3 + Z2}} = -20 \text{ dB}$$

$$V_{OUT} \text{ (at = 100 Hz)} = \frac{\dfrac{R2\,(R3 + 10 \cdot Z2)}{R2 + R3 + 10 \cdot Z2}}{\dfrac{R1 \cdot 10 \cdot Z1}{R1 + 10 \cdot Z1} + \dfrac{R2\,(R3 + 10 \cdot Z2)}{R2 + R3 + 10 \cdot Z2}} = -15 \text{ dB}$$

From the above equations we find:

Z1 = 891.5 kΩ and Z2 = 880 Ω.

Therefore, the specifications will be met if capacitors that have these impedances at f = 1 kHz are connected externally. The result is that C1 = 178.5 pF and C2 = 0.18 μF.

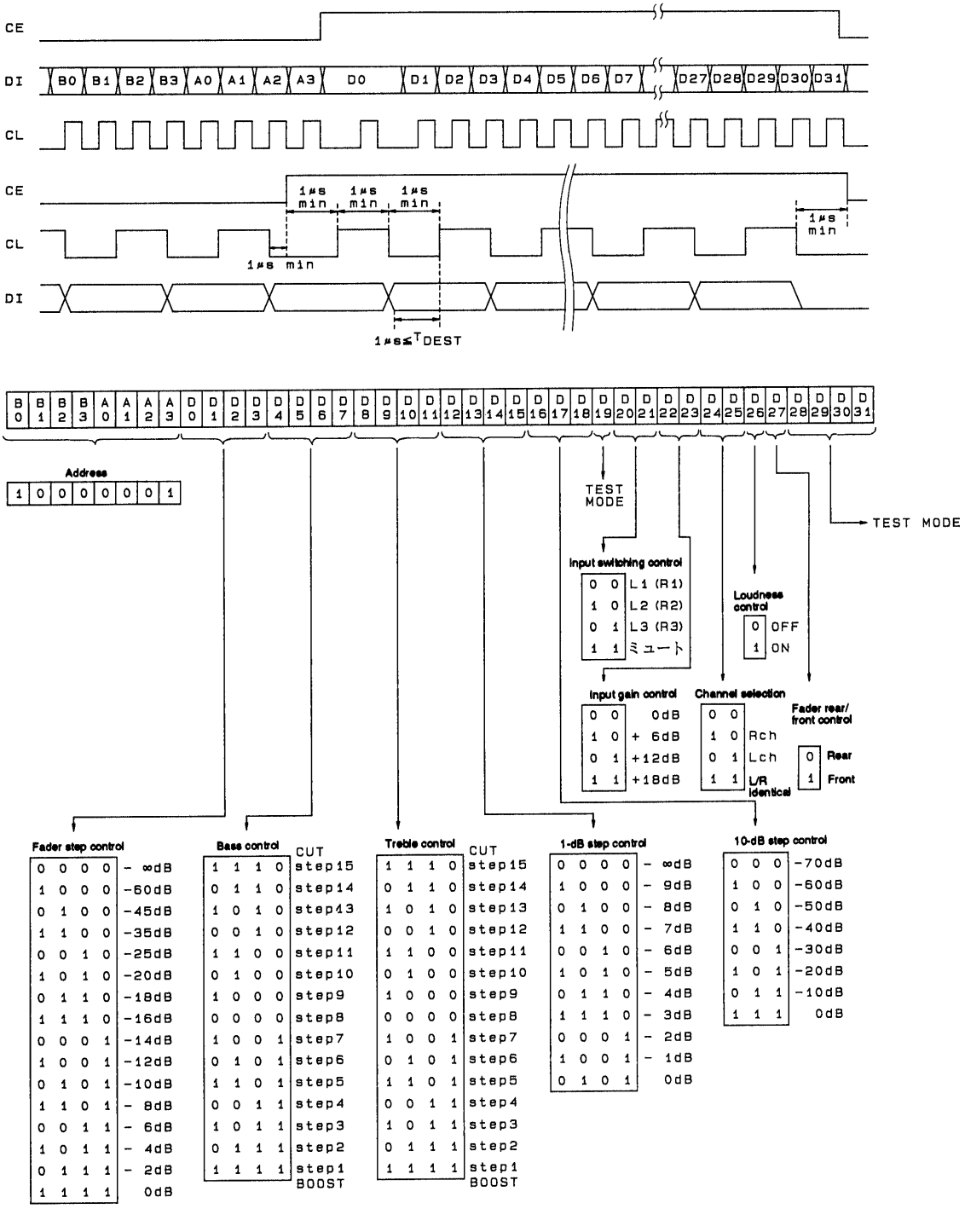


R1, R2, R3: LC75371M internal resistances
C1: External high-band compensation capacitor
C2: External low-band compensation capacitor

Figure 1

Control System Timing and Data Format

The LC75371M is controlled by applying data in the stipulated format to the CE, CL, and DI pins. The data consists of 40 bits, of which 8 bits are the chip address and 32 bits are the data.



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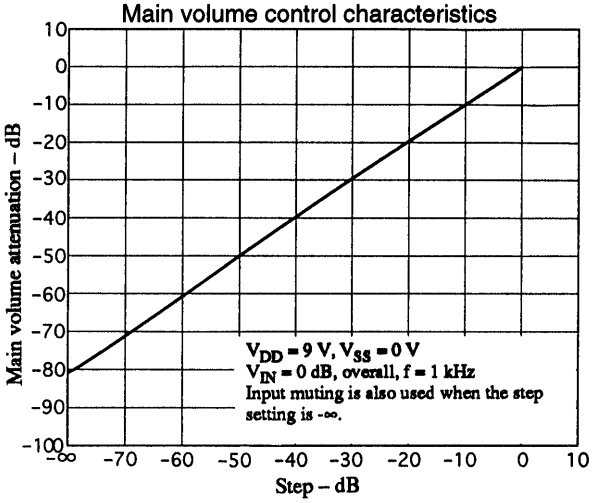
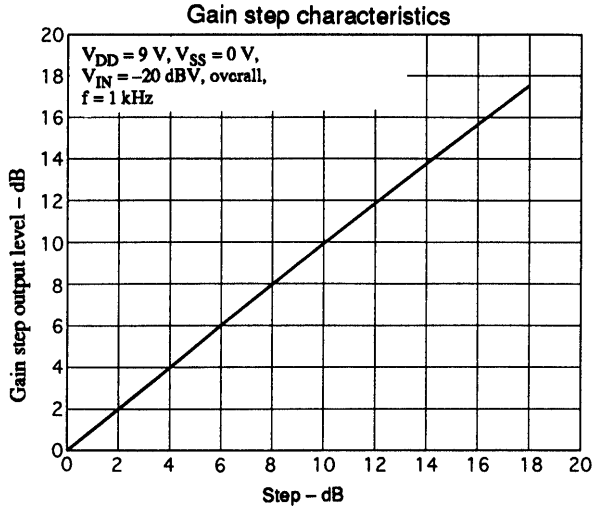
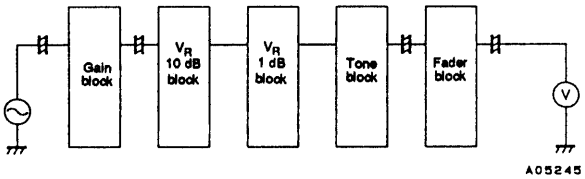
Note: The bits D19 and D28 to D31 are LSI test bits, and must be set to 0.

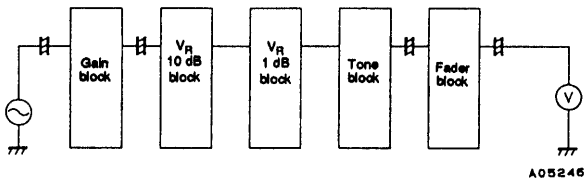
Main volume control characteristics



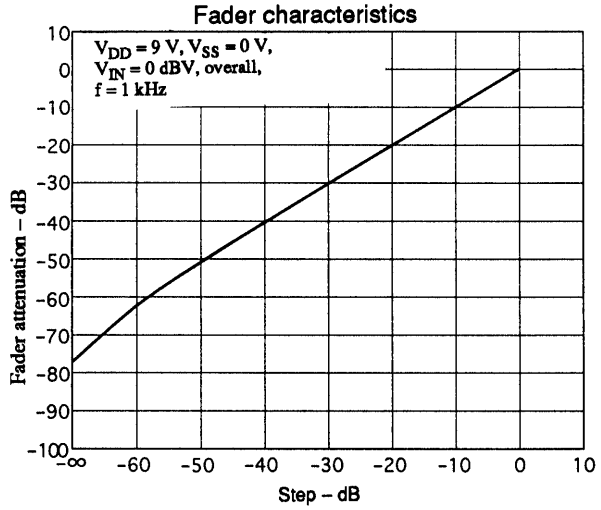
Gain step characteristics



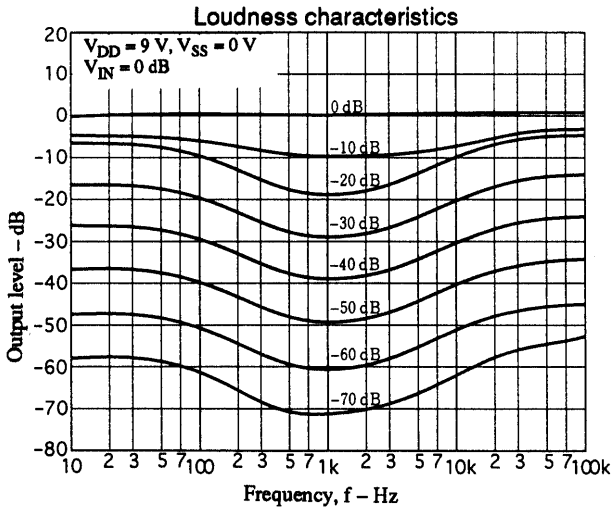


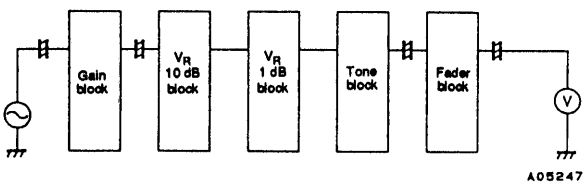


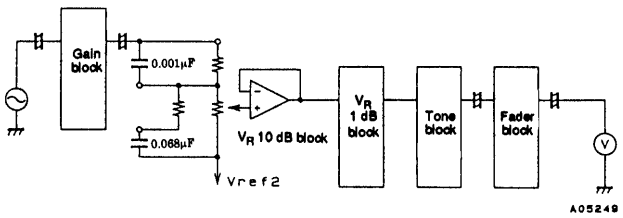
Fader characteristics



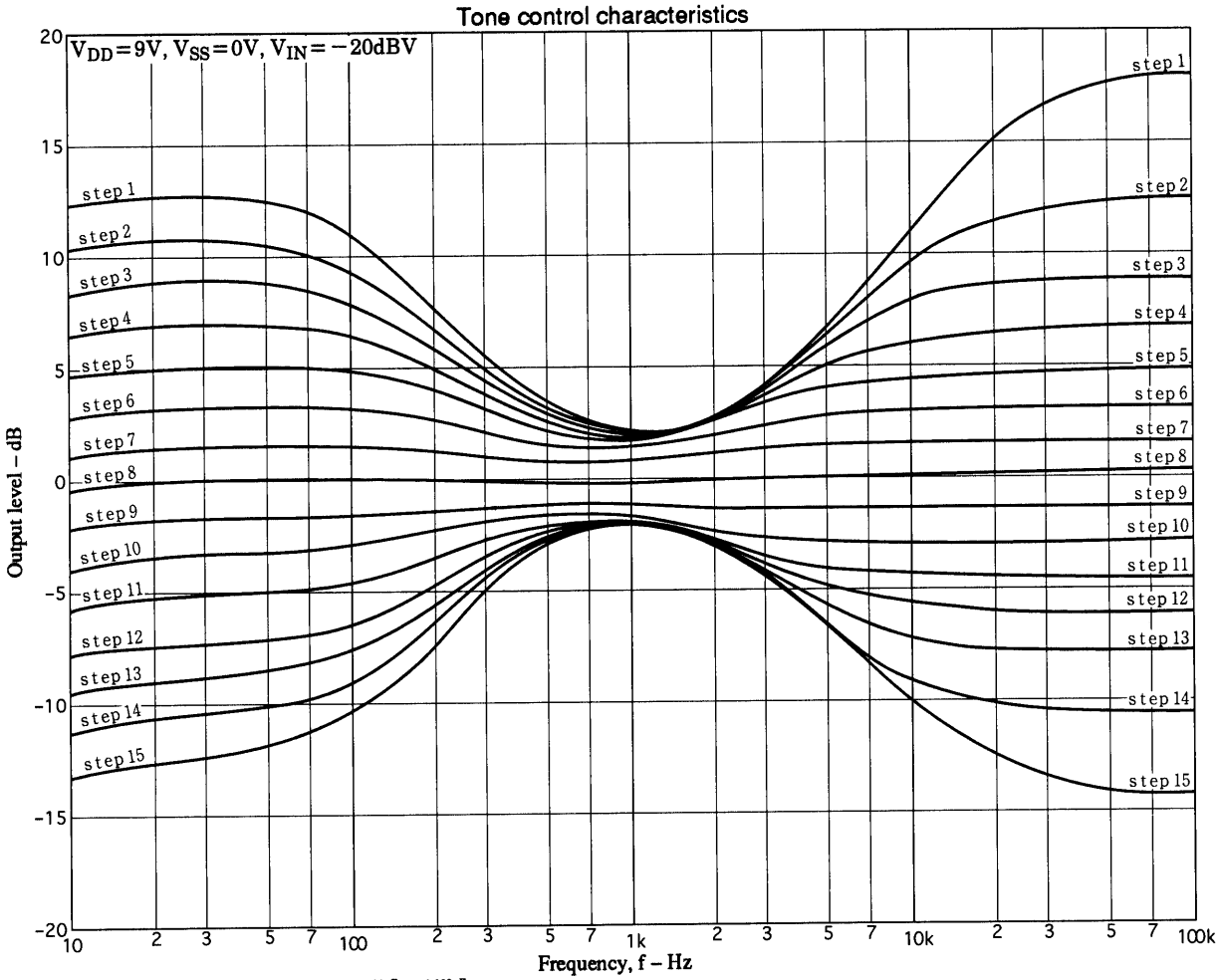
Loudness characteristics

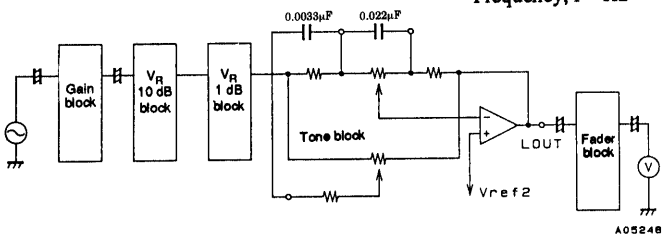




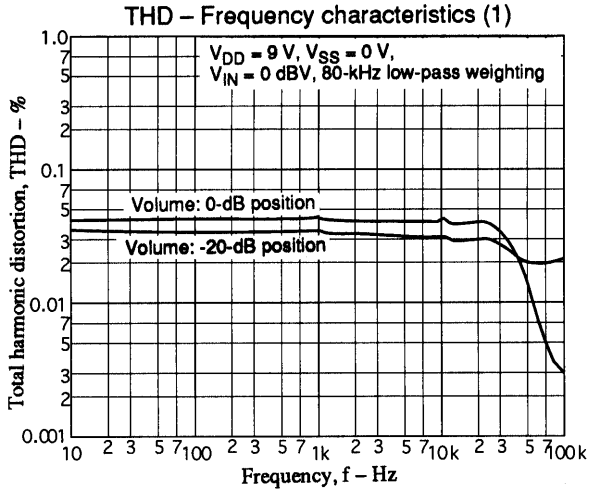


Tone control characteristics

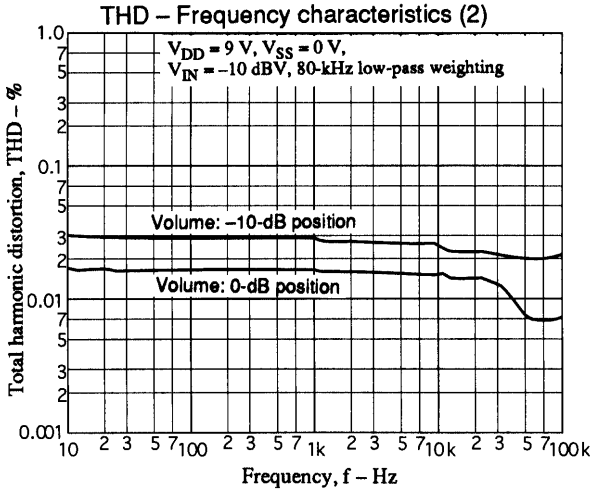


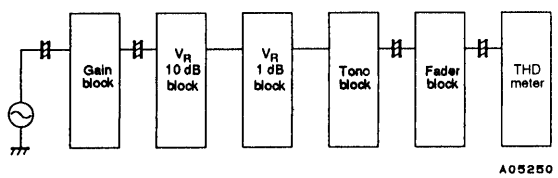


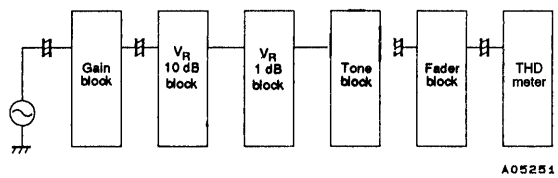
THD – Frequency characteristics (1)



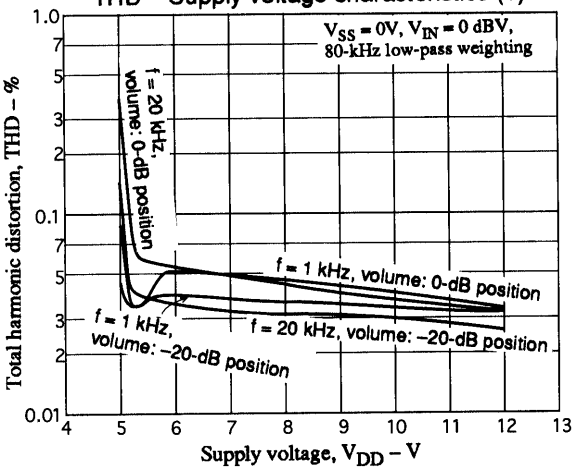
THD – Frequency characteristics (2)

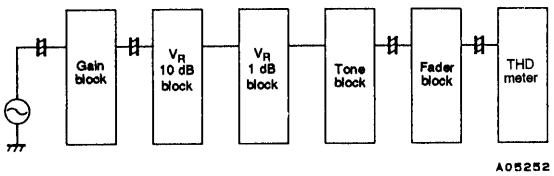






THD – Supply voltage characteristics (1)





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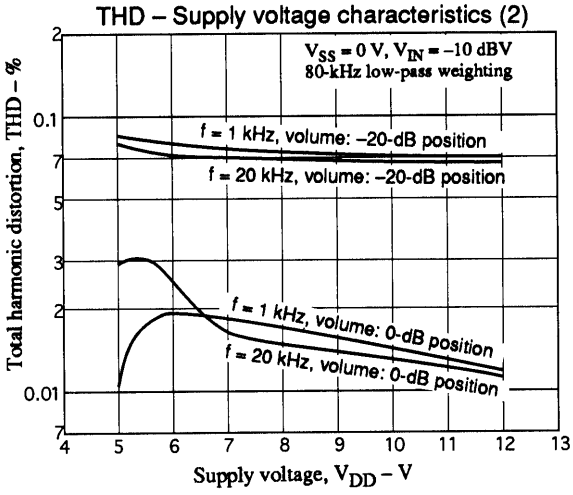
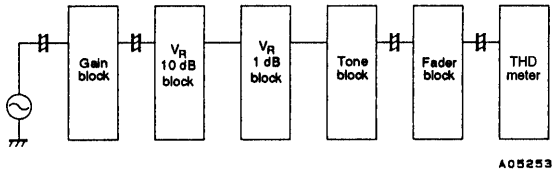
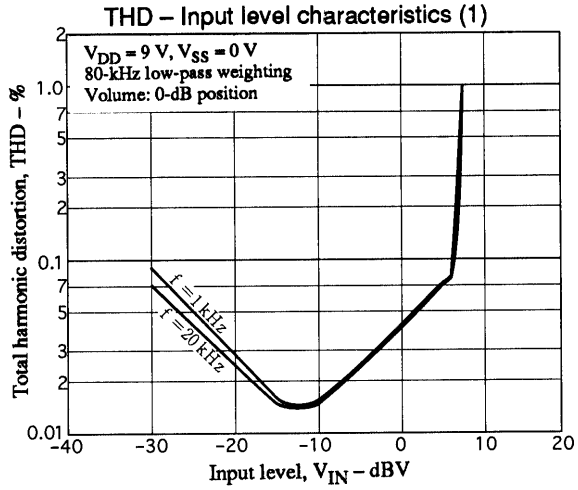
THD – Supply voltage characteristics (2)

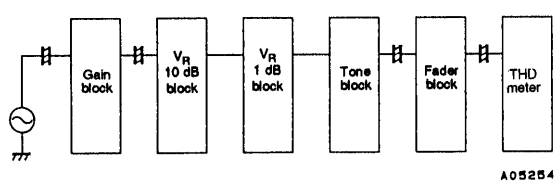




A05253

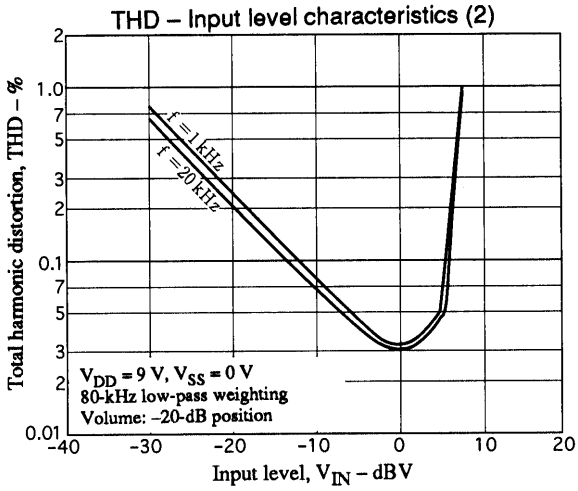
THD – Input level characteristics (1)

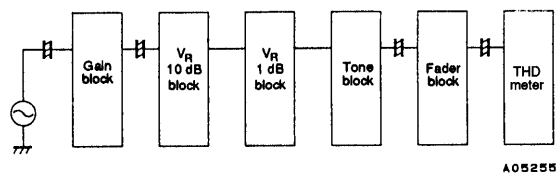




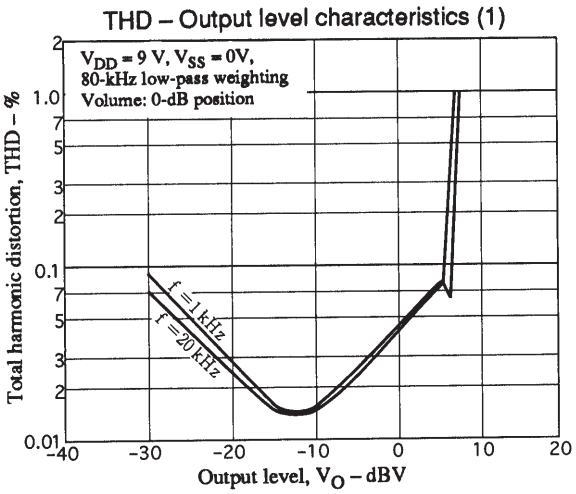
A05254

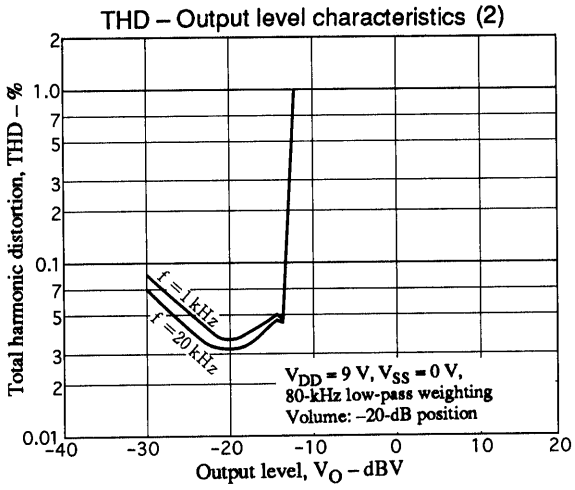
THD – Input level characteristics (2)

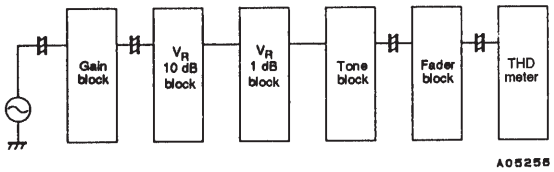


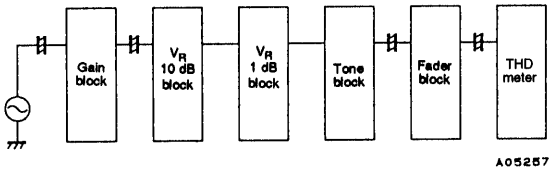


A05255









Usage Notes

1. The states of the internal analog switches are undefined when power is first applied. Use an external muting circuit or other technique to mute the outputs until correct control data has been set up in the LC75371M.
2. Either cover the lines connected to the CL, DI, and CE pins with the ground pattern or use shielded cable for those lines to prevent the high-frequency digital signals on those lines from entering the analog system.
3. Muting by input switching must be used in conjunction with the volume control setting when the maximum volume control attenuation (the VOL = –∞ position) is used.
4. Since there is significant sample-to-sample variation in the magnitude of the main volume switching noise, request a switching noise verification sample to verify the maximum switching noise.