Ordering number : EN*5241

CMOS LSI

LC895125Q, 895125W

CD-ROM Driver with On-Chip SCSI Interface and Subcode Functions

Preliminary

Functions

CD-ROM ECC function, subcode read function, SCSI interface

Features

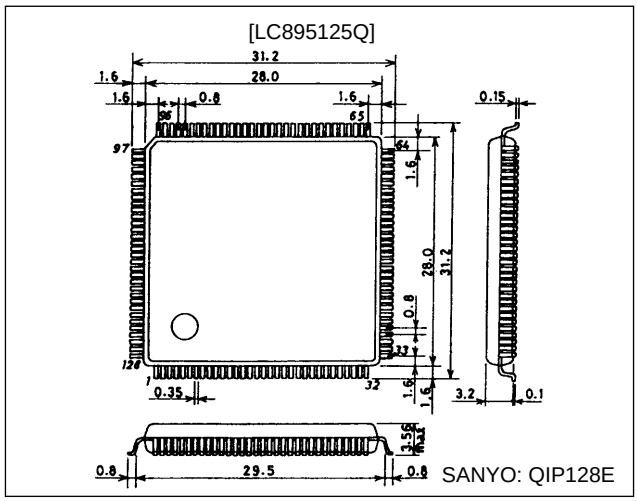
- On-chip SCSI interface (with built-in SCAM selection register)
- Supports 8× playback - Using ×16 80-ns DRAMs
- Supports 4× playback - Using ×16 80-ns DRAMs or ×8 70-ns DRAMs
- Transfer rates: 10 MB/s (synchronous), 5 MB/s (asynchronous) using ×16 80-ns DRAMs*1
- Transfer rates: 8.467 MB/s (synchronous), 4.2336 MB/s (asynchronous) using ×8 70-ns DRAMs*2
- Supports the connection of up to 32 Mb of buffer RAM (using DRAM)
- The user can freely set the CD main channel, C2 flag, and other areas in buffer RAM.
- Batch transfer function (transfers the CD main channel and C2 flag data in a single operation)
- Multi-block transfer function (automatically transfers multiple blocks in a single operation)
- High-speed transfer mode supports a 10-MB/s (synchronous) transfer rate using ×8 80-ns DRAMs
- Subcode ECC function

Note: 1. For speeds up to 8× speed, use a SCSI master clock frequency of 20 MHz.
2. For speeds up to 4× speed, use a SCSI master clock frequency of 16.9344 MHz.

Package Dimensions

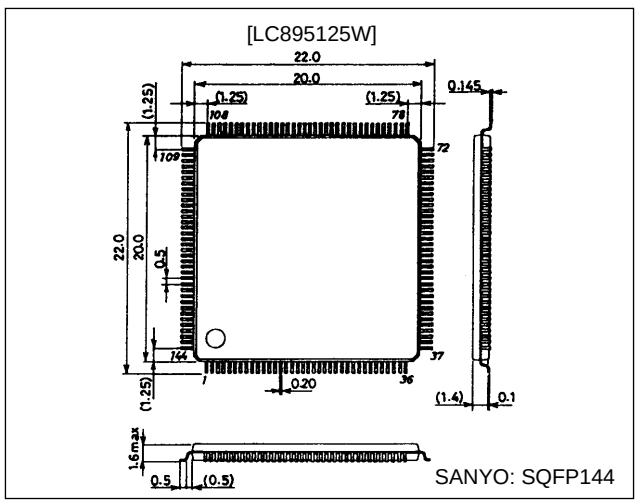
unit: mm

3182-QIP128E



unit: mm

3214-SQFP144



Specifications

Absolute Maximum Ratings at V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	Ta = 25°C	–0.3 to +7.0	V
I/O voltages	V_I, V_O	Ta = 25°C	–0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max	Ta ≤ 70°C	450	mW
Operating temperature	Topr		–30 to +70	°C
Storage temperature	Tstg		–55 to +125	°C
Soldering heat resistance (pins only)		10 seconds	260	°C

Allowable Operating Ranges at Ta = –30 to +70°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
Input voltage range	V_{IN}		0		V_{DD}	V

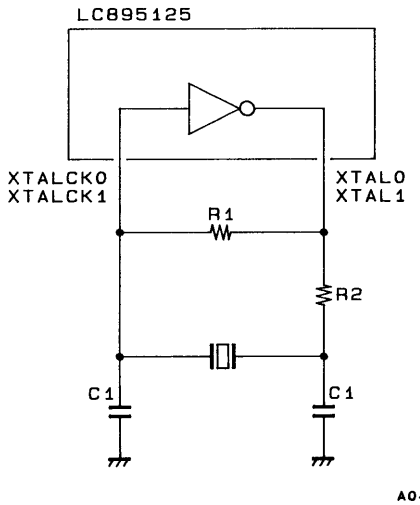
DC Characteristics at V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Ta = –30 to +70°C

Parameter	Symbol	Applicable Pins* (See below)	min	typ	max	Unit
Input high level voltage	$V_{IH}1$	All input pins other than (1), (3), and XTALCK	2.2			V
Input low level voltage	$V_{IL}1$				0.8	V
Input high level voltage	$V_{IH}2$	$\overline{RESET}$, IO0 to IO15, D0 to D7, $\overline{RD}$, $\overline{CS}$, $\overline{WR}$, WFCK, SBSO, SCOR (1)	2.5			V
Input low level voltage	$V_{IL}2$				0.6	V
Input high level voltage	$V_{IH}3$	Input pins (3), $\overline{ACK}$, and $\overline{ATN}$	2.0			V
Input low level voltage	$V_{IL}3$				0.8	V
Output high level voltage	$V_{OH}1$	$I_{OH}1$ = –2 mA: All output pins except (2), (3), and XTALCK, IO0 to IO15, and D0 to D7	2.4			V
Output low level voltage	$V_{OL}1$	$I_{OL}1$ = 2 mA: All output pins except (2), (3), and XTALCK, IO0 to IO15, and D0 to D7			0.4	V
Output low level voltage	$V_{OL}2$	$I_{OL}2$ = 2 mA: $\overline{INT1}$, $\overline{INT0}$, and ZSWAIT (open-drain outputs with pull-up resistors) (2)			0.4	V
Output low level voltage	$V_{OL}3$	$I_{OL}3$ = 48 mA: $\overline{DB0}$, to $\overline{DB7}$, $\overline{DBP}$, $\overline{BSY}$, I/O, $\overline{MSG}$, $\overline{SEL}$, $\overline{RST}$, $\overline{REQ}$, C/D (3)			0.4	V
Input leakage current	I_L	V_I = V_{SS}, V_{DD}: All input pins	–25		+25	µA
Pull-up resistance	R_{UP}	IO0 to IO15, D0 to D7, $\overline{INT0}$, $\overline{INT1}$, ZSWAIT	40	80	160	kΩ

SCSI Pin Input Characteristics

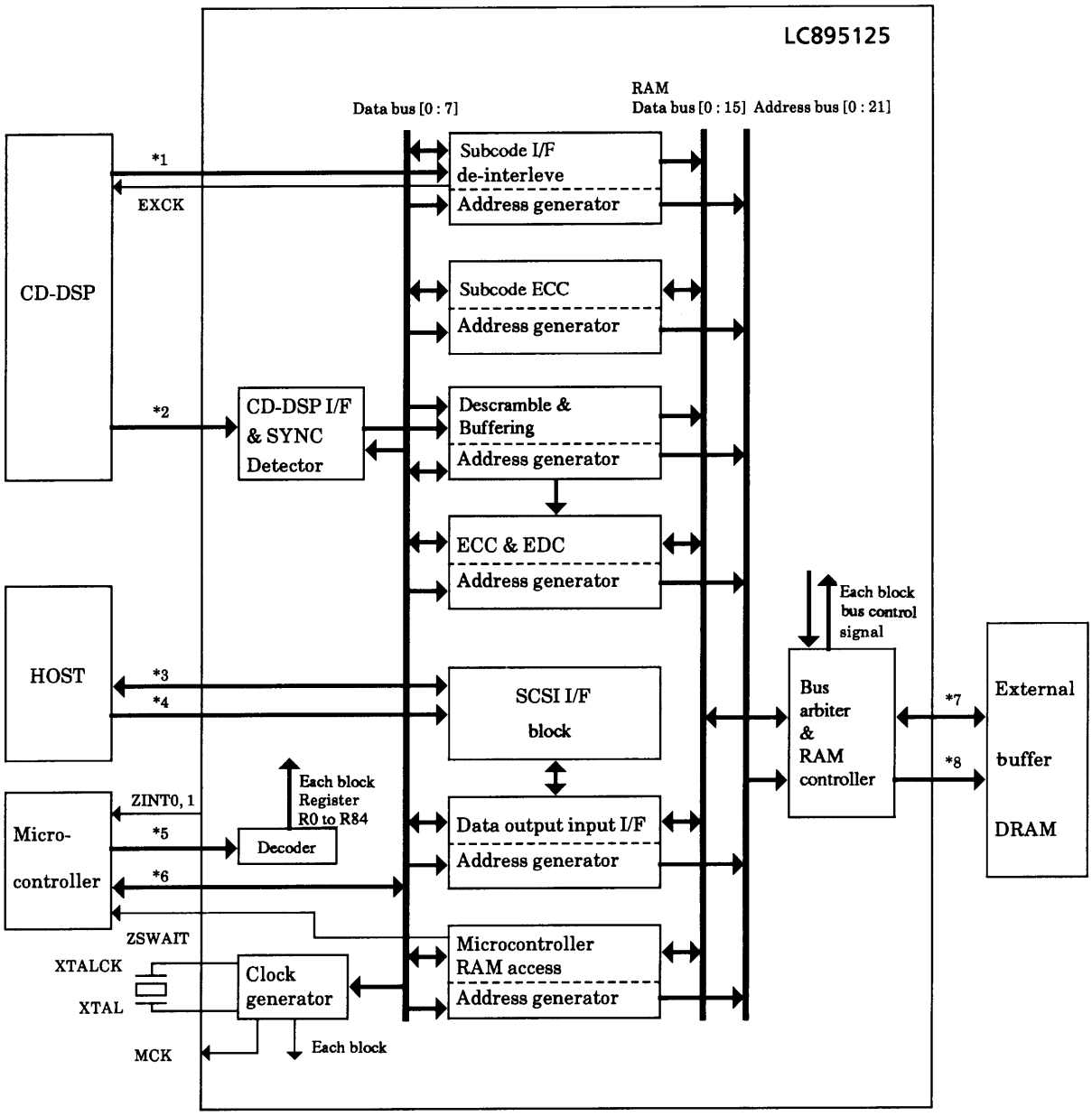
Parameter	Symbol	Conditions	min	typ	max	Unit
Input threshold voltage	V_{t+t1}	V_{DD} = 4.5 to 5.5 V		1.60	2.00	V
	V_{t-t1}		0.80	1.11		V
Hysteresis width	ΔV_{tt1}	V_{DD} = 5.0 V	0.41	0.49		V

Sample Recommended Oscillator Circuit



R1 = 120 kΩ
R2 = 47 Ω
C1 = 30 pF
Crystal oscillator frequencies: XTALCK0 = 16.9344 MHz and XTALCK1 = 20 MHz
or:
R1 = 3.3 kΩ
R2 = None
C1 = 5 pF
Crystal oscillator frequency: XTALCK0 = 33.8688 MHz
If third harmonic overtones appear when using a 33.8688 MHz frequency with the recommended circuit example, consult with the manufacturer of the crystal element, since detailed values of the circuit constants will be influenced by the printed circuit board.

Block Diagram



Note: 1. WFCK, SBSO, SCOR
2. BCK, SDATA, LRCK, C2PO
3. $\overline{DB0}$ to $\overline{DB7}$, $\overline{DBP}$, $\overline{BSY}$, $\overline{MSG}$, $\overline{SEL}$, $\overline{RST}$, $\overline{REQ}$, I/O, C/D
4. $\overline{ACK}$, $\overline{ATN}$
5. ZRD, ZWR, SUA0 to SUA6, ZCS, CSCTRL
6. D0 to D7
7. IO0 to IO15
8. RA0 to RA16, ZRAS0, ZRAS1, ZCAS0, ZCAS1, ZOE, ZUWE, ZLWE

Note: IO8 to IO15 and RA9 to RA16 are the same pins.

Pin Functions (LC895125Q)

Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, NC: No connection pin

Pin No.	Symbol	Type	Function
1	V_{DD}	P	
2	V_{SS0}	P	
3	RA5	O	Address outputs for the buffer RAM
4	RA6	O	
5	RA7	O	
6	RA8	O	
7	RA9 (IO15)	B	Address outputs for the buffer RAM or data I/O pins The pin circuits include pull-up resistors.
8	RA10 (IO14)	B	
9	V_{SS0}	P	
10	RA11 (IO13)	B	Address outputs for the buffer RAM or data I/O pins The pin circuits include pull-up resistors.
11	RA12 (IO12)	B	
12	RA13 (IO11)	B	
13	RA14 (IO10)	B	
14	RA15 (IO9)	B	
15	RA16 (IO8)	B	
16	IO7	B	Buffer RAM data I/O. The pin circuit includes a pull-up resistor.
17	V_{SS0}	P	
18	IO6	B	Buffer RAM data I/O. The pin circuits include pull-up resistors.
19	IO5	B	
20	IO4	B	
21	IO3	B	
22	IO2	B	
23	IO1	B	
24	IO0	B	
25	V_{SS0}	P	
26	TEST0	I	Test pins. These pins must be connected to V_{SS0}.
27	TEST1	I	
28	TEST2	I	
29	TEST3	I	
30	TEST4	I	
31	ZRESET	I	LSI reset. The LSI is reset on a 0 input.
32	V_{DD}	P	
33	V_{SS0}	P	
34	CSCTRL	I	Selects active-high or active-low for the microcontroller CS logic.
35	XTALCK0	I	Crystal oscillator input
36	XTAL0	O	Crystal oscillator output
37	V_{SS0}	P	
38	D0	B	Microcontroller data signals
39	D1	B	
40	D2	B	
41	D3	B	
42	D4	B	
43	D5	B	
44	D6	B	
45	D7	B	
46	V_{SS0}	P	
47	ZSWAIT	O	WAIT signal output to the microcontroller
48	ZINT0	O	Interrupt request output to the microcontroller (ECC side. Set with a register.)
49	V_{DD}	P	
50	ZINT1	O	Interrupt request output to the microcontroller (SCSI side. Set with a register.)

Note: 1. NC pins must be left open. Do not connect any signal to these pins.
2. Pin names that start with Z are negative-logic signals.
3. V_{SS0} is the logic system ground and V_{SS1} is the SCSI interface ground.
4. Applications that use DRAM must insert resistors in the CAS and RAS lines, connect capacitors between these lines and ground, and take any other measures necessary to prevent undershoot in the DRAM related circuits.
5. Since these circuits include buffers that sink 48 mA, adequate noise prevention measures must be applied.

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Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, NC: No connection pin

Pin No.	Symbol	Type	Function
51	ZRD	I	Microcontroller data read signal input
52	ZWR	I	Microcontroller data write signal input
53	ZCS	I	Register chip select signal from the microcontroller
54	SUA0	I	Microcontroller register selection signals
55	SUA1	I	
56	SUA2	I	
57	SUA3	I	
58	SUA4	I	
59	SUA5	I	
60	SUA6	I	
61	V_{SS0}	P	
62	X1EN	I	Selection pin that must be set to 1 when XTALCK1 is used.
63	XTALCK1	I	SCSI block oscillator circuit input. Selected by X1EN.
64	XTAL1	O	SCSI block oscillator circuit output.
65	V_{DD}	P	
66	V_{SS1}	P	
67	$\overline{DB0}$	B	SCSI connection
68	$\overline{DB1}$	B	
69	V_{SS1}	P	
70	$\overline{DB2}$	B	SCSI connection
71	$\overline{DB3}$	B	
72	V_{DD}	P	
73	V_{SS1}	P	
74	$\overline{DB4}$	B	SCSI connection
75	$\overline{DB5}$	B	
76	V_{SS1}	P	
77	$\overline{DB6}$	B	SCSI connection
78	$\overline{DB7}$	B	
79	V_{SS1}	P	
80	$\overline{DBP}$	B	SCSI connection
81	V_{SS1}	P	
82	ATN	B	SCSI connection
83	V_{DD}	P	
84	$\overline{BSY}$	B	SCSI connection
85	$\overline{ACK}$	B	
86	V_{SS1}	P	
87	$\overline{RST}$	B	SCSI connection
88	$\overline{MSG}$	B	
89	V_{DD}	P	
90	$\overline{SEL}$	B	SCSI connection
91	C/D	B	
92	V_{SS1}	P	
93	$\overline{REQ}$	B	SCSI connection
94	I/O	B	
95	V_{SS1}	P	
96	V_{DD}	P	
97	V_{SS0}	P	
98		NC	
99	V_{SS0}	P	
100	V_{SS0}	P	

Note: 1. NC pins must be left open. Do not connect any signal to these pins.
2. Pin names that start with Z are negative-logic signals.
3. V_{SS0} is the logic system ground and V_{SS1} is the SCSI interface ground.
4. Applications that use DRAM must insert resistors in the CAS and RAS lines, connect capacitors between these lines and ground, and take any other measures necessary to prevent undershoot in the DRAM related circuits.
5. Since these circuits include buffers that sink 48 mA, adequate noise prevention measures must be applied.

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Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, NC: No connection pin

Pin No.	Symbol	Type	Function
101	V_{SS0}	P	
102		NC	
103		NC	
104	C2PO	I	CD DSP interface
105	SDATA	I	
106	BCK	I	
107	LRCK	I	
108	MCK	O	Outputs the XTALCK0 frequency, or that frequency divided by 2.
109	V_{SS0}	P	
110	EXCK	O	Subcode I/O
111	WFCK	I	
112	SBSO	I	
113	V_{DD}	P	
114	SCOR	I	Subcode I/O
115	V_{SS0}	P	
116	ZRAS0	O	Buffer RAM RAS signal output pin 0 (Normally, pin 0 is used)
117	ZRAS1	O	Buffer RAM RAS signal output pin 1
118	ZCAS0	O	Buffer RAM CAS signal output pin 0 (Normally, pin 0 is used)
119	ZCAS1	O	Buffer RAM CAS signal output pin 1
120	ZOE	O	Buffer RAM output enable
121	ZUWE	O	Buffer RAM upper write enable
122	ZLWE	O	Buffer RAM lower write enable
123	V_{SS0}	P	
124	RA0	O	Buffer RAM address signal outputs
125	RA1	O	
126	RA2	O	
127	RA3	O	
128	RA4	O	

Note: 1. NC pins must be left open. Do not connect any signal to these pins.
2. Pin names that start with Z are negative-logic signals.
3. V_{SS0} is the logic system ground and V_{SS1} is the SCSI interface ground.
4. Applications that use DRAM must insert resistors in the CAS and RAS lines, connect capacitors between these lines and ground, and take any other measures necessary to prevent undershoot in the DRAM related circuits.
5. Since these circuits include buffers that sink 48 mA, adequate noise prevention measures must be applied.

Pin Functions (LC895125W)

Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, NC: No connection pin

Pin No.	Symbol	Type	Function
1	V_{SS0}	P	
2	V_{DD}	P	
3	V_{SS0}	P	
4	RA5	O	Buffer RAM address signal outputs
5	RA6	O	
6	RA7	O	
7	RA8	O	
8	RA9 (IO15)	B	Address outputs for the buffer RAM or data I/O pins The pin circuits include pull-up resistors.
9	RA10 (IO14)	B	
10	V_{SS0}	P	
11	RA11 (IO13)	B	Address outputs for the buffer RAM or data I/O pins The pin circuits include pull-up resistors.
12	RA12 (IO12)	B	
13	RA13 (IO11)	B	
14	RA14 (IO10)	B	
15	RA15 (IO9)	B	
16	RA16 (IO8)	B	
17	IO7	B	Buffer RAM data I/O. The pin circuit includes a pull-up resistor.
18	V_{DD}	P	
19	V_{SS0}	P	
20		NC	
21	IO6	B	Buffer RAM data I/O. The pin circuit includes a pull-up resistor.
22	IO5	B	
23	IO4	B	
24	IO3	B	
25	IO2	B	
26	IO1	B	
27	IO0	B	
28	V_{SS0}	P	
29	TEST0	I	Test pins. These pins must be connected to V_{SS0}.
30	TEST1	I	
31	TEST2	I	
32	TEST3	I	
33	TEST4	I	
34	ZRESET	I	LSI reset. The LSI is reset on a 0 input.
35	V_{DD}	P	
36	V_{SS0}	P	
37	V_{DD}	P	
38	V_{SS0}	P	
39	CSCTRL	I	Selects active-high or active-low for the microcontroller CS logic.
40	XTALCK0	I	Crystal oscillator input
41	XTAL0	O	Crystal oscillator output
42	V_{SS0}	P	
43	D0	B	Microcontroller data signals
44	D1	B	
45	D2	B	
46	D3	B	
47	D4	B	
48	D5	B	
49	D6	B	
50	D7	B	

Note: 1. NC pins must be left open. Do not connect any signal to these pins.
2. Pin names that start with Z are negative-logic signals.
3. V_{SS0} is the logic system ground and V_{SS1} is the SCSI interface ground.
4. Applications that use DRAM must insert resistors in the CAS and RAS lines, connect capacitors between these lines and ground, and take any other measures necessary to prevent undershoot in the DRAM related circuits.
5. Since these circuits include buffers that sink 48 mA, adequate noise prevention measures must be applied.

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Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, NC: No connection pin

Pin No.	Symbol	Type	Function
51	V_{SS0}	P	
52	ZSWAIT	O	WAIT signal output to the microcontroller
53	ZINT0	O	Interrupt request output to the microcontroller (ECC side. Set with a register.)
54	V_{DD}	P	
55	V_{SS0}	P	
56	ZINT1	O	Interrupt request output to the microcontroller (SCSI side. Set with a register.)
57	ZRD	I	Microcontroller data read signal input
58		NC	
59	ZWR	I	Microcontroller data write signal input
60	ZCS	I	Input for the register chip select signal from the microcontroller
61	SUA0	I	Microcontroller register selection signals
62	SUA1	I	
63	SUA2	I	
64	SUA3	I	
65	SUA4	I	
66	SUA5	I	
67	SUA6	I	
68	V_{SS0}	P	
69	X1EN	I	Selection pin that must be set to 1 when XTALCK1 is used
70	XTALCK1	I	SCSI block oscillator circuit input. Selected by X1EN.
71	XTAL1	O	SCSI block oscillator circuit output
72	V_{SS0}	P	
73	V_{DD}	P	
74	V_{SS1}	P	
75	$\overline{DB0}$	B	SCSI connection
76	$\overline{DB1}$	B	
77	V_{SS1}	P	
78	$\overline{DB2}$	B	SCSI connection
79	$\overline{DB3}$	B	
80		NC	
81	V_{DD}	P	
82	V_{SS1}	P	
83	$\overline{DB4}$	B	SCSI connection
84	$\overline{DB5}$	B	
85	V_{SS1}	P	
86	$\overline{DB6}$	B	SCSI connection
87	$\overline{DB7}$	B	
88	V_{SS1}	P	
89	$\overline{DBP}$	B	SCSI connection
90	V_{DD}	P	
91	V_{SS1}	P	
92		NC	
93	$\overline{ATN}$	B	SCSI connection
94	V_{DD}	P	
95	$\overline{BSY}$	B	SCSI connection
96	$\overline{ACK}$	B	
97	V_{SS1}	P	
98	$\overline{RST}$	B	SCSI connection
99	$\overline{MSG}$	B	
100	V_{DD}	P	

Note: 1. NC pins must be left open. Do not connect any signal to these pins.
2. Pin names that start with Z are negative-logic signals.
3. V_{SS0} is the logic system ground and V_{SS1} is the SCSI interface ground.
4. Applications that use DRAM must insert resistors in the CAS and RAS lines, connect capacitors between these lines and ground, and take any other measures necessary to prevent undershoot in the DRAM related circuits.
5. Since these circuits include buffers that sink 48 mA, adequate noise prevention measures must be applied.

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Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, NC: No connection pin

Pin No.	Symbol	Type	Function
101	$\overline{SEL}$	B	SCSI connection
102	C/D	B	
103	V_{SS1}	P	
104	$\overline{REQ}$	B	SCSI connection
105	I/O	B	
106	V_{SS1}	P	
107	V_{DD}	P	
108	V_{SS0}	P	
109	V_{DD}	P	
110	V_{SS0}	P	
111		NC	
112	V_{SS0}	P	
113	V_{SS0}	P	
114	V_{SS0}	P	
115		NC	
116		NC	
117	C2PO	I	CD DSP interface
118	SDATA	I	
119	BCK	I	
120	LRCK	I	
121	MCK	O	Outputs the XTALCK0 frequency, or that frequency divided by 2.
122	V_{SS0}	P	
123	EXCK	O	Subcode I/O
124	WFCK	I	
125	SBSO	I	
126	V_{DD}	P	
127	V_{SS0}	P	
128	SCOR	I	Subcode I/O
129	V_{SS0}	P	
130		NC	
131	ZRAS0	O	Buffer RAM RAS signal output pin 0 (Normally, pin 0 is used)
132	ZRAS1	O	Buffer RAM RAS signal output pin 1
133	ZCAS0	O	Buffer RAM CAS signal output pin 0 (Normally, pin 0 is used)
134	ZCAS1	O	Buffer RAM CAS signal output pin 1
135	ZOE	O	Buffer RAM output enable
136	ZUWE	O	Buffer RAM upper write enable
137	ZLWE	O	Buffer RAM lower write enable
138	V_{SS0}	P	
139	RA0	O	Buffer RAM address signal outputs
140	RA1	O	
141	RA2	O	
142	RA3	O	
143	RA4	O	
144	V_{DD}	P	

Note: 1. NC pins must be left open. Do not connect any signal to these pins.
2. Pin names that start with Z are negative-logic signals.
3. V_{SS0} is the logic system ground and V_{SS1} is the SCSI interface ground.
4. Applications that use DRAM must insert resistors in the CAS and RAS lines, connect capacitors between these lines and ground, and take any other measures necessary to prevent undershoot in the DRAM related circuits.
5. Since these circuits include buffers that sink 48 mA, adequate noise prevention measures must be applied.

Pin Functions

1. SCSI Pins
   - $\overline{\text{BSY}}$, $\overline{\text{ACK}}$, $\overline{\text{MSG}}$, $\overline{\text{SEL}}$, $\overline{\text{REQ}}$, $\overline{\text{ATN}}$, I/O, C/D (input and output)
     SCSI bus control pins.

   - $\overline{\text{DB0}}$ to $\overline{\text{DB7}}$, $\overline{\text{DBPB}}$ (input and output)
     These are the SCSI data bus pins.

2. Microcontroller Interface Pins
   - ZCS (input)
     Microcontroller chip select line
   - CSCTRL (input)
     Microcontroller chip select logic selection signal
     High - ZCS is an active low signal.
     Low - ZCS is an active high signal.
   - ZRD, ZWR, SUA0 to SUA6 (input)
     Microcontroller interface control signal
     The SUA0 to SUA6 pins are used for addressing.
   - ZSWAIT (output)
     When the microcontroller accesses RAM, it must wait if this pin is low.
     This is a built-in pull-up resistor open-drain output.
   - D7 to D0 (input and output)
     Microcontroller data bus. Pull-up resistors are built in.
   - ZINT0, ZINT1 (output)
     Interrupt request output to the microcontroller. A SCSI-side interrupt can be output from ZINT1 by setting the C register (bit 7 in R11).
     This is a built-in pull-up resistor open-drain output.

3. Buffer RAM Pins
   - IO0 to IO15 (input and output)
     Buffer RAM data bus. Pull-up resistors are built in. The IO8 to IO15 pins have shared functions as the RA9 to RA16 pins.
     This means that 16-bit PSRAM cannot be used.
   - RA0 to RA16 (output)
     Buffer RAM address lines. RA9 to RA16 have shared functions as the IO8 to IO15 pins.
     This means that 16-bit PSRAM cannot be used.
   - ZRAS0, ZRAS1, (ZCS0), (ZCS1) (output)
     Buffer DRAM RAS outputs. Normally, ZRAS0 is used. However, when two 1-MB (64k × 16-bit) DRAM chips are used, the respective DRAM RAS pins are connected to ZRAS0 and ZRAS1. Connected to the CS pin if PSRAM is used.
   - ZCAS0, ZCAS1 (output)
     Buffer DRAM CAS outputs. Normally, ZCAS0 is used. However, when two 1-MB (64k × 16-bit) DRAM chips are used, the respective DRAM CAS pins are connected to ZCAS0.
   - ZOE (output)
     Buffer RAM read output signal
   - ZUWE, ZLWE (output)
     Buffer RAM write output signals. Connected to the corresponding pins on the RAM chip.
     Leave ZUWE open if an 8-bit RAM is used.

4. Subcode Interface Pins
   - EXCK, WFCK, SBSO, SCOR (input and output)
     Subcode interface pins. Connecting a CD DSP using these pins allows the LC895125 to read in subcode data and transfer it to the host.

5. CD DSP Data Pins
   - BCK, SDATA, LRCK, C2PO (input)
     The LC895125 reads in CD-ROM data over these pins connected to a CD DSP.
     C2PO is the C2 flag pin.

6. Other Pins
   - ZRESET (input)
     Reset input to the LC895125. The LC895125 is reset by a low-level input.
     This pin must be held low for a period of at least 1 μs when power is first applied.
   - XTALCK0, XTAL0
     The main clock for the ECC and SCSI blocks. These pins support frequencies from 16.9344 to 25 MHz.
     When a double-frequency input is used, these pins accept frequencies up to 38 MHz.
     Use a double-frequency input when a ceramic oscillator and DRAM are used.
     (This is because the internal clock must have a 50% duty.)
     An external clock may input to the XTALCK pin.
     The SCSI block main clock can also be provided from XTALCK1 and XTAL1 if so specified by the setting of X1EN (pin 89).
   - XTALCK1, XTAL1
     The main clock for the ECC and SCSI blocks. These pins are enabled for oscillator operation by setting X1EN (pin 89). The LC895125 is designed so that the ECC and SCSI blocks can also be operated asynchronously.
     This means that precise 10-MB/s synchronous transfers can be achieved by providing a 20-MHz input to XTALCK1 and XTAL1.
     A ceramic oscillator may be used here since only the rising edge of this signal is used.
     In applications that do not use these pins, XTALCK1 must be tied to V_{SS} and XTAL1 must be left open.
   - X1EN (input)
     Set this pin to 1 to us use XTALCK1 and XTAL1 for the SCSI block main clock.
     Set this pin to 0 to drive both the ECC and SCSI blocks from XTALCK0 and XTAL0.
   - MCK (output)
     Outputs either the XTALCK0 frequency or that frequency divided by 2. This pin's output can also be stopped if desired.