Ordering number : EN*5237

CMOS LSI

LC8905V

Digital Audio Interface Receiver

Preliminary

Overview

The LC8905V is for use in IEC 958 and EIAJ CP-1201 format data transmission between digital audio equipment. This LSI is used on the receiving side, and handles synchronization with the input signal and demodulation of that signal to a normal format signal.

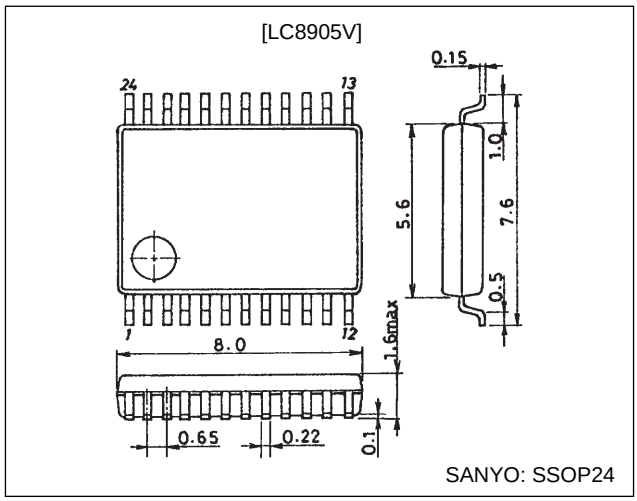
Features

- On-chip PLL circuit synchronizes with the transmitted IEC 958 and EIAJ CP-1201 format signal.
- Provides 128fs, bit, and L/R clock outputs.
- System clock can be selected to be either 384fs or 512fs.
- Microprocessor interface code settings for different output types
  - — Input pin, emphasis output, input bi-phase data output, and validity flag output settings
  - — Audio data output format setting
  - — Channel status output (32-bit output for consumer products)
  - — Subcode Q output with CRC flags (80 bits)
- Start ID and shortening ID detection for DAT (Digital Audio Tape recorder) that use subcodes
- CMOS, single-voltage power supply
- Miniature package: SSOP-24

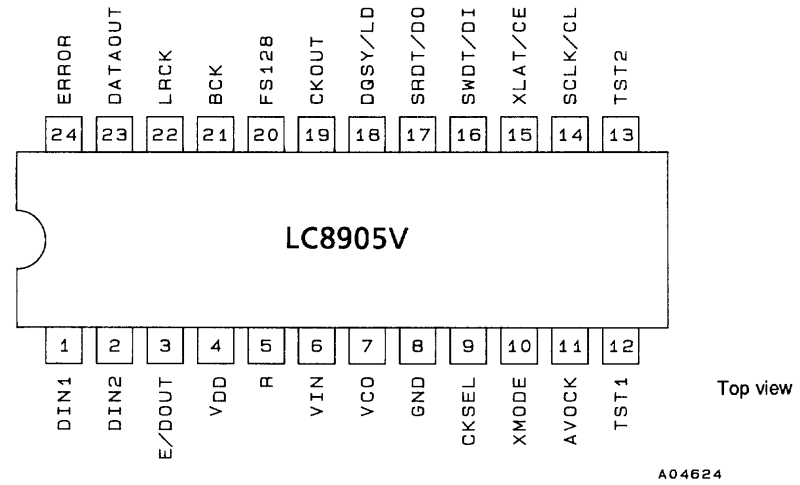
Package Dimensions

unit: mm

3175A-SSOP24



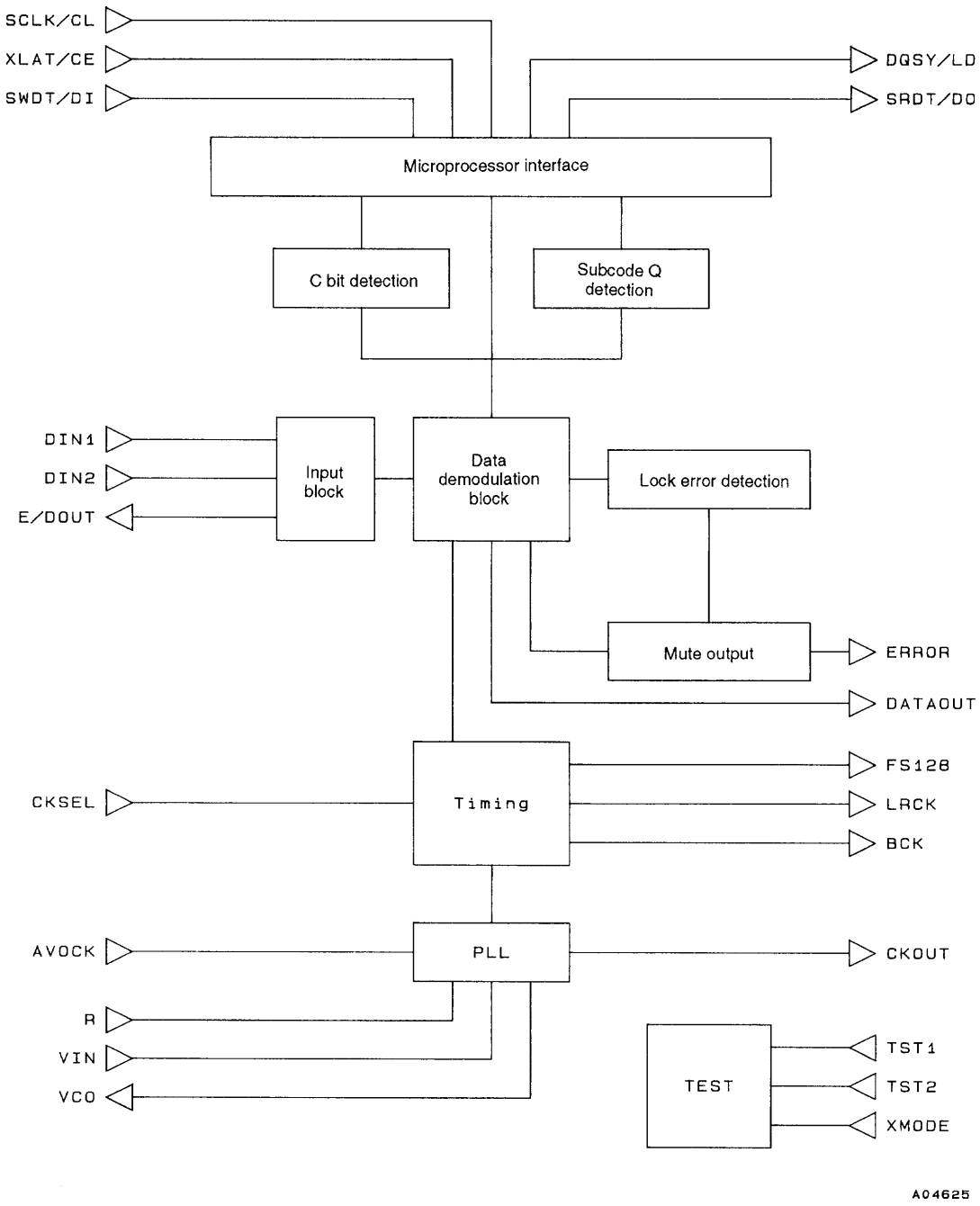
Pin Assignment



Pin Functions

Pin No.	Symbol	I/O	Description
1	DIN1	I	Data input with built-in amplifier (for coaxial or optical module input)
2	DIN2	I	Data input (for optical module input)
3	E/DOUT	O	Emphasis, input bi-phase, and validity flag output
4	V_{DD}		Power supply
5	R	I	VCO gain control input
6	VIN	I	VCO free-running setting input
7	VCO	O	PLL low-pass filter setting
8	GND		Ground
9	CKSEL	I	System clock selection input (384fs or 512fs)
10	XMODE	I	Reset input
11	AVOCK	I	PLL error lock avoidance clock input
12	TST1	I	Test input (Must be connected to ground in normal operation)
13	TST2	I	Test input (Must be connected to ground in normal operation)
14	SCLK/CL	I	Microprocessor interface clock input
15	XLAT/CE	I	Microprocessor interface latch/chip enable input
16	SWDT/DI	I	Microprocessor interface write data input
17	SRDT/DO	O	Microprocessor interface read data output
18	DQSY/LD	O	Microprocessor interface subcode Q and ID synchronization output
19	CKOUT	O	VCO clock output (free running, 384fs, or 512fs)
20	FS128	O	128fs clock output
21	BCK	O	Bit clock output
22	LRCK	O	L/R clock output (left channel = high, right channel = low)
23	DATAOUT	O	Audio data output
24	ERROR	O	PLL lock error mute output

Block Diagram



Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		–0.3 to +7.0	V
Maximum I/O voltages	V_I V_O max		–0.3 to V_{DD} + 0.3	V
Operating temperature	Topr		–30 to +75	°C
Storage temperature	Tstg		–55 to +125	°C

Allowable Operating Ranges

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V

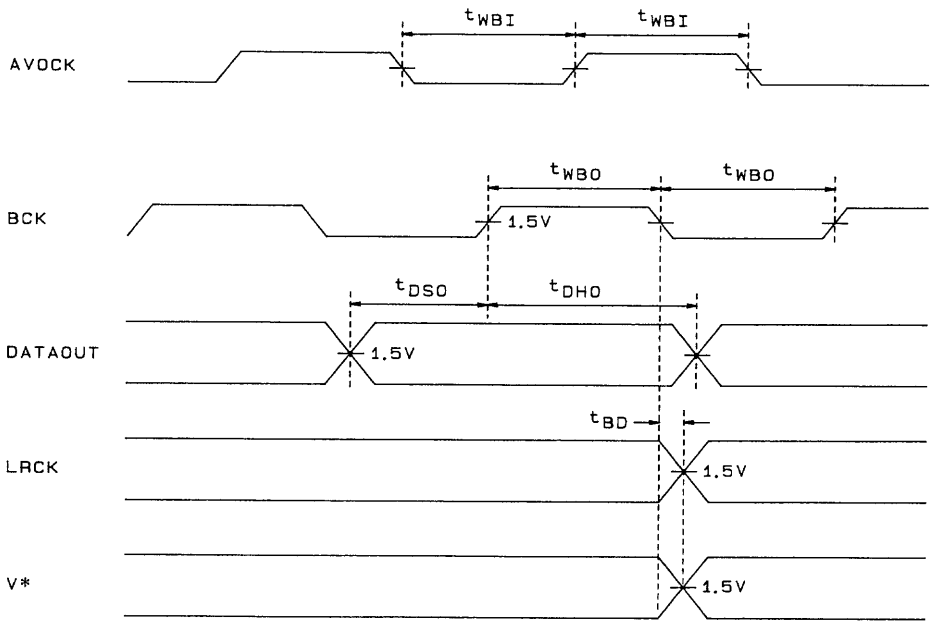
Electrical Characteristics

DC Characteristics at Ta = –30 to +75°C, V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Input high-level voltage	$V_{IH}1$	Applies to the DIN2 pin. TTL levels	2.2		V_{DD} + 0.3	V
Input low-level voltage	$V_{IL}1$	Applies to the DIN2 pin. TTL levels	–0.3		+0.8	V
Input high-level voltage	$V_{IH}2$	Applies to the CKSEL, AVOCK, TST1, and TST2 pins. CMOS levels	0.7 V_{DD}		V_{DD} + 0.3	V
Input low-level voltage	$V_{IL}2$	Applies to the CKSEL, AVOCK, TST1, and TST2 pins. CMOS levels	–0.3		0.3 V_{DD}	V
Input high-level voltage	$V_{IH}3$	Applies to the XMODE, SCLK/CL, XLAT/CE, SWDT/DI pins. CMOS Schmitt inputs	0.8 V_{DD}		V_{DD} + 0.3	V
Input low-level voltage	$V_{IL}3$	Applies to the XMODE, SCLK/CL, XLAT/CE, SWDT/DI pins. CMOS Schmitt inputs	–0.3		0.2 V_{DD}	V
Input high-level voltage	V_{OH}	I_{OH} = –1 µA	V_{DD} – 0.05			V
Input low-level voltage	V_{OL}	I_{OL} = 1 µA			V_{DD} + 0.05	V
Current drain	I_{DD}	V_{DD} = 5.0 V, Ta = 25°C, input data fs = 48 kHz		10	15	mA
Input amplitude	Vpp	Measured before the DIN1 pin input capacitor.	0.4		V_{DD} + 0.3	V

AC Characteristics at Ta = –30 to +75°C, V_{DD} = 4.5 to 5.5 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Input pulse width	t_{WBI}		10			µs
Output pulse width	t_{WBO}	fs = 48 kHz	160			ns
Output data setup time	t_{DSO}		80			ns
Output data hold time	t_{DHO}		80			ns
Output delay	t_{BD}		–10	0	+10	ns



* Note: When the validity flag is output from the E/DOUT pin

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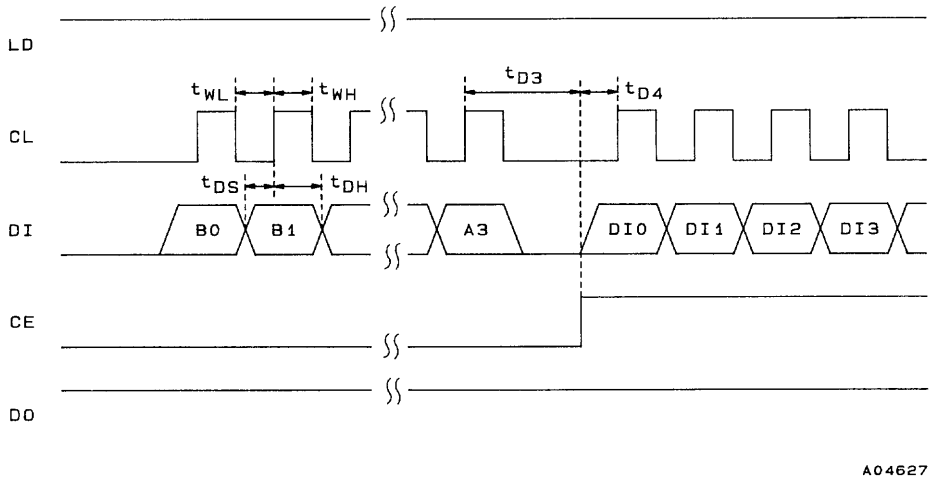
Microprocessor Interface Block AC Characteristics

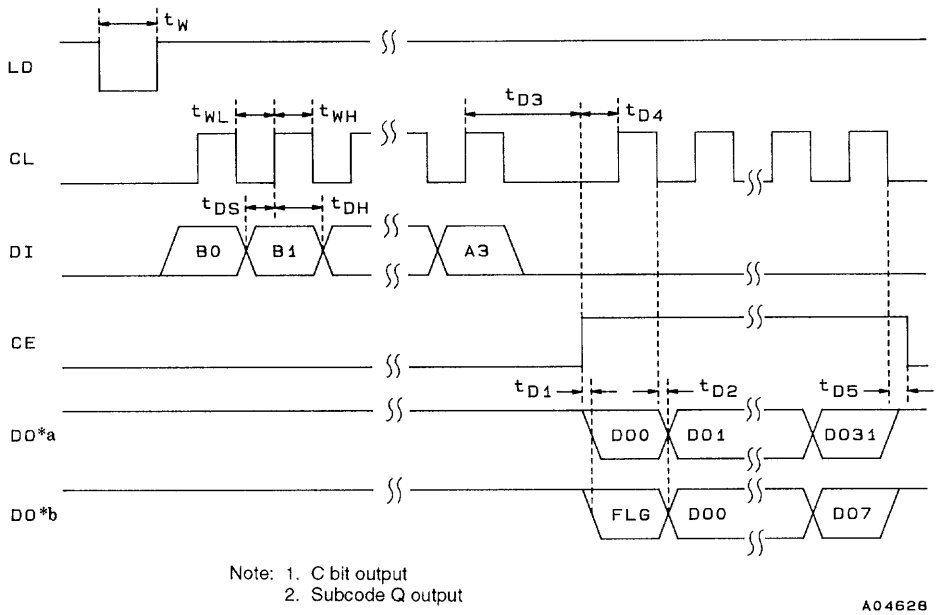
at Ta = –30 to +75°C, V_{DD} = 4.5 to 5.5 V (when CKSEL is low)

Parameter	Symbol	Conditions	min	typ	max	Unit
CL low pulse width	t_{WL}		100			ns
CL high pulse width	t_{WH}		100			ns
Data setup time	t_{DS}		50			ns
Data hold time	t_{DH}		50			ns
CE delay time	t_{D3}		1.0			µs
CL delay time	t_{D4}		50			ns
CE delay time	t_{D5}				100	ns
LD pulse width	t_W	fs = 44.1 kHz		136		µs
Data delay time	t_{D1}	CL = 30 pF			75	ns
Data delay time	t_{D2}	CL = 30 pF			75	ns

Input mode



Output mode



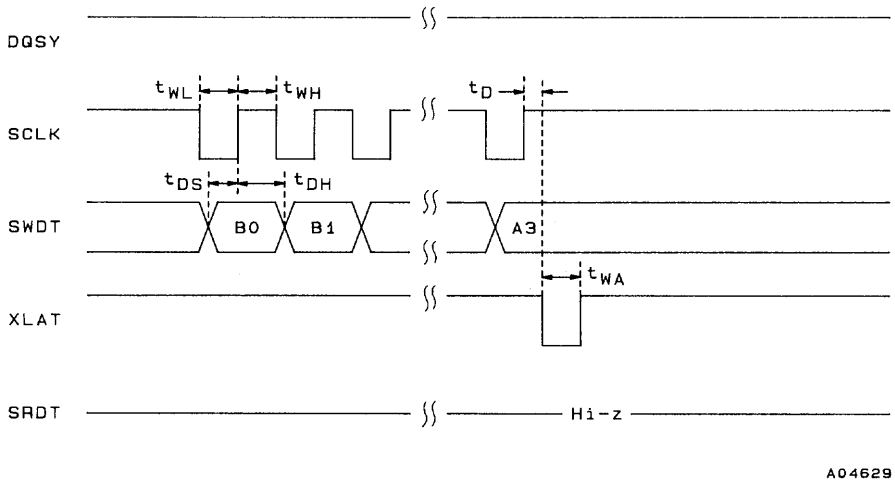
Note: 1. C bit output
2. Subcode Q output

Microprocessor Interface Block AC Characteristics

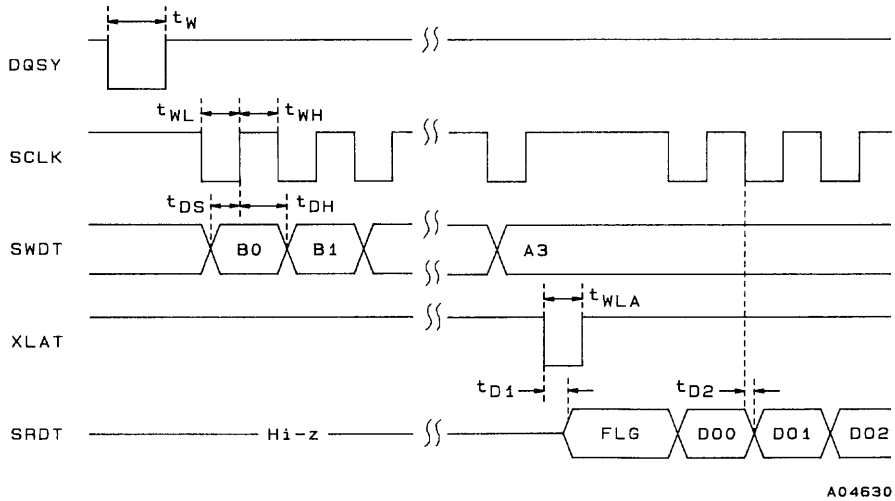
at Ta = –30 to +75°C, V_{DD} = 4.5 to 5.5 V (when CKSEL is high)

Parameter	Symbol	Conditions	min	typ	max	Unit
CL low pulse width	t_{WL}		100			ns
CL high pulse width	t_{WH}		100			ns
Data setup time	t_{DS}		50			ns
Data hold time	t_{DH}		50			ns
CE delay time	t_D		100			µs
LD pulse width	t_W	fs = 44.1 kHz		136		µs
Data delay time	t_{D1}	CL = 30 pF			75	ns
Data delay time	t_{D2}	CL = 30 pF			75	ns

Input mode



Output mode



Functions

1. Data Input and Output (DIN1, DIN2, E/DOUT)
   The DIN1 pin has a built-in amplifier, and can receive signals with an amplitude of about 400 mVp-p (coaxial input).
   The DIN2 pin is only for use with optical modules.
   Note that although the data input pins are controlled by the microprocessor, DIN1 can be selected when a microprocessor is not used. The microprocessor interface pins must be tied low in such applications.
   The E/DOUT normally outputs channel status information. However, it can be set to output either the input bi-phase data or the validity flag by command codes from the microprocessor.
2. PLL (R, VIN, VCO, AVOCK)
   This circuit includes a built-in VCO and supports sampling frequencies of 32, 44.1, and 48 kHz.
   The resistor connected to R functions as both the VCO gain control and as temperature compensation. The VIN pin sets the VCO free-running frequency.
   The PLL circuit can be reset within a fixed period when it operates incorrectly, for example, if a lock pull-in failure occurs, by inputting an asynchronous, continuously operating clock signal to the AVOCK pin.
3. Clock Settings and Output (FS128, BCK, LRCK, DATAOUT, CKSEL, CKOUT)
   A 128fs clock signal is output from the FS128 pin. Figure 1 shows the output timing for the BCK, LRCK, and DATAOUT pins.
   The CKOUT clock output is set by the CKSEL pin as listed in the table below.

CKSEL	CKOUT
L	384fs clock output
H	512fs clock output

   The microprocessor interface format is also set by CKSEL as listed in the table below.

CKSEL	Microprocessor interface
L	Figure 2
H	Figure 3

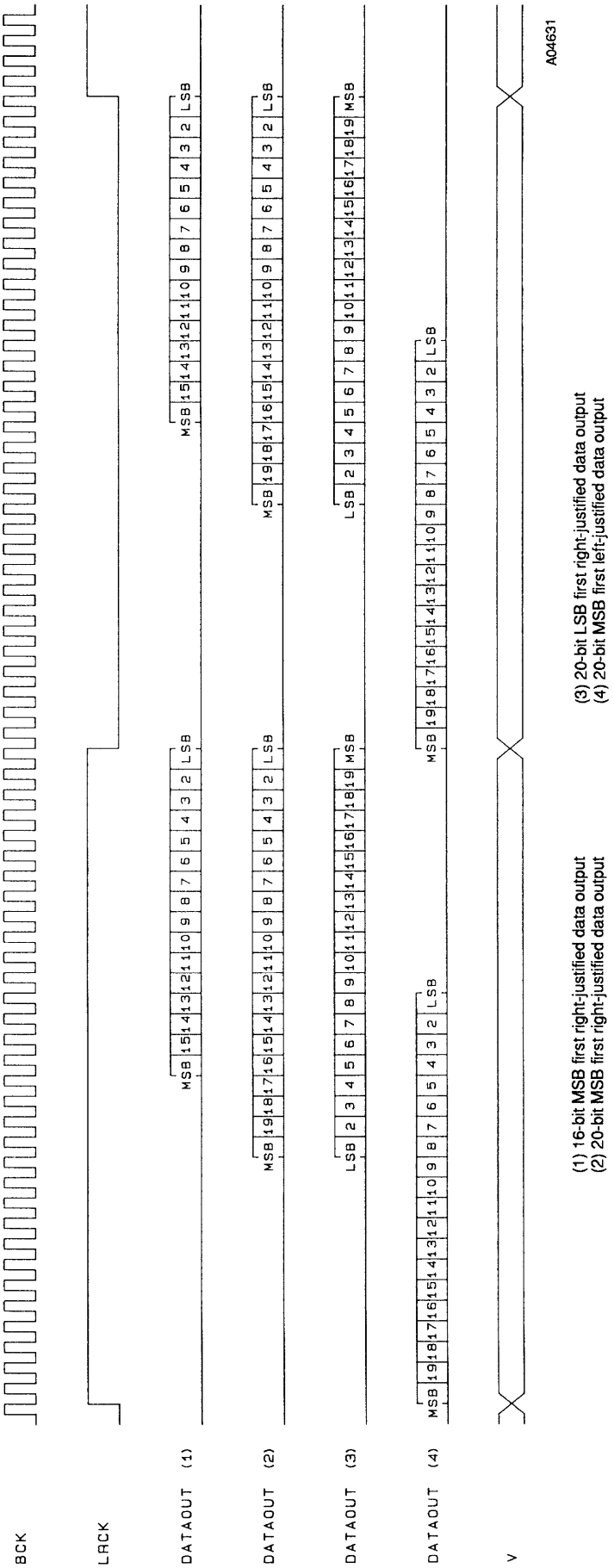


Figure 1 Data Output Timing

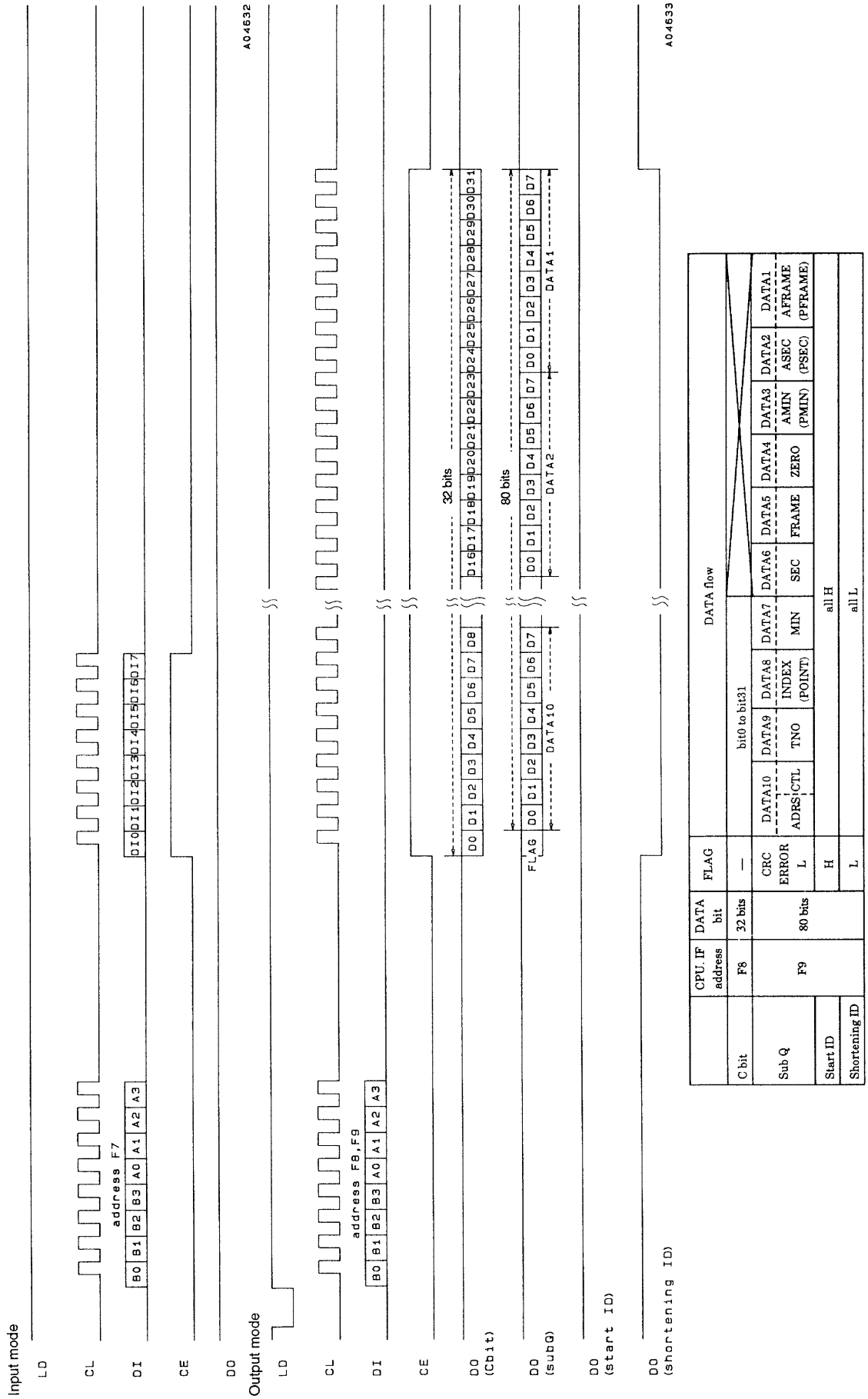


Figure 2 Microprocessor Interface Timing 1

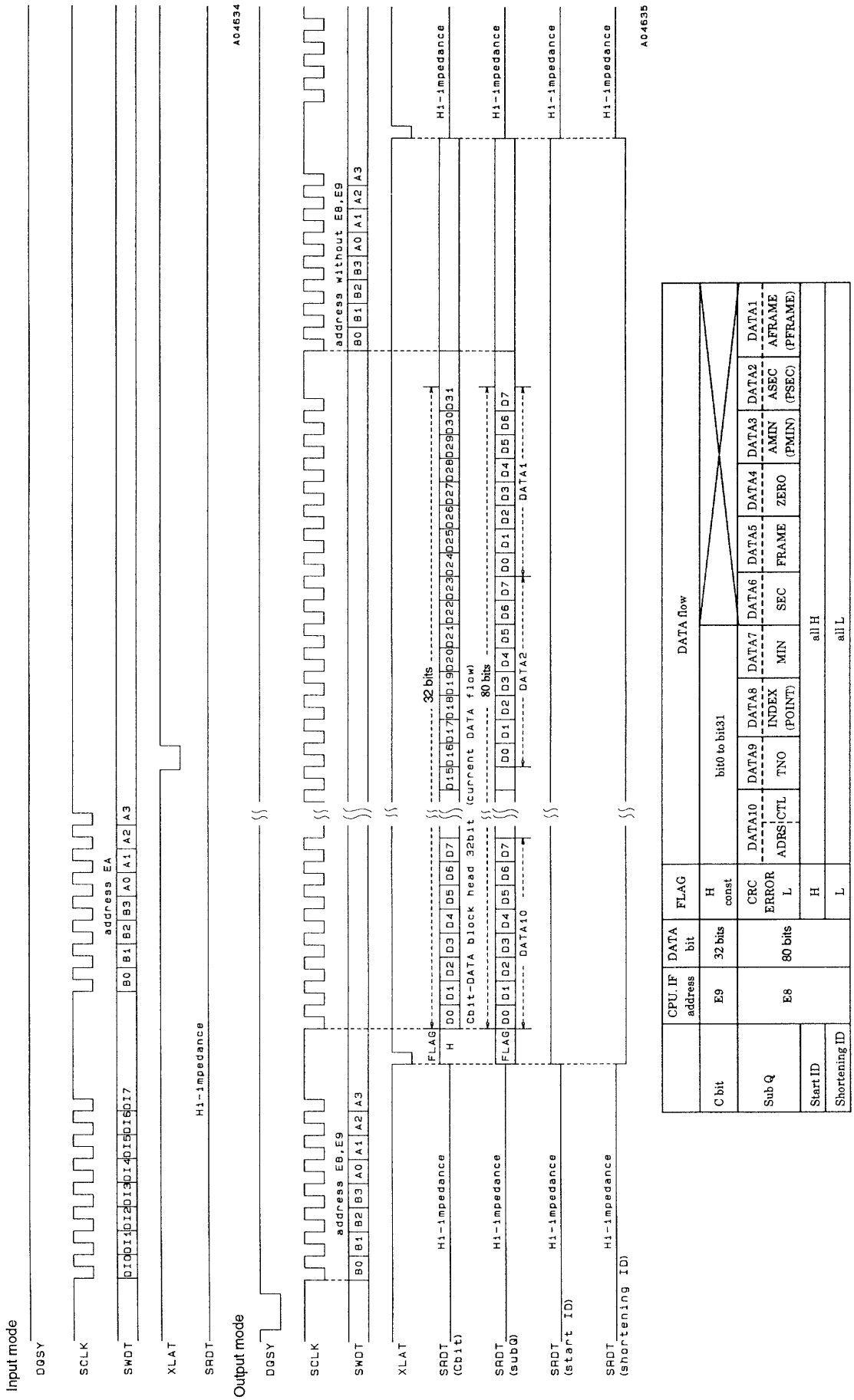


Figure 3 Microprocessor Interface Timing 2

Microprocessor Interface (SCLK/CL, XLAT/CE, SWDT/DI, SRDT/DO, DQSY/LD)

1. Data input and output addresses are allocated as follows:

Data input or output	Figure 2: Microprocessor Interface Timing 1									Figure 3: Microprocessor Interface Timing 2								
		B0	B1	B2	B3	A0	A1	A2	A3		B0	B1	B2	B3	A0	A1	A2	A3
Data input	F7	1	1	1	0	1	1	1	1	EA	0	1	0	1	0	1	1	1
C bit output	F8	0	0	0	1	1	1	1	1	E9	1	0	0	1	0	1	1	1
Subcode Q, ID output	F9	1	0	0	1	1	1	1	1	E8	0	0	0	1	0	1	1	1

2. The input command codes control the following settings:
   - System stop
   - Data input pin settings
   - Input bi-phase data output selection
   - Validity flag output selection
   - Audio data output format setting

   DI1: Stops VCO operation and thus stops the system.

DI1	L	H
System	Operating	Stopped

   DI2: Selects which input data to demodulate.

DI2	L	H
Data demodulation input	DIN1	DIN2

   DI3 and DI4: Select the E/DOUT pin output.

DI3	L		H	
DI4	L	H	L	H
E/DOUT	Emphasis data output	Validity flag output	DIN1 input data output	DIN2 input data output

   DI5 and DI6: Set the audio data output format.

DI5	L		H	
DI6	L	H	L	H
DATAOUT	16-bit right-justified MSB first	20-bit right-justified LSB first	20-bit right-justified MSB first	20-bit left-justified MSB first

   All bits are set low immediately after XMODE is switched from low to high. DI0 and DI7 are not used.

3. The following output settings can be controlled:
   - Channel status (C bit) output
   - Subcode Q data output
   - Status ID and shortening ID detection for DAT that use subcodes

   C bit output
   - This function presumes that this IC will be used in consumer mode and thus only handles the first 32 bits.
   - The flag is fixed at the high level (although there is no flag in the type 1 microprocessor interface timing), and the data format is LSB first.
   - Error and update checking is not applied to the data.
   - The internal shift register is reset if a PLL lock error occurs.
   - An interval of at least 6 msec must be provided between consecutive data readout operations.

   Subcode Q output
   - Subcode Q can be read out after the fall of the DQSY/LD signal. Also note that the data is updated every time this signal falls. However, this signal will not be output (fall) unless 96 bits of subcode Q data (include the CRC check bits) is input.
   - The flag outputs a high when the CRC check passes, and low if the CRC check fails.
   - The bit order is LSB first within each byte of the 80 bits of subcode Q data.

   ID detection
   - The start ID and shortening ID are only detected when the DAT category code (1100000L) is received.
   - These IDs are detected as follows:
     — A low pulse is output from DQSY/LD if a start ID (R_0) or a shortening ID (L_1) is detected following a sync signal (L_0).
     — After this signal, data can be read out from SRDT/DO by inputting the same address value as that used for subcode Q data to SWDT/DI.

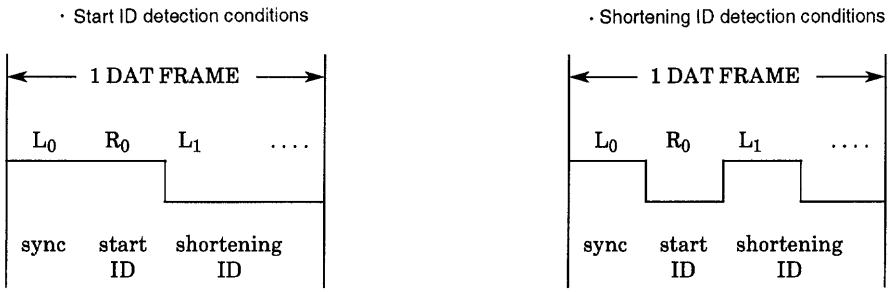


Figure 4 User Data for DAT that Use Subcodes

- The table below shows the relationship between the sync signal (L_0), the start ID (R_0), the shortening ID (L_1), and the data output.

(L_0): SYNC	H	H
(R_0): Start ID	H	L
(L_1): Shortening ID	L	H
Flags + 80 data bits	all H	all L
Detected ID	Start ID	Shortening ID

- Output pins
  The output scheme used for SRDT/DO differs depending on the microprocessor interface format selected by CKSEL.

CKSEL	Format	SRDT/DO
L	Figure 2	Open-drain output
H	Figure 3	Three-state output

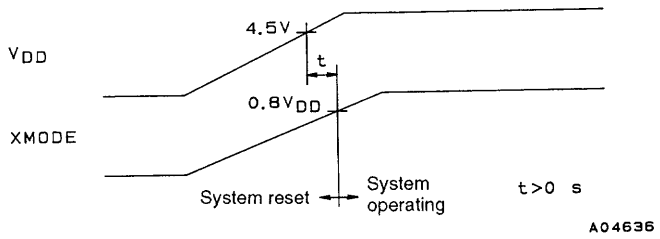
Error (ERROR)

The ERROR pin goes high if there is an error in the input data or if the PLL is unlocked. It holds the high level for about 200 to 300 msec after data demodulation returns to normal and then goes low. The table below lists the data processing when an error has occurred.

Type of error	DATAOUT	C bit	Sub Q	ID	E/DOUT
Up to 8 consecutive parity errors	Previous data value	Output	Output	Output	Output
Over 8 consecutive parity errors	L	Output	Output	Output	Output
PLL lock error	L	L	L	L	L

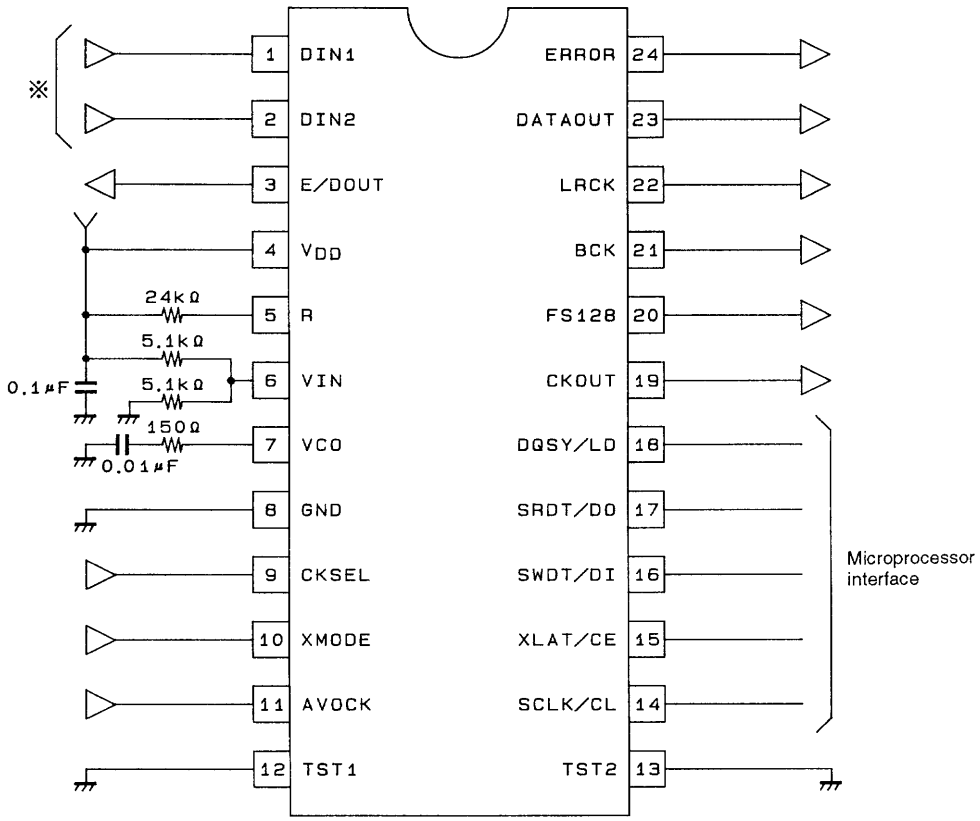
System Reset (XMODE)

Normal system operation is started by setting XMODE high after the power supply has risen above at least 4.5 V. If XMODE is set low, the VCO free-running oscillator clock is output from CKOUT.



Setting XMODE low once again after power on resets the system.

Sample Application Circuit



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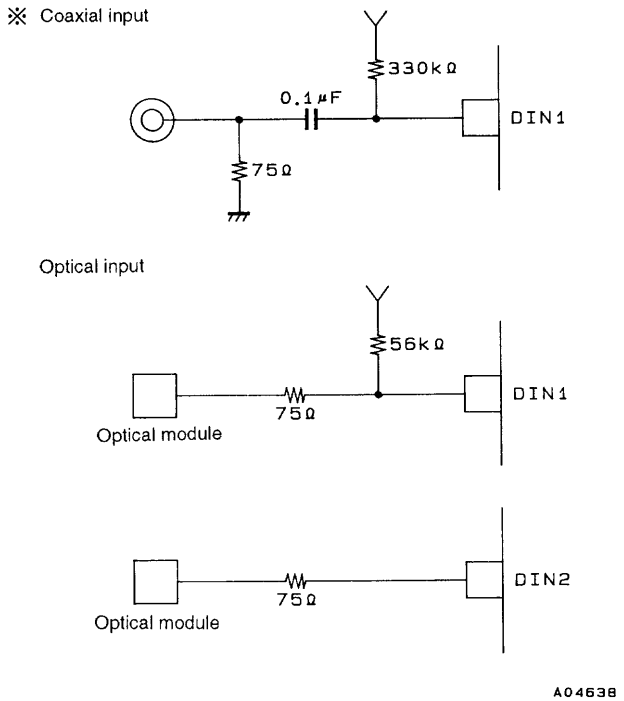

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