



# LC99012A-S

## Black-and-White CCD Timing Generator

### Preliminary

#### Overview

The LC99012A-S is a timing generator for the 1/5-inch LC9947G and LC9948G and the 1/6-inch LC9949G black-and-white CCD image sensors.

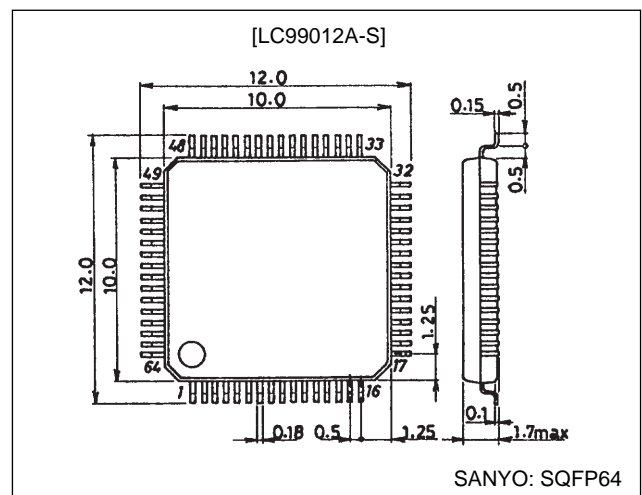
#### Features

- 5 V single-voltage power supply
- Generates all pulses required for CCD drivers.
- Generates all pulses required for video signal processing.
- Built-in synchronizing signal generator that supports both EIA and CCIR.
- Includes buffer circuits for directly driving the CCD horizontal transfer and reset gates.
- Includes light metering and control systems for an automatic electronic iris function.
- Fixed rate-of-change control allows a smooth electronic iris function to be implemented (an iris state output is provided).
- Supports AGC control and a light metering mode that compensates for backlighting.
- Selectable CCD storage mode (non-interlaced or interlaced)
- Selectable TV scan mode (non-interlaced or interlaced)
- Allows all types of external synchronization.
- Built-in EXT-C.SYNC sync separator circuit
- Built-in phase comparator for external synchronization
- Control from external electronic shutter pulses and frame shift pulses supports one-shot imaging.
- Package: 0.5 mm lead pitch flat package (SQFP-64)
- Flickerless function
- Sensitivity-increasing function

#### Package Dimensions

unit: mm

#### 3190-SQFP64



## Specifications

### Absolute Maximum Ratings at $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD\text{ max}}$		-0.3 to +7.0	V
Input and output voltages	$V_I, V_O$		-0.3 to $V_{DD} + 0.3$	V
Allowable power dissipation	$Pd\text{ max}$	$T_a \leq 65^\circ\text{C}$	290	mW
Operating temperature	$T_{opr}$		-30 to +65	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-55 to +125	$^\circ\text{C}$
Soldering heat resistance		Hand soldering: 3 seconds	350	$^\circ\text{C}$
		Reflow soldering: 10 seconds	235	$^\circ\text{C}$
Input and output currents	$I_I, I_O$		$\pm 20^*$	mA

Note: \* Per individual I/O reference cell

### Allowable Operating Ranges at $T_a = -30\text{ to }+65^\circ\text{C}$ , $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	$V_{DD}$		4.5	5.0	5.5	V
Input voltage range	$V_{IN}$		0		$V_{DD}$	V

### DC Characteristics: Input and Output Levels at $V_{SS} = 0\text{ V}$ , $V_{DD} = 4.5\text{ to }5.5\text{ V}$ , $T_a = -30\text{ to }+65^\circ\text{C}$

See the note on next page.

Parameter	Symbol	Conditions	min	typ	max	Unit
Input high-level voltage	$V_{IH1}$	TTL levels: (6)	2.2			V
Input low-level voltage	$V_{IL1}$	TTL levels: (6)			0.8	V
Input high-level voltage	$V_{IH2}$	CMOS levels: (1), (3)	$0.7 V_{DD}$			V
Input low-level voltage	$V_{IL2}$	CMOS levels: (1), (3)			$0.3 V_{DD}$	V
Input high-level voltage	$V_{IH3}$	CMOS levels, Schmitt inputs: (4)	$0.8 V_{DD}$			V
Input low-level voltage	$V_{IL3}$	CMOS levels, Schmitt inputs: (4)			$0.2 V_{DD}$	V
Input high-level voltage	$V_{IH4}$	CMOS levels, inputs with pull-up resistors: (2)	$0.7 V_{DD}$			V
Input low-level voltage	$V_{IL4}$	CMOS levels, inputs with pull-up resistors: (2)			$0.3 V_{DD}$	V
Input high-level voltage	$V_{IH5}$	CMOS levels, inputs with pull-up resistors: (5)	$0.7 V_{DD}$			V
Input low-level voltage	$V_{IL5}$	CMOS levels, inputs with pull-up resistors: (5)			$0.3 V_{DD}$	V
Output high-level voltage	$V_{OH1}$	$I_{OH} = -3\text{ mA}$ : (6), (13), (14), (15)	$V_{SS} - 2.1$			V
Output low-level voltage	$V_{OL1}$	$I_{OL} = 3\text{ mA}$ : (6), (13), (14), (15)			0.4	V
Output low-level voltage	$V_{OL2}$	$I_{OL} = 3\text{ mA}$ : (9)			0.4	V
Output high-level voltage	$V_{OH3}$	$I_{OH} = -6\text{ mA}$ : (12)	$V_{DD} - 2.1$			V
Output low-level voltage	$V_{OL3}$	$I_{OL} = 6\text{ mA}$ : (12)			0.4	V
Output high-level voltage	$V_{OH4}$	$I_{OH} = -6\text{ mA}$ : (7)	$V_{DD} - 2.1$			V
Output low-level voltage	$V_{OL4}$	$I_{OL} = 2\text{ mA}$ : (7)			0.4	V
Output high-level voltage	$V_{OH5}$	$I_{OH} = -30\text{ mA}$ : (11)	$V_{DD} - 2.1$			V
Output low-level voltage	$V_{OL5}$	$I_{OL} = 10\text{ mA}$ : (11)			0.4	V
Output high-level voltage	$V_{OH6}$	$I_{OH} = -12\text{ mA}$ : (8)	$V_{DD} - 2.1$			V
Output low-level voltage	$V_{OL6}$	$I_{OL} = 12\text{ mA}$ : (8)			0.4	V
Output high-level voltage	$V_{OH6}$	$I_{OH} = -12\text{ mA}$ : (10)	$V_{DD} - 1.5$			V
Output low-level voltage	$V_{OL7}$	$I_{OL} = 6\text{ mA}$ : (8)			0.4	V
Input leakage current	$I_{IL}$	$V_I = V_{SS}, V_{DD}$ : (1), (3), (4), (6)	-10		+10	$\mu\text{A}$
Output leakage current	$I_{OZ}$	In high-impedance output mode: (6), (9), (13)	-10		+10	$\mu\text{A}$
Pull-up resistance	$R_{UP}$	(2)	10	20	40	$\text{k}\Omega$
Pull-down resistance	$R_{DN}$	(5)	25	50	100	$\text{k}\Omega$

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Note: The applicable pin sets are defined as follows:

Input

- (1) .....AI, CKI
- (2) .....FLESS, STR, TEST
- (3) .....EXT1, EXT2, KISYU, TV
- (4) .....HR, SELMET1, SELMET2, VR
- (5) .....CCDSCAN, EXT3, EXT4, MSENS, SENS, SSGSCAN

I/O

- (6) .....STEPSTOP

Output

- (7) .....PCO
- (8) .....DHTR
- (9) .....IRRES
- (10) ....A0, CKO
- (11) ....DHT1, DHT2
- (12) ....DS1, DS2
- (13) ....AGCC2, IRSTA
- (14) ....CLK14M, CLP1, CLP2, FLD, HD, NSUB1, NSUB2, VD
- (15) ....CBLK, C.SYNC, NSUB3, PBLK, V11 to V14, VS1 to VS4

\* .....VIDI, VIDO, DCH, DCL, IRIS (These pins are not covered in the DC characteristics.)

### Pin Assignment

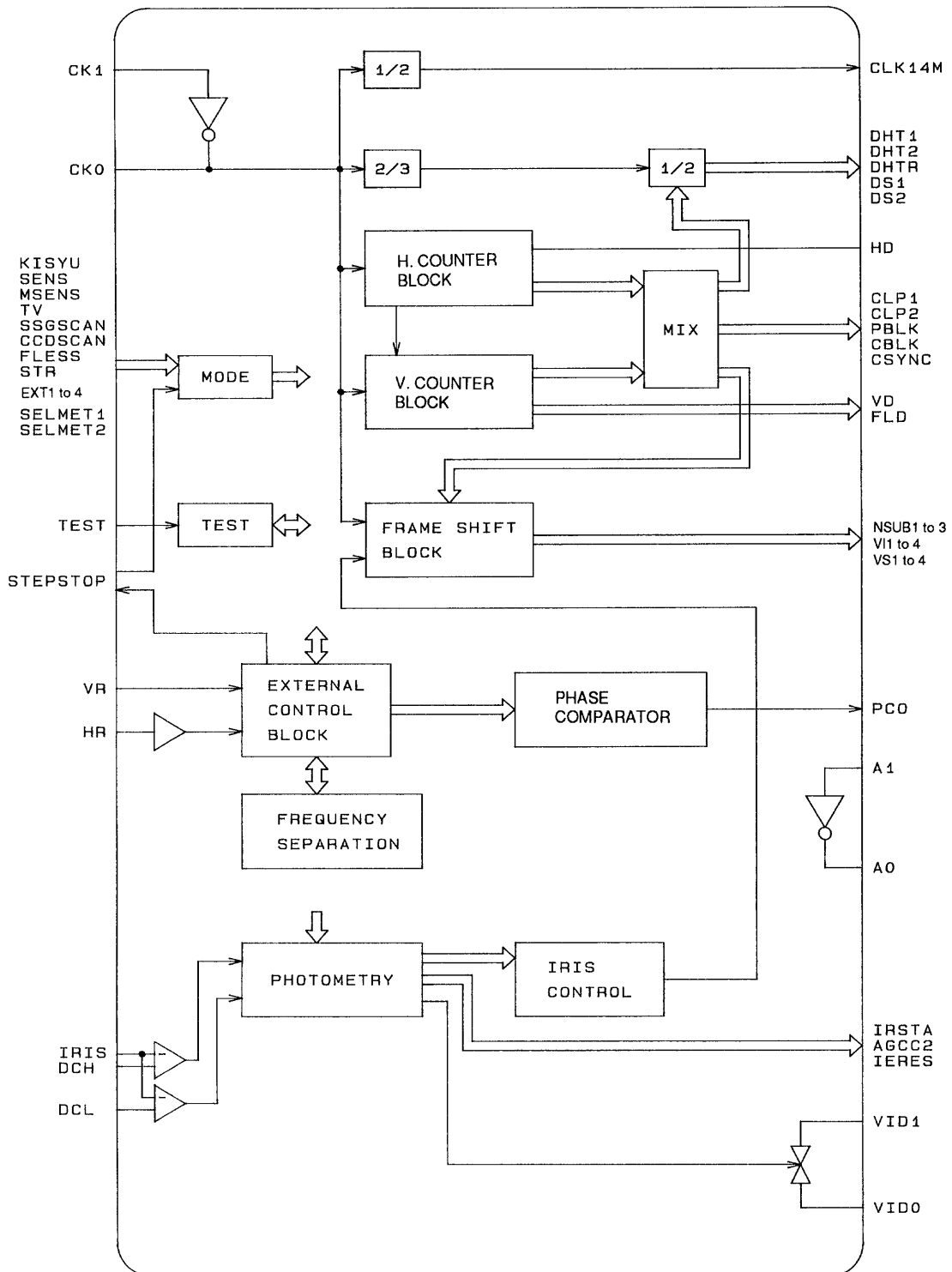
I/O → I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, NC: Unconnected pin

No.	Symbol	I/O	No.	Symbol	I/O
1	V <sub>SS</sub>	P	64	DCL	I
2	PCO	O	63	DCH	I
3	AI	I	62	IRIS	I
4	AO	O	61	IRRES	O
5	CKI	I	60	VIDO	O
6	CKO	O	59	VIDI	I
7	CCDSCAN	I	58	IRSTA	O
8	SSGSCAN	I	57	AGCC2	O
9	CLK14M	O	56	V <sub>DD</sub>	P
10	HD	O	55	TV	I
11	VD	O	54	C.SYNC	O
12	FLD	O	53	CBLK	O
13	V <sub>DD</sub>	P	52	PBLK	O
14	KISYU	I	51	CLP2	O
15	HR	I	50	CLP1	O
16	VR	I	49	V <sub>SS</sub>	P
17	V <sub>SS</sub>	P	48	DS1	O
18	SELMET1	I	47	DS2	O
19	SELMET2	I	46	V <sub>DD</sub>	P
20	EXT1	I	45	DHT2	O
21	EXT2	I	44	DHT1	O
22	EXT3	I	43	DHTR	O
23	EXT4	I	42	V <sub>SS</sub>	P
24	V <sub>DD</sub>	P	41	VS3	O
25	STEPSTOP	B	40	VS2	O
26	SENS	I	39	VS1	O
27	MSENS	I	38	VS4	O
28	FLESS	I	37	V14	O
29	STR	I	36	V12	O
30	NSUB3	O	35	V13	O
31	NSUB2	O	34	V11	O
32	NSUB1	O	33	TEST	I

Note: All V<sub>DD</sub> and V<sub>SS</sub> pins must be connected to the power supply or ground. Do not leave any of these pins open.

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Block Diagram



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### Pin Functions

Pin No.	Symbol	I/O	Function
1	GND		
2	PCO	O	Phase comparator output
3	AI	I	PCO output signal low-pass filter amplifier input
4	AO	O	PCO output signal low-pass filter amplifier output
5	CKI	I	Reference clock input (resonator inverter input) LC9947G: 28.63636 MHz LC9948G: 28.375 MHz LC9949G: 14.31818 MHz
6	CKO	O	Resonator inverter output
7	CCDSCAN	I	Low/open: CCD interlaced storage mode High: CCD non-interlaced storage mode
8	SSGSCAN	I	Low/open: C.SYNC interlaced mode High: C.SYNC non-interlaced mode
9	CLK14M	O	LC9947G/9949G: 14.31818 MHz LC9948G: 14.1875 MHz
10	HD	O	HD output
11	VD	O	VD output
12	FLD	O	Field identifier signal High: odd Low: even Must be tied high if SSGSCAN is high.
13	V <sub>DD</sub>		
14	KISYU	I	Must be tied high when used with the LC9949G. Otherwise must be tied low.
15	HR	I	Horizontal reset, C.SYNC reset, and vertical reset pulse input
16	VR	I	Vertical reset pulse input and external synchronization mode setup
17	GND		
18	SELMET1	I	Light metering mode control
19	SELMET2	I	Light metering mode control
20	EXT1	I	External synchronization mode control
21	EXT2	I	External synchronization mode control
22	EXT3	I	CCD drive external control mode control
23	EXT4	I	CCD drive external control mode control
24	V <sub>DD</sub>	I	
25	STEPSTOP	I/O	Normally used to control the electronic iris step (rate of change) Low: 1/8 High: 1/16
26	SENS	I	Sensitivity increasing switch Low/open: normal High: Increased sensitivity mode
27	MSENS	I	Increased sensitivity mode type switching Low or open: In field units High: In single scan line (1H) units
28	FLESS	I	Flickerless mode* switch Low: Flickerless mode High/open: normal
29	STR	I	CCD storage mode control This pin must be left open or tied high when the LC99012A-S is used with an LC9947G/49G, and must be tied low when used with an LC9948G.
30	NSUB3	O	CCD NSUB pulses
31	NSUB2	O	CCD NSUB pulses
32	NSUB1	O	CCD NSUB pulses
33	TEST	I	Low: test mode High/open: normal operating mode
34	VI1	O	CCD imaging block transfer clock (ø1)
35	VI3	O	CCD imaging block transfer clock (ø3)
36	VI2	O	CCD imaging block transfer clock (ø2)
37	VI4	O	CCD imaging block transfer clock (ø4)
38	VS4	O	CCD imaging block transfer clock (øS4)

Note: \* Flickerless mode can be used when the auto-iris function is off, i.e. when EXT3 is high and EXT4 is low.

Continued on next page.

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Pin No.	Symbol	I/O	Function
39	VS1	O	CCD imaging block transfer clock ( $\phi$ S1)
40	VS2	O	CCD imaging block transfer clock ( $\phi$ S2)
41	VS3	O	CCD imaging block transfer clock ( $\phi$ S3)
42	GND		
43	DHTR		CCD output block reset pulse
44	DHT1	O	CCD horizontal transfer clock ( $\phi$ H1)
45	DHT2	O	CCD horizontal transfer clock ( $\phi$ H2)
46	V <sub>DD</sub>		
47	DS2	O	CCD output floating level sampling pulse
48	DS1	O	CCD output video signal sampling pulse
49	GND		
50	CLP1	O	OPB clamp pulse 
51	CLP2	O	OPB clamp pulse 
52	PBLK	O	Pre-blanking pulse 
53	CBLK	O	Composite blanking pulse 
54	C.SYNC	O	Composite sync pulse 
55	TV	I	Low: EIA (LC9947G/49G) High: CCIR (LC9948G)
56	V <sub>DD</sub>		
57	AGCC2	O	AGC detection signal weighting processing pulse
58	IRSTA	O	Electronic iris state output High: The iris is in the fully stopped down state. Low: The iris is in the fully open state. High-impedance: The iris is in an appropriate state.
59	VIDI	I	Analog switch input for iris detection signal window processing
60	VIDO	O	Analog switch output for iris detection signal window processing
61	IRRES	O	Reset (discharge) pulse that is input by the iris signal detection (integration) circuit
62	IRIS	I	Iris integration signal input
63	DCH	I	High-level reference voltage for the iris level detection comparator
64	DCL	I	Low-level reference voltage for the iris level detection comparator

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