



# LC4608C

## Printer Head Driver

### Overview

The LC4608C is a driver for ink-jet printer heads with 64-bit output. It converts 4-bit parallel input into 16-step gray scale output by regulating the transmission gate's output time.

- 16-step gray scale output from 4-bit parallel input
- Built-in 64 × 2-channel transmission gate output
- Transmission gate on resistance of 60 Ω (typ.) 100 Ω (max)
- CMOS process with high withstand voltage (42 V)

### Features

This 64-bit CMOS driver with 16-step gray scale output and high withstand voltage offers the following features.

- Built-in 64 × 4-bit static shift register
- Built-in 64 × 4-bit static latch

### Specifications

#### Maximum Ratings

| Parameter  | Symbol    | Conditions                                  | Ratings                | Unit |
|--|-----------|---|------------------------|------|
| Supply voltage (logic)                           | $V_{DD}$  |   | -0.5 to +7.0           | V    |
| Supply voltage (high withstand voltage circuits) | $V_H$     |   | -0.5 to +42            | V    |
| Driver output breakdown voltage                  | $BV_{DO}$ |   | -0.5 to +42            | V    |
| Driver output current                            | $I_{DO}$  | Peak value within allowable operating range | ±400                   | mA   |
| Input current                                    | $I_{IN}$  |   | -20 to +20             | mA   |
| Input voltage (logic)                            | $V_{IN1}$ |   | -0.5 to $V_{DD} + 0.5$ | V    |
| Input voltage (COM, output)                      | $V_{IN2}$ |   | -0.5 to $V_H + 0.5$    | V    |
| Operating temperature                            | $T_{opr}$ |   | -10 to +90             | °C   |
| Storage temperature                              | $T_{stg}$ |   | -65 to +150            | °C   |
| Junction temperature                             | $T_j$     |   | -10 to +125            | °C   |

#### Allowable Operating Ranges at $V_{DD} = 5.0\text{ V} \pm 10\%$ , $T_{opr} = -10\text{ to }+90\text{ °C}$ unless otherwise specified

| Parameter          | Symbol     | Conditions             | Ratings |     |          | Unit |
|--------------------|------------|------------------------|---------|-----|----------|------|
|                    |            |                        | min     | typ | max      |      |
| Supply voltage     | $V_{DD}$   |                        | 4.5     | 5.0 | 5.5      | V    |
|                    | $V_H$      | *1                     | 24.0    |     | 40.0     | V    |
| Input voltage      | $V_{IN}$   |                        | 0       |     | $V_{DD}$ | V    |
|                    | COM        |                        | 0       |     | $V_H$    | V    |
| Output current DOn | $I_{DO}$   | $V_H = 40\text{ V}$ *2 |         | 200 | 400      | mA   |
| Clock frequency    | $f_{clk}$  |                        |         |     | 8.0      | MHz  |
| Data setup time    | $t_{ds}$   |                        | 40      |     |          | ns   |
| Data hold time     | $t_{dh}$   |                        | 40      |     |          | ns   |
| Latch setup time   | $t_{Ls}$   |                        | 140     |     |          | ns   |
| Clock pulse width  | $t_{wCLK}$ |                        | 50      |     |          | ns   |
| Latch pulse width  | $t_{wLAT}$ |                        | 80      |     |          | ns   |

Continued on next page.

## LC4608C

Continued from preceding page.

| Parameter                | Symbol     | Conditions | Ratings |     |     | Unit |
|--------------------------|------------|------------|---------|-----|-----|------|
|                          |            |            | min     | typ | max |      |
| STBCLK frequency         | $f_{STB}$  |            |         |     | 1.0 | MHz  |
| CLK → LOAD setup time    | $t_{SL}$   |            | 80      |     |     | ns   |
| LOAD → CLK hold time     | $t_{HL}$   |            | 80      |     |     | ns   |
| LOAD pulse width         | $t_{WL}$   |            | 80      |     |     | ns   |
| STBCLK → LOAD setup time | $t_{STBL}$ |            | 80      |     |     | ns   |
| LOAD → STBCLK hold time  | $t_{LSTB}$ |            | 80      |     |     | ns   |
| Clock rising edge time   | $t_r$      |            |         |     | 35  | ns   |
| Clock falling edge time  | $t_f$      |            |         |     | 35  | ns   |
| Latch rising edge time   | $t_{lr}$   |            |         |     | 70  | ns   |
| Latch falling edge time  | $t_{lf}$   |            |         |     | 70  | ns   |
| Operating temperature    | $T_{jopr}$ |            | -1.0    |     | +90 | °C   |

Note : 1. The figures for normal operation are a load capacitance Cpzt of 1 nF, a power supply voltage  $V_H$  of 30 V, and a max input level COMmax of 25 V.  
 2. Value for  $V_H = 40$  V, COMmax = 40 V, frequency = 35 kHz, and duty factor = 1/100.

### Electrical Characteristics

#### DC Characteristics at $V_{DD} = 5.0\text{ V} \pm 10\%$ , $T_{jopr} = -10$ to $+90^\circ\text{C}$ unless otherwise specified

| Parameter   | Symbol       | Conditions   | Ratings             |      |                     | Unit          |
|---|--------------|--|---------------------|------|---------------------|---------------|
|   |              |  | min                 | typ  | max                 |               |
| Input high-level voltage                            | $V_{IH}$     |  | $V_{DD} \times 0.7$ |      | $V_{DD} + 0.3$      | V             |
| Input low-level voltage                             | $V_{IL}$     |  | -0.3                |      | $V_{DD} \times 0.3$ | V             |
| Input high-level current *2                         | $-I_{IH1}$   | $V_{DD} = 5.0\text{ V}, V_{IH} = 5.0\text{ V}$   | 0                   |      | 0.5                 | $\mu\text{A}$ |
|   | $-I_{IH2}$   | $V_{DD} = 5.0\text{ V}, V_{IH} = 5.0\text{ V}$   | 0                   | 50   | 100                 | $\mu\text{A}$ |
| Input low-level current *3                          | $I_{IL}$     | $V_{DD} = 5.0\text{ V}$  | 0                   |      | 0.5                 | $\mu\text{A}$ |
| Output high-level voltage                           | $V_{OH}$     | $I_O = -400\ \mu\text{A}$  | $V_{DD} - 0.5$      |      |                     | V             |
| Output low-level voltage                            | $V_{OL}$     | $I_O = 400\ \mu\text{A}$   |                     |      | 0.5                 | V             |
| Output high-level current transmission gate voltage | $V_{OHT}$    | $V_{DD} = 5.0\text{ V}, V_H = 40\text{ V}, \text{COMn} = 40\text{ V}, I_{OHT} = 10\text{ mA}$  | 39                  | 39.4 |                     | V             |
| Output low-level current transmission gate voltage  | $V_{OLT}$    | $V_{DD} = 5.0\text{ V}, V_H = 40\text{ V}, \text{COMn} = 40\text{ V}, -I_{OHT} = 10\text{ mA}$ |                     | 0.6  | 1.0                 | V             |
| Transmission gate on resistance                     | $R_{ON}$     | $V_H = 40\text{ V}, V_{DS} = 3\text{ V}$   |                     | 60   | 100                 | $\Omega$      |
| Transmission gate on resistance variation           | $R_x$        | Within chip<br>$\frac{2(\text{MAX} - \text{MIN}) \times 100}{\text{MAX} + \text{MIN}}$         | -15                 |      | +15                 | $\Omega$      |
| Current drain                                       | $I_{DD1}$    | $V_{DD} - \text{GND}, \text{fclk} = 3.5\text{ MHz}, \text{fslin} = 1.75\text{ MHz}$            | -15                 |      | +15                 | $\Omega$      |
| Leakage current between pins                        | $\pm I_{NL}$ | Leakage current between pins   | 0                   |      | 10                  | $\mu\text{A}$ |
| Output leakage current                              | $I_{LEAK}$   | $V_{DD} = 5.0\text{ V}, V_H = 42\text{ V}$   | 0                   |      | 100                 | $\mu\text{A}$ |

Note : 1. The sign is negative for incoming current and positive for outgoing current.

2.  $-I_{IH1}$  applies to the following input pins: SI0 to SI3, CLK, LAT, LOAD, STBCLK, and STB1 to STB3.  $-I_{IH}$  applies to the following input pins: STB4 and STB5.
3.  $I_{IL1}$  applies to the following input pins: SI0 to SI3, CLK, LAT, LOAD, STBCLK, and STB1 to STB5.

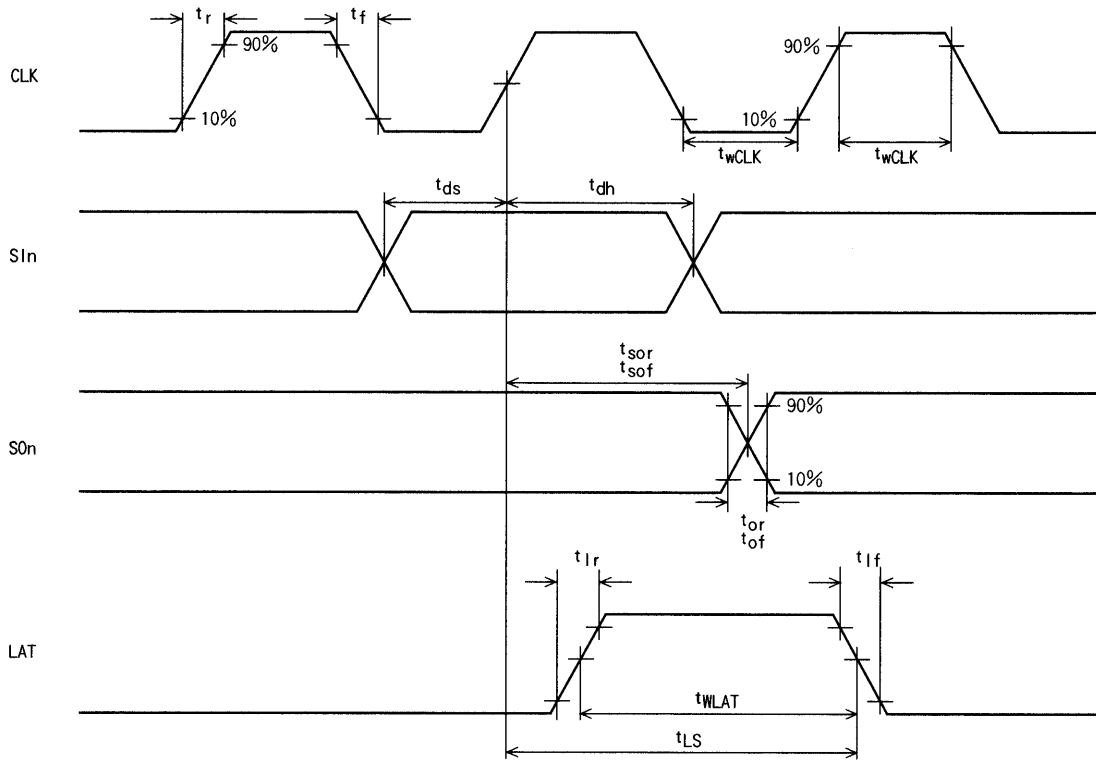
#### Switching Characteristics at $V_{DD} = 5.0\text{ V} \pm 10\%$ , $T_{jopr} = -10$ to $+90^\circ\text{C}$ unless otherwise specified

| Parameter                         | Symbol    | Conditions           | Ratings |     |     | Unit          |
|-----------------------------------|-----------|----------------------|---------|-----|-----|---------------|
|                                   |           |                      | min     | typ | max |               |
| SOn output rising edge time       | $t_{or}$  | $C_L = 10\text{ pF}$ |         |     | 50  | ns            |
| SOn input rising edge time        | $t_{of}$  | $C_L = 10\text{ pF}$ |         |     | 50  | ns            |
| STBn → DOn propagation delay time | $t_{dor}$ | *5                   |         |     | 1.0 | $\mu\text{s}$ |
|                                   | $t_{dof}$ | *5                   |         |     | 1.0 | $\mu\text{s}$ |
| CLK → SOn propagation delay time  | $t_{sor}$ | $C_L = 10\text{ pF}$ |         |     | 140 | ns            |
|                                   | $t_{sof}$ | $C_L = 10\text{ pF}$ |         |     | 140 | ns            |

Note : 5. The figures are for a load capacitance Cpzt of 1 nF and a power supply voltage  $V_H$  of 30 V as measured with  $R_L = 3\text{ k}\Omega$  and COMn = 25 V DC.

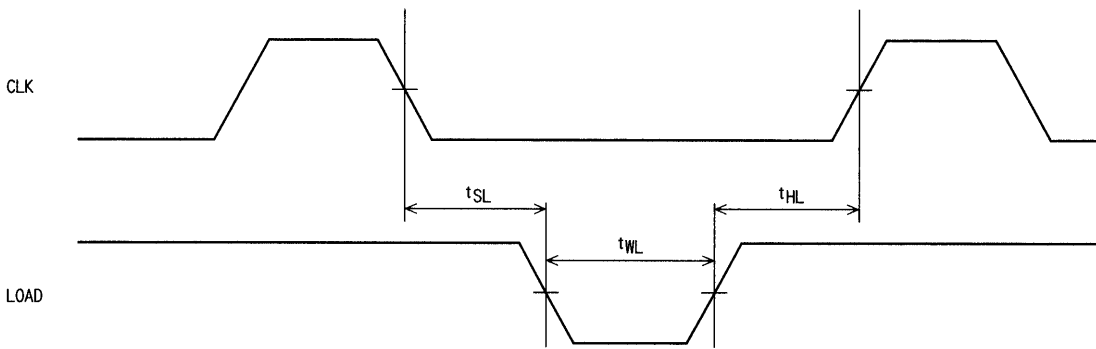
LC4608C

Timing Chart 1



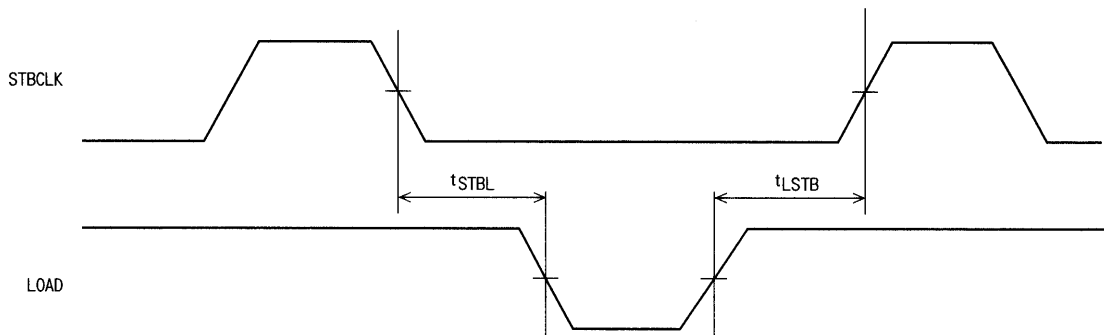
A09833

Timing Chart 2



A09834

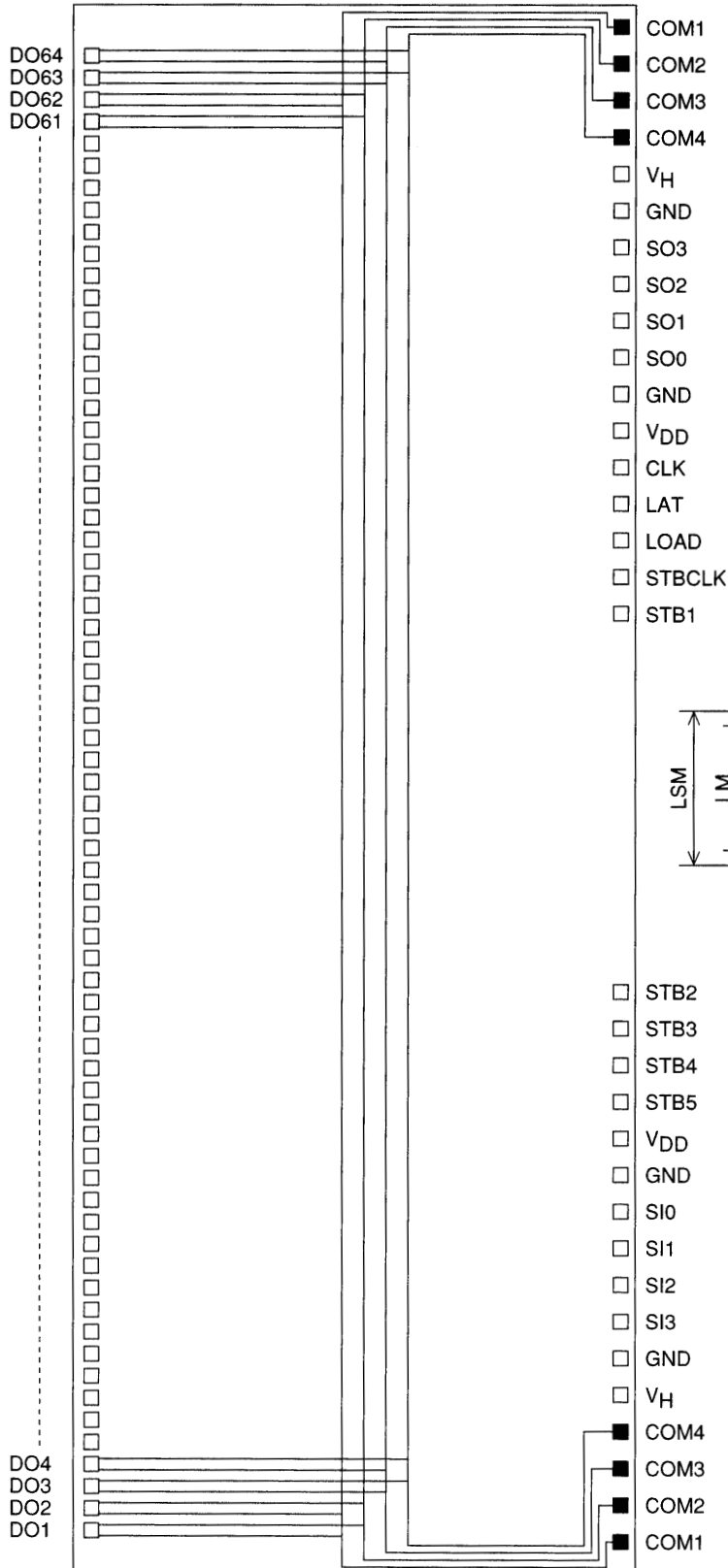
Timing Chart 3



A09835

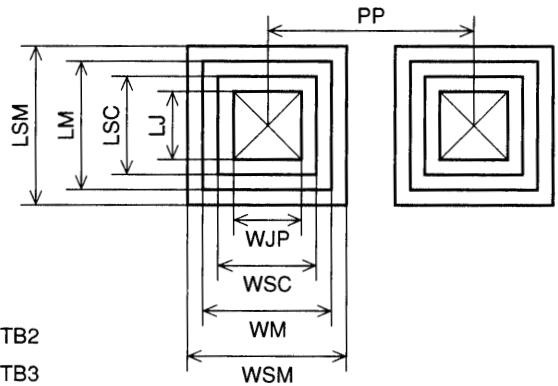


Pad Layout Diagram

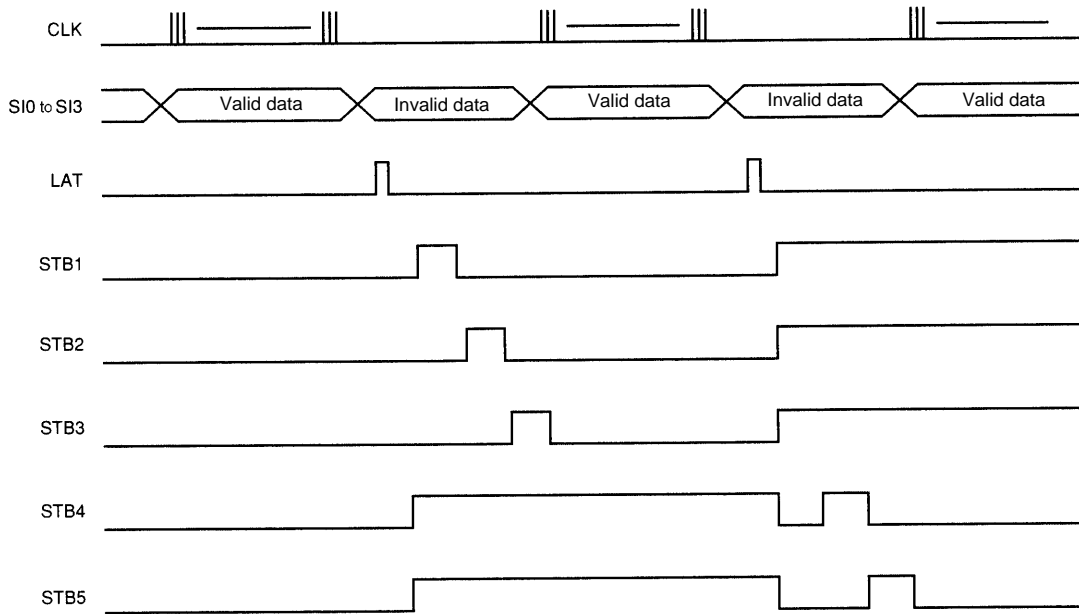


Chip size  
2.67 mm × 9.48 mm

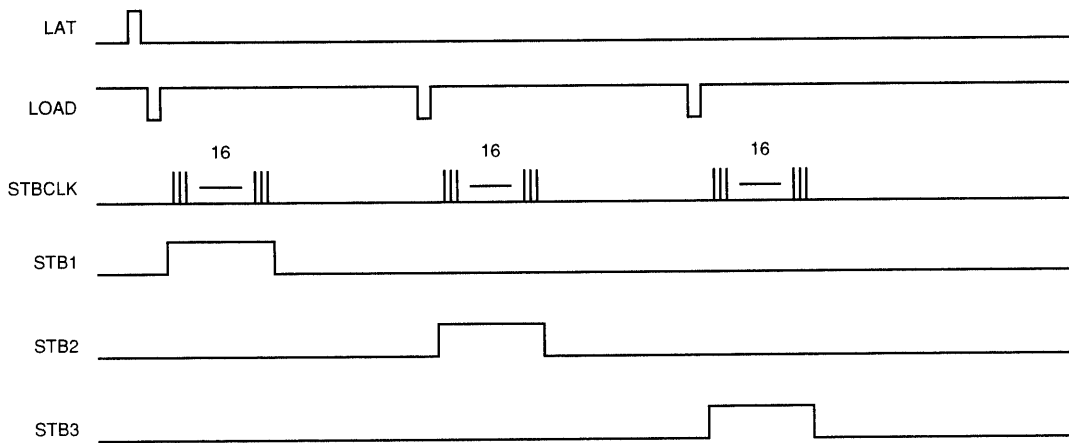
|                       |          |        |
|-----------------------|----------|--------|
| Output pad dimensions | PP       | 140 μm |
|                       | WSM, LSM | 116 μm |
|                       | WM, LM   | 106 μm |
|                       | WSC, LSC | 96 μm  |
|                       | WJP, LJ  | 90 μm  |
| Input pad dimensions  | PP (min) | 200 μm |
|                       | WSM, LSM | 116 μm |
|                       | WM, LM   | 106 μm |
|                       | WSC, LSC | 96 μm  |
|                       | WJP, LJ  | 90 μm  |



Signal sequence



A09839



A09840

## LC4608C

### Pad Functions

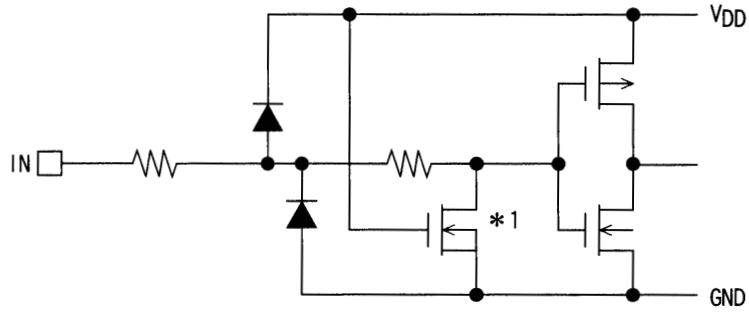
| Pad Name        | I/O | Function   | Pin Count |
|-----------------|-----|--|-----------|
| CLK             | I   | Shift register clock input   | 1         |
| SI0 to SI3      | I   | Shift register serial data input. SI0 is the least significant bit of the gray scale data; SI3, the most significant bit.  | 4         |
| LAT             | I   | Parallel output latch input. high level input converts serial data to parallel data; low level latches the data.   | 1         |
| STB1, 2, 3      | I   | 3-phase selector inputs. high level input turns on the corresponding output. STB1 controls output bits DO1, DO4, DO7, DO10,... DO62. STB2 controls output bits DO2, DO5, DO8, DO11,... DO63. STB3 controls output bits DO3, DO6, DO9, DO12,... DO64. | 3         |
| STB4, 5         | I   | 2-phase selector inputs with pull-down register. high level input turns on the corresponding output. STB4 controls the odd bits: DO1, DO3, DO5,... DO63. STB5 controls the even bits: DO2, DO4, DO6,... DO64.  | 2         |
| STBCLK          | I   | External clock signal input for gray scale signal generator  | 1         |
| LOAD            | I   | Reset input for 4-bit counter. low level input resets the counter to "0."  | 1         |
| COM1            | I   | Scan voltage signal input, latched when the shift register bit is "1" (DO pin pairs 1, 2, 5, 6,... 57, 58, 61, 62)   | 2         |
| COM2            | I   | Scan voltage signal input, latched when the shift register bit is "0" (DO pin pairs 1, 2, 5, 6,... 57, 58, 61, 62)   | 2         |
| COM3            | I   | Scan voltage signal input, latched when the shift register bit is "1" (DO pin pairs 3, 4, 7, 8,... 59, 60, 63, 64)   | 2         |
| COM4            | I   | Scan voltage signal input, latched when the shift register bit is "0" (DO pin pairs 3, 4, 7, 8,... 59, 60, 63, 64)   | 2         |
| SO0 to SO3      | O   | Shift register serial data output. SO0 is the least significant bit of the gray scale data; SO3, the most significant bit.   | 4         |
| DO1 to DO64     | O   | Parallel data output. Transmission gate output.  | 64        |
| V <sub>DD</sub> | —   | Power supply for logic circuits (+5 V)   | 2         |
| GND             | —   | Ground for logic and level conversion circuits   | 4         |
| V <sub>H</sub>  | —   | Power supply for level conversion circuits +40 V   | 2         |

**I/O Circuits**

- Logic circuit inputs

Pins: SI0 to SI3, CLK, LAT, STB1 to STB3, STBCLK, LOAD

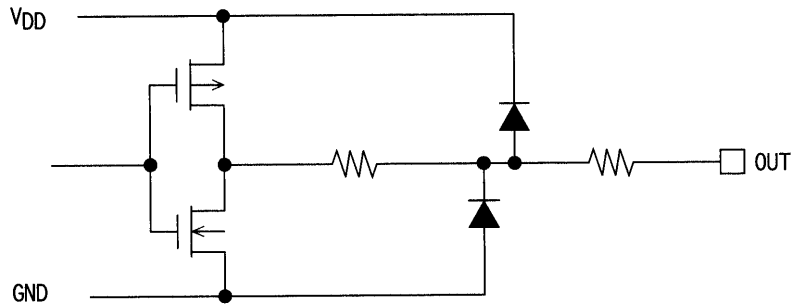
The pull-down resistor \*1 is only available for STB4 and STB5.



A09841

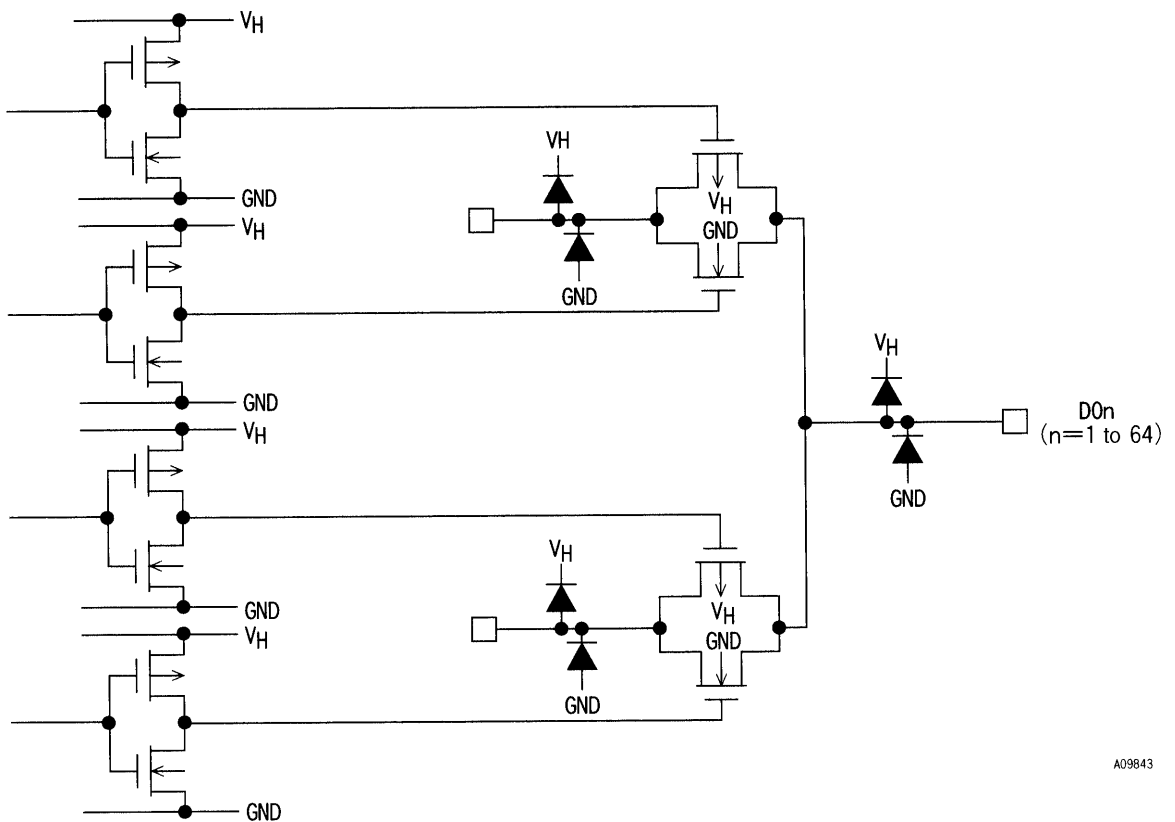
- Logic circuit outputs

Pins: SO0 to SO3



A09842

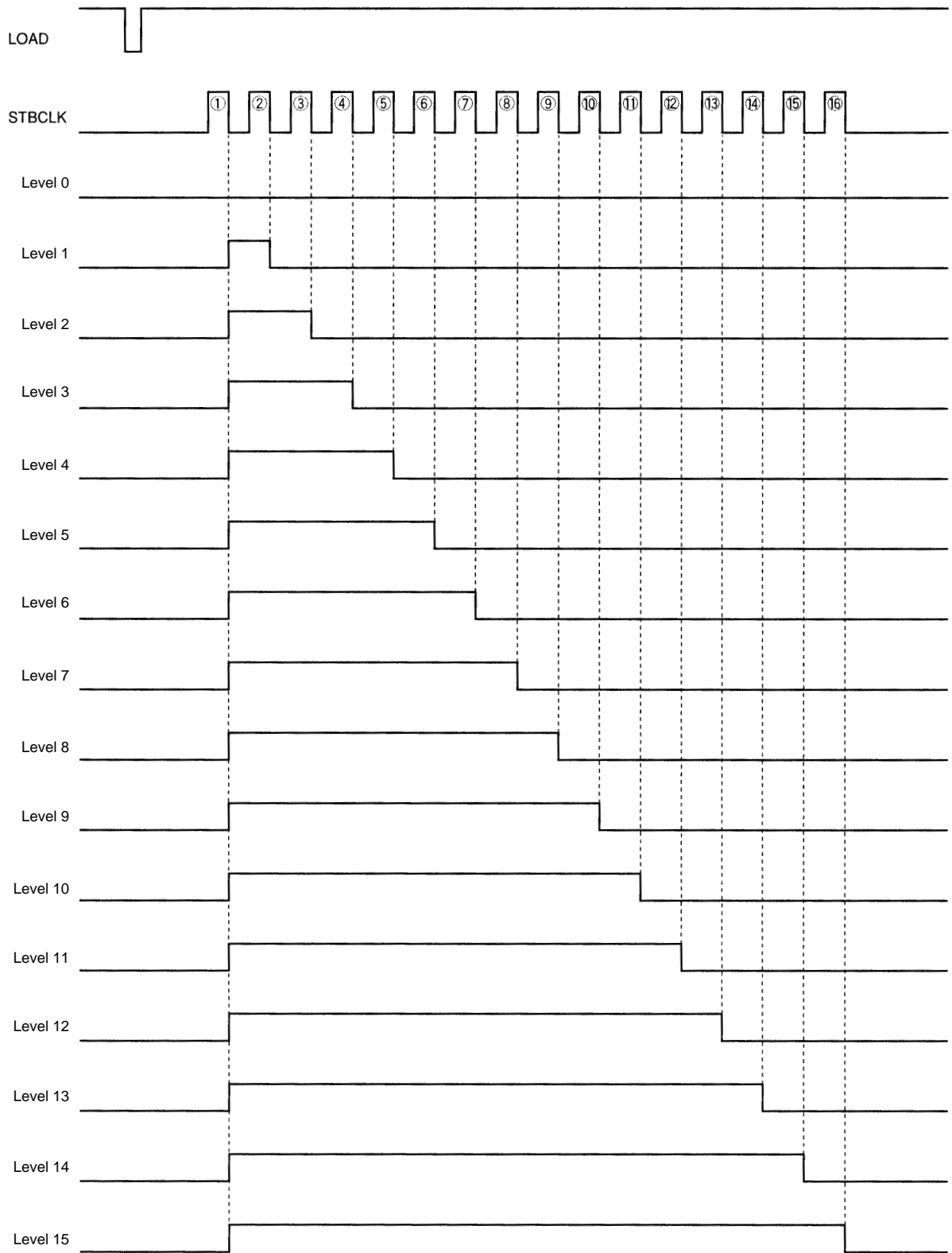
- DOn outputs



A09843



Gray Scale Timing Chart



The rising edge is synchronized with the STBCLK falling edge.

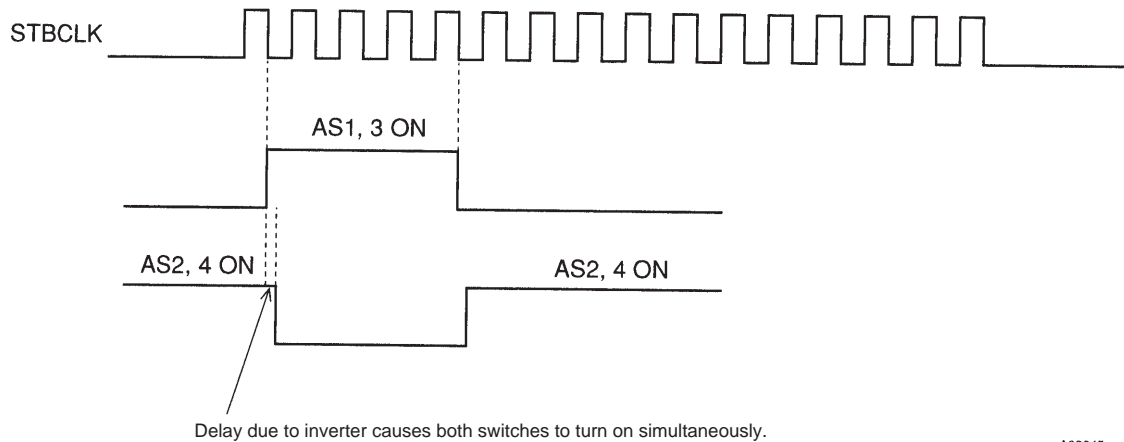
A09844

## LC4608C

### Pad Coordinates

| Pin Name | x-Coordinate | y-Coordinate | Pin Name        | x-Coordinate | y-Coordinate |
|----------|--------------|--------------|-----------------|--------------|--------------|
| DO1      | -4410.0      | 1162.0       | DO50            | 2450.0       | 1162.0       |
| DO2      | -4270.0      | 1162.0       | DO51            | 2590.0       | 1162.0       |
| DO3      | -4130.0      | 1162.0       | DO52            | 2730.0       | 1162.0       |
| DO4      | -3990.0      | 1162.0       | DO53            | 2870.0       | 1162.0       |
| DO5      | -3850.0      | 1162.0       | DO54            | 3010.0       | 1162.0       |
| DO6      | -3710.0      | 1162.0       | DO55            | 3150.0       | 1162.0       |
| DO7      | -3570.0      | 1162.0       | DO56            | 3290.0       | 1162.0       |
| DO8      | -3430.0      | 1162.0       | DO57            | 3430.0       | 1162.0       |
| DO9      | -3290.0      | 1162.0       | DO58            | 3570.0       | 1162.0       |
| DO10     | -3150.0      | 1162.0       | DO59            | 3710.0       | 1162.0       |
| DO11     | -3010.0      | 1162.0       | DO60            | 3850.0       | 1162.0       |
| DO12     | -2870.0      | 1162.0       | DO61            | 3990.0       | 1162.0       |
| DO13     | -2730.0      | 1162.0       | DO62            | 4130.0       | 1162.0       |
| DO14     | -2590.0      | 1162.0       | DO63            | 4270.0       | 1162.0       |
| DO15     | -2450.0      | 1162.0       | DO64            | 4410.0       | 1162.0       |
| DO16     | -2310.0      | 1162.0       | COM1            | -4567.0      | -1162.0      |
| DO17     | -2170.0      | 1162.0       | COM2            | -4367.0      | -1162.0      |
| DO18     | -2030.0      | 1162.0       | COM3            | -4167.0      | -1162.0      |
| DO19     | -1890.0      | 1162.0       | COM4            | -3967.0      | -1162.0      |
| DO20     | -1750.0      | 1162.0       | V <sub>H</sub>  | -3730.0      | -1162.0      |
| DO21     | -1610.0      | 1162.0       | GND             | -3457.8      | -1162.0      |
| DO22     | -1470.0      | 1162.0       | SI3             | -3255.8      | -1162.0      |
| DO23     | -1330.0      | 1162.0       | SI2             | -3019.8      | -1162.0      |
| DO24     | -1190.0      | 1162.0       | SI1             | -2755.8      | -1162.0      |
| DO25     | -1050.0      | 1162.0       | SI0             | -2519.8      | -1162.0      |
| DO26     | -910.0       | 1162.0       | GND             | -2215.8      | -1162.0      |
| DO27     | -770.0       | 1162.0       | V <sub>DD</sub> | -1993.4      | -1162.0      |
| DO28     | -630.0       | 1162.0       | STB5            | -1791.4      | -1162.0      |
| DO29     | -490.0       | 1162.0       | STB4            | -1555.4      | -1162.0      |
| DO30     | -350.0       | 1162.0       | STB3            | -1291.4      | -1162.0      |
| DO31     | -210.0       | 1162.0       | STB2            | -1055.4      | -1162.0      |
| DO32     | -70.0        | 1162.0       | STB1            | 802.4        | -1162.0      |
| DO33     | 70.0         | 1162.0       | STBCLK          | 1038.4       | -1162.0      |
| DO34     | 210.0        | 1162.0       | LOAD            | 1302.4       | -1162.0      |
| DO35     | 350.0        | 1162.0       | LAT             | 1538.4       | -1162.0      |
| DO36     | 490.0        | 1162.0       | CLK             | 1802.4       | -1162.0      |
| DO37     | 630.0        | 1162.0       | V <sub>DD</sub> | 1990.4       | -1162.0      |
| DO38     | 770.0        | 1162.0       | GND             | 2212.8       | -1162.0      |
| DO39     | 910.0        | 1162.0       | SO0             | 2516.8       | -1162.0      |
| DO40     | 1050.0       | 1162.0       | SO1             | 2752.8       | -1162.0      |
| DO41     | 1190.0       | 1162.0       | SO2             | 3016.8       | -1162.0      |
| DO42     | 1330.0       | 1162.0       | SO3             | 3252.8       | -1162.0      |
| DO43     | 1470.0       | 1162.0       | GND             | 3454.8       | -1162.0      |
| DO44     | 1610.0       | 1162.0       | V <sub>H</sub>  | 3727.8       | -1162.0      |
| DO45     | 1750.0       | 1162.0       | COM4            | 3967.8       | -1162.0      |
| DO46     | 1890.0       | 1162.0       | COM3            | 4167.0       | -1162.0      |
| DO47     | 2030.0       | 1162.0       | COM2            | 4367.0       | -1162.0      |
| DO48     | 2170.0       | 1162.0       | COM1            | 4567.0       | -1162.0      |
| DO49     | 2310.0       | 1162.0       |                 |              |              |

Note: The coordinate system places the origin at the chip center, the output pads across the top, and the input pads across the bottom.

**Note on COMn Input (Example: input data = 0100)**

A09845

Because the chip turns the output analog switches on in pairs using the timing shown above, make sure that there are no potential differences between the pairs COM1-COM2 and COM3-COM4.

- No products described or contained herein are intended for use in surgical implants, life-support systems, aerospace equipment, nuclear power control systems, vehicles, disaster/crime-prevention equipment and the like, the failure of which may directly or indirectly cause injury, death or property loss.
- Anyone purchasing any products described or contained herein for an above-mentioned use shall:
  - ① Accept full responsibility and indemnify and defend SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors and all their officers and employees, jointly and severally, against any and all claims and litigation and all damages, cost and expenses associated with such use:
  - ② Not impose any responsibility for any fault or negligence which may be cited in any such claim or litigation on SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors or any of their officers and employees jointly or severally.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of March, 1998. Specifications and information herein are subject to change without notice.