Ordering number : EN5760

CMOS IC

LC7535M

Electronic Volume/Loudness Control with Serial Data Control and High Voltage-Handling Capacity

Overview

The LC7535M is an electronic volume and loudness control IC that provides volume, balance, and loudness functions with a minimal number of external components and that can be controlled electronically.

Functions

- Volume: Provides 81 positions from 0 dB to –79 dB in 1-dB steps and –∞. A balance function can be implemented by controlling the left and right volume levels independently.
- Loudness: A loudness function can be implemented by attaching external capacitors at the output tap provided at the –20-dB position in the 5-dB step volume control.
- S (select) pin: Up to two LC7535M chips can be used on the same bus.
- Serial data input: The LC7535M supports communication with the controller in the CCB format.

- **CCB is a trademark of SANYO ELECTRIC CO., LTD.**
- **CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.**

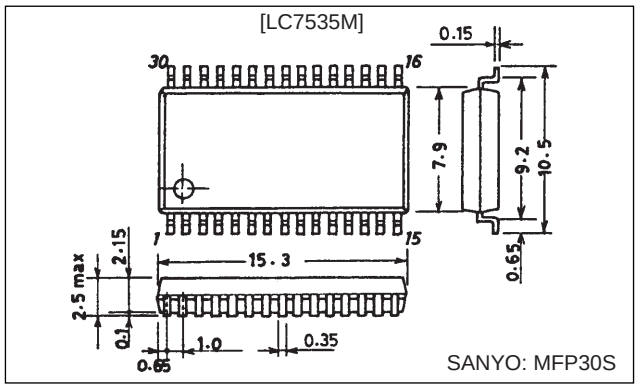
Feature

- High voltage-handling capacity: ±16 V.

Package Dimensions

unit: mm

3216A-MFP30S



Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	$V_{EE} \le V_{SS} < V_{CC} < V_{DD}$	V_{SS} to V_{SS} + 18	V
	V_{EE} max	$V_{EE} \le V_{SS} < V_{CC} < V_{DD}$	V_{SS} – 18 to V_{SS}	V
	V_{CC} max	$V_{EE} \le V_{SS} < V_{CC} < V_{DD}$	V_{SS} to V_{SS} + 7	V
Maximum input voltage	V_{IN} max1	CL, DI, CE	0 to V_{CC} + 0.3	V
	V_{IN} max2	L5dBIN, R5dBIN, L1dBIN, R1dBIN	V_{EE} – 0.3 to V_{DD} + 0.3	V
	V_{IN} max3	S	V_{CC} – 0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max	Ta ≤ 75°C	250	mW
Operating temperature	Topr		–30 to +75	°C
Storage temperature	Tstg		–40 to +125	°C

Allowable Operating Ranges at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}	V_{DD}	V_{CC} + 4.5		16	V
	V_{EE}	V_{EE}	–16		0	V
	V_{CC}	V_{CC}	4.5	5	5.5	V
Input high-level voltage	$V_{IH}1$	CL, DI, CE	0.8 V_{CC}		V_{CC}	V
	$V_{IH}2$	S	0.8 × (V_{DD} – V_{CC}) + V_{CC}		V_{DD}	V
Input low-level voltage	$V_{IL}1$	CL, DI, CE	V_{SS}		0.2 V_{CC}	V
	$V_{IL}2$	S	V_{CC}		0.2 × (V_{DD} – V_{CC}) + V_{CC}	V

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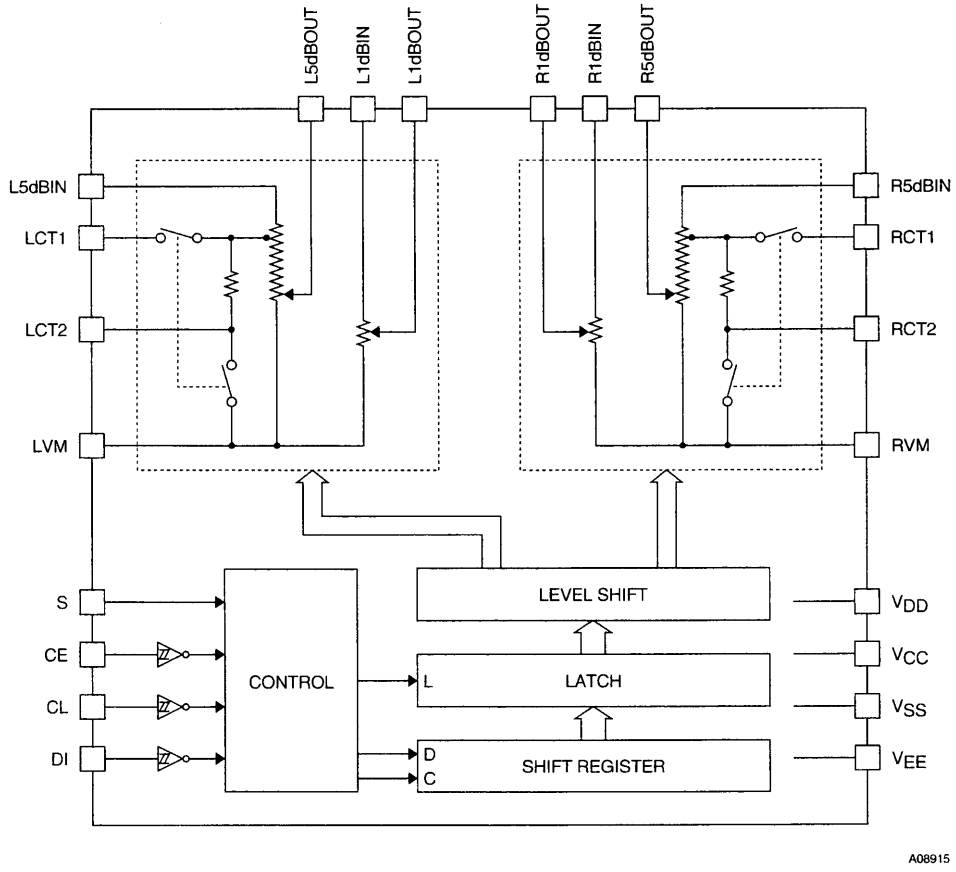
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input voltage amplitude	V_{IN}	L5dBIN, R5dBIN, L1dBIN, R1dBIN	V_{EE}		V_{DD}	Vp-p
Input pulse width	$t_{øw}$	CL	1			µs
Setup time	$t_{set\ up}$	CL, DI, CE	1			µs
Hold time	t_{hold}	CL, DI, CE	1			µs
Operating frequency	t_{opg}	CL			500	kHz

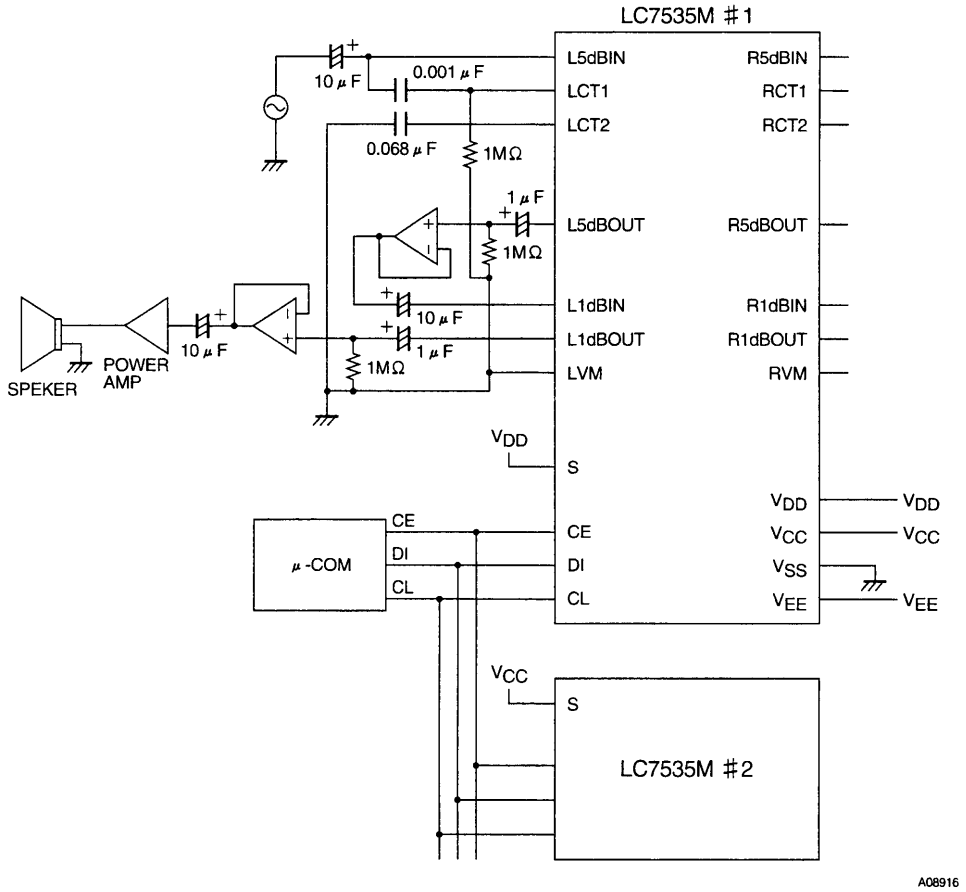
Electrical Characteristics at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Total harmonic distortion	THD	V_{IN} = 1 Vrms, f = 1 kHz, With all tone control settings flat, $V_{DD} - V_{EE}$ = 30 V		0.002		%
Crosstalk	C_T	V_{IN} = 1 Vrms, f = 1 kHz, With all tone control settings flat, RG = 1 kΩ, $V_{DD} - V_{EE}$ = 30 V		70		dB
Output at maximum attenuation	V_{Omin}	V_{IN} = 1 V rms, f = 1 kHz, with the volume set at –∞, $V_{DD} - V_{EE}$ = 30 V		–95		dB
Output noise voltage	V_N	With all tone control settings flat, Rg = 1 kΩ IHF-A, $V_{DD} - V_{EE}$ = 30 V		2	10	µV
Total resistance	Rvol1	5-dB volume control block		75		kΩ
	Rvol2	1-dB volume control block		20		kΩ
Output off leakage current	I_{OFF}	L5dBIN, R5dBIN, LCT1, RCT1, LCT2, RCT2, L5dBOUT, R5dBOUT, L1dBIN, R1dBIN, L1dBOUT, R1dBOUT, LVM, RVM	–10		+10	µA
Input high-level current	I_{IH}	CL, DI, CE : $V_{IN} = V_{CC}$			10	µA
Input low-level current	I_{IL}	CL, DI, CE : $V_{IN} = V_{SS}$	–10			µA
Current drain	I_{DD}	V_{DD} = 16 V			1	mA
	I_{CC}	V_{CC} = 5.5 V			1	mA

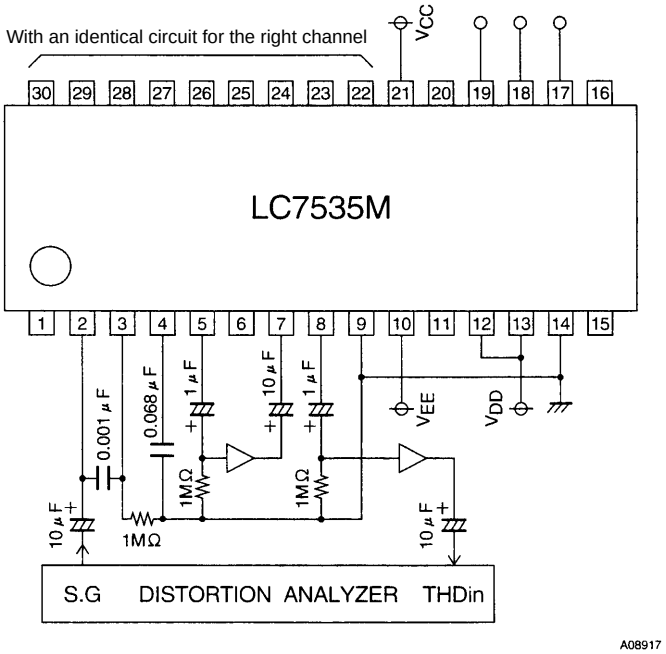
Equivalent Circuit



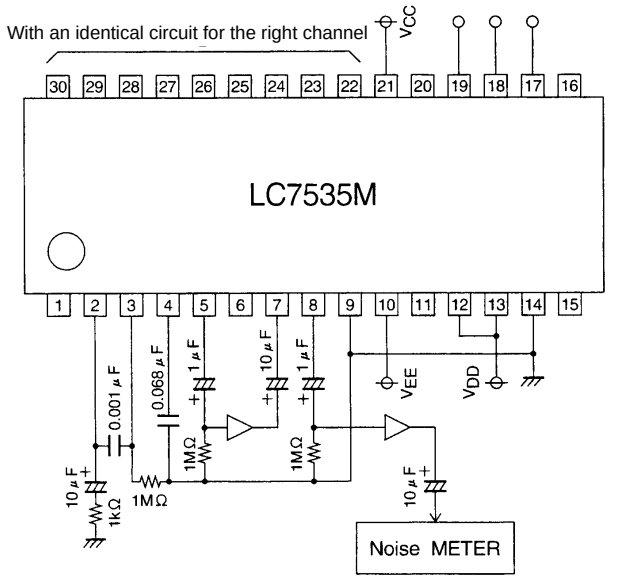
Sample Application Circuit



Test Circuit
Total Harmonic Distortion



Output Noise Voltage



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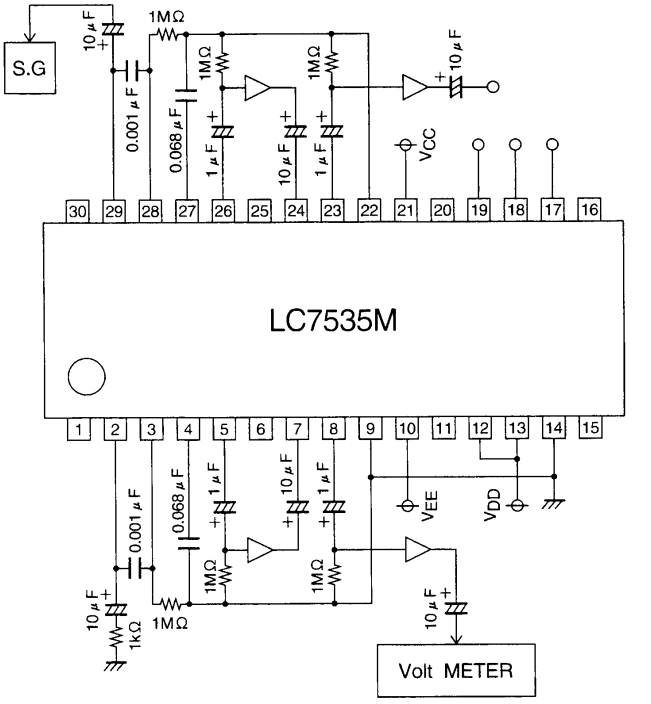
Crosstalk



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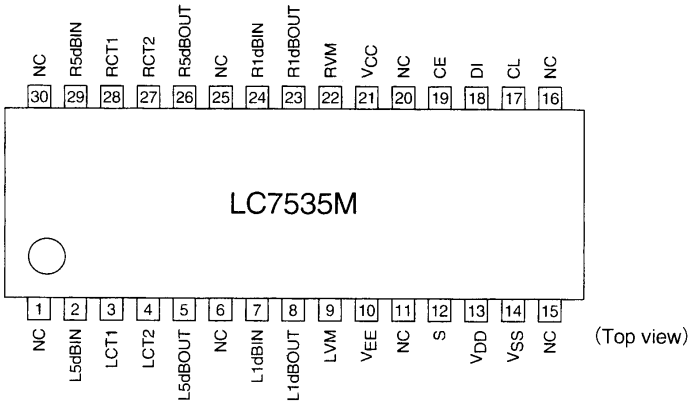
Pin Assignment



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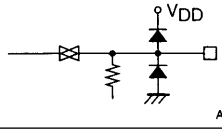
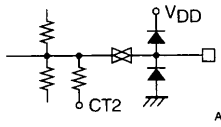
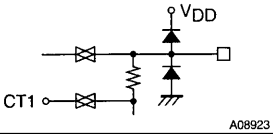
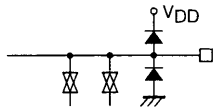
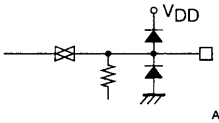
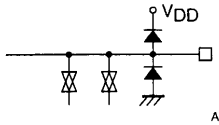
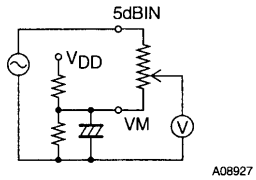
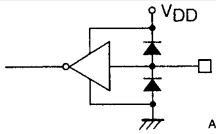
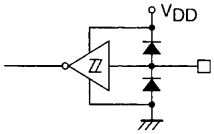
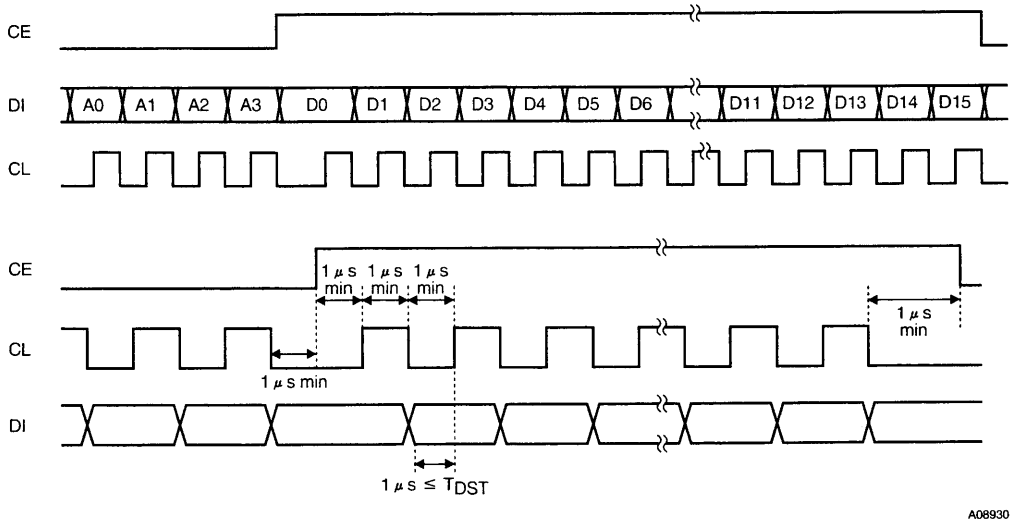
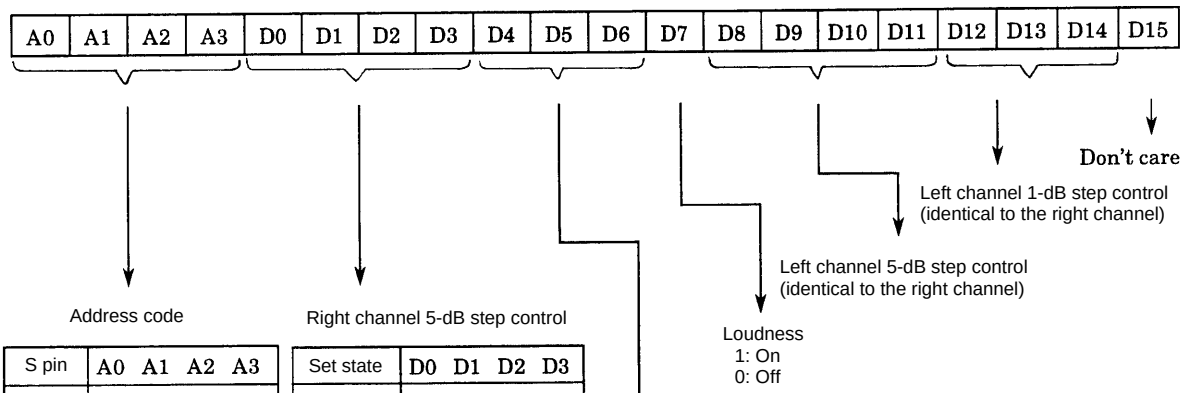
Pin Descriptions

Pin No.	Pin	Function	Equivalent circuit
2	L5dBIN	• 5-dB step attenuator inputs These inputs must be driven by low-impedance circuits.	
29	R5dBIN		
3	LCT1	• Loudness circuit connections Connect the high-band compensation capacitors between the CT1 and 5dBIN pins, and connect the low band compensation capacitors between the CT2 and the V_M pins.	
28	RCT1		
4	LCT2		
27	RCT2		
5	L5dBOUT	• 5-dB step attenuator outputs These outputs must be accepted by circuits with an impedance of between 47 kΩ and 1 MΩ.	
26	R5dBOUT		
7	L1dBIN	• 1-dB step attenuator inputs These inputs must be driven by low-impedance circuits.	
24	R1dBIN		
8	L1dBOUT	• 1-dB step attenuator outputs These outputs must be accepted by circuits with an impedance of between 47 kΩ and 1 MΩ.	
23	R1dBOUT		
9	LV_M	• Common connections for the volume control circuit. The impedance of the printed circuit board pattern connected to these pins must be kept as low as possible. Since the LV_M, RV_M, and V_{SS} pins are not connected internally, they must be connected externally as required by the various specifications. When a single-sided power supply is used, the capacitors between V_M and V_{SS} become the residual resistance when the volume control is set at its maximum attenuation. This means that care is required in selecting the values of these capacitors.	
22	RV_M		
12	S	• Selection input for the address code in the data format. If this pin is connected to V_{DD}, data will be accepted when the address code is 9, and if connected to V_{CC}, data will be accepted when the address code is 8.	
17	CL	• Input pins for the serial data used to control the device. These inputs must have an amplitude of 0 to 5 V. In applications in which any of microcontroller CL, DI, or CE may go high in backup mode (when $V_{DD} = V_{CC} = 0$ V), the signal lines must have series resistors of at least 2 kΩ inserted.	
18	DI		
19	CE		
10	V_{EE}	• Power supply connections. All these pins must be connected to the corresponding power supply voltage. When power is first applied, the V_{CC} voltage must not rise before V_{DD}.	
13	V_{DD}		
14	V_{SS}		
21	V_{CC}		
1, 6, 11, 15, 16, 20, 25, 30	NC	• Unconnected (NC) pins Do not connect any signals or devices to these pins.	

Control System Timing and Data Format

The stipulated serial data must be input to the CL, DI, and CE pins to control the LC7535M. The data consists of a total of 20 bits, of which 4 bits are address and 16 bits are data.





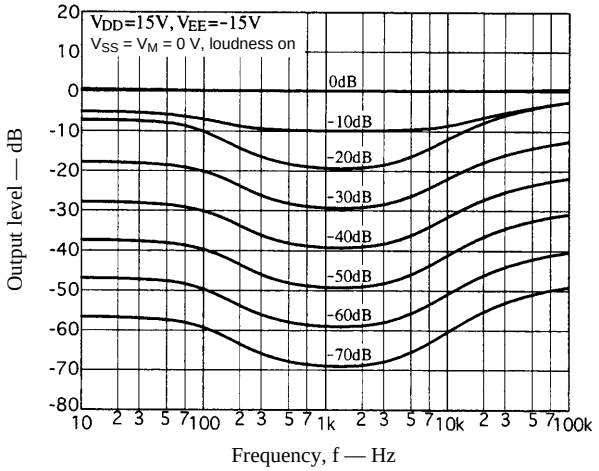
S pin	A0	A1	A2	A3
V_{DD}	1	0	0	1
V_{CC}	0	0	0	1

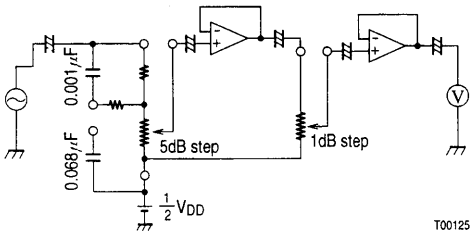
Set state	D0	D1	D2	D3
−75dB	0	0	0	0
−70dB	1	0	0	0
−65dB	0	1	0	0
−60dB	1	1	0	0
−55dB	0	0	1	0
−50dB	1	0	1	0
−45dB	0	1	1	0
−40dB	1	1	1	0
−35dB	0	0	0	1
−30dB	1	0	0	1
−25dB	0	1	0	1
−20dB	1	1	0	1
−15dB	0	0	1	1
−10dB	1	0	1	1
−5dB	0	1	1	1
0dB	1	1	1	1

Set state	D4	D5	D6
−∞	0	0	0
Dummy *	1	0	0
−4dB	0	1	0
−3dB	1	1	0
−2dB	0	0	1
−1dB	1	0	1
0dB	0	1	1

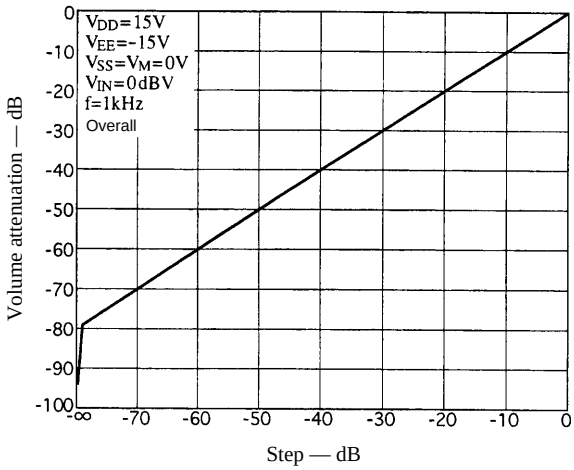
Note *: To minimize switching noise, applications should input dummy data in the following sequence: –79 dB → dummy → –∞

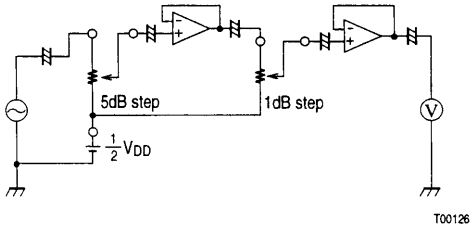
Loudness Characteristics



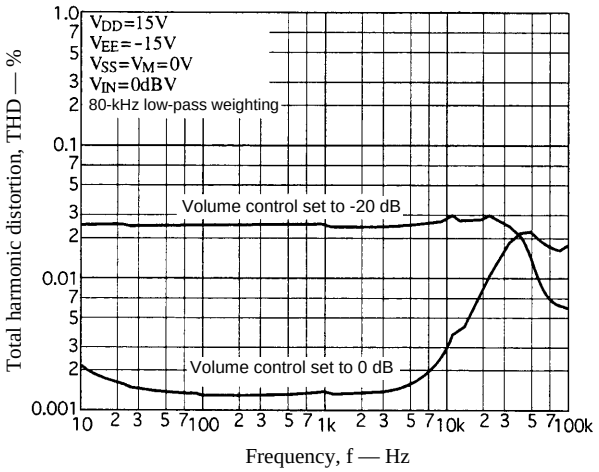


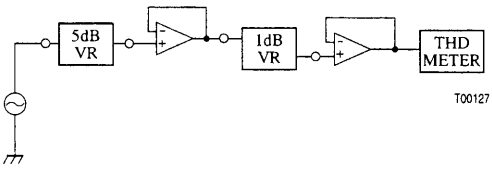
Volume Step Characteristics



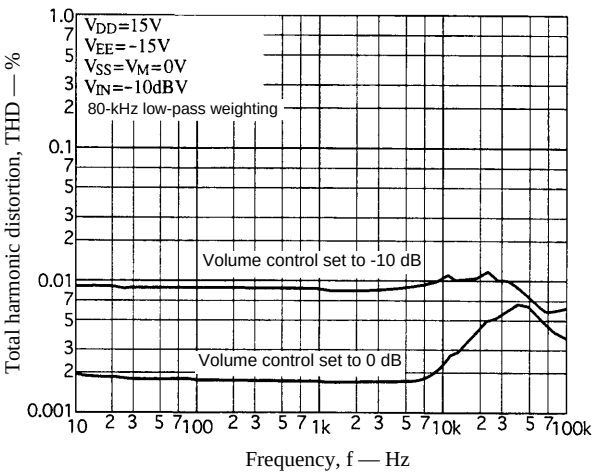


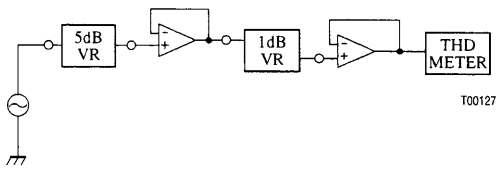
THD – Frequency Characteristics (1)



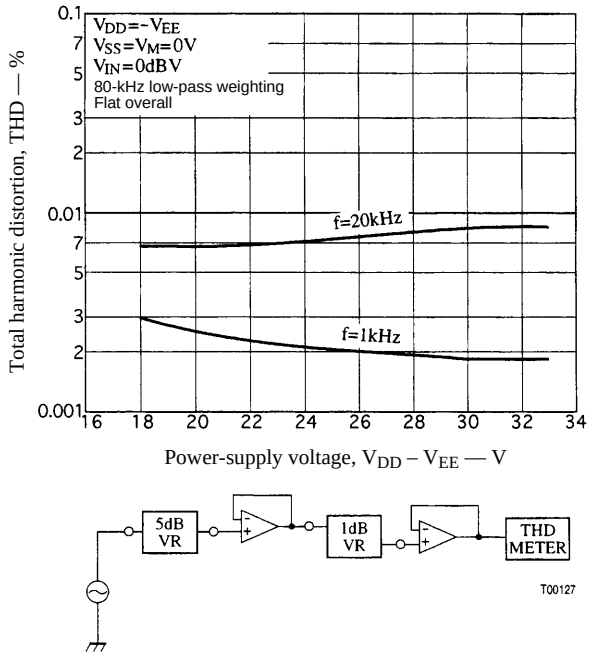


THD – Frequency Characteristics (2)

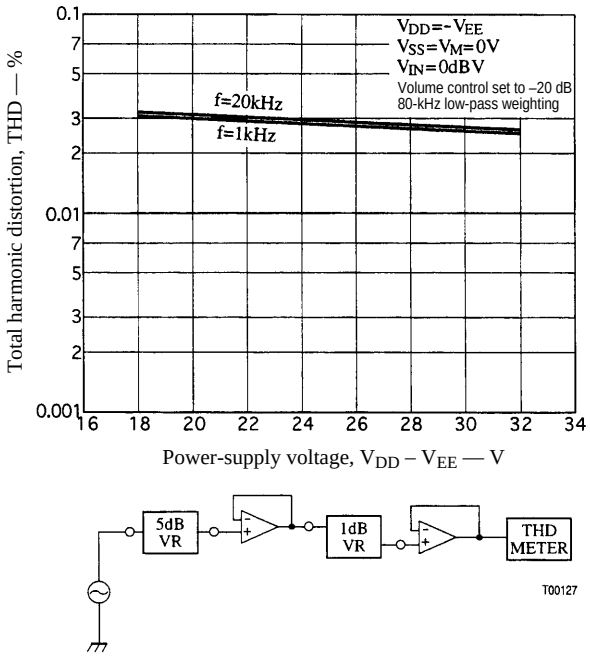




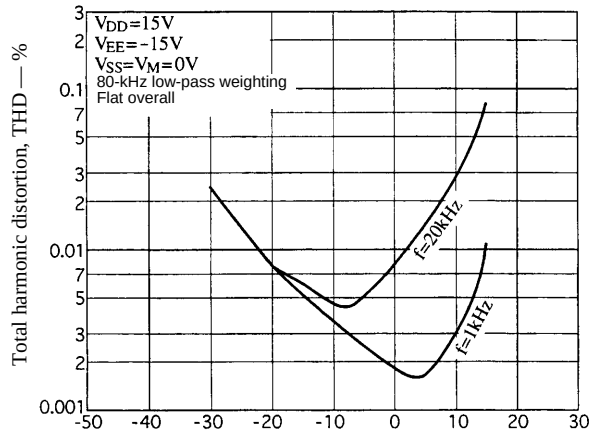
THD – Power-Supply Voltage Characteristics (1)

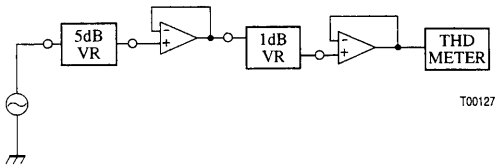


THD – Power-Supply Voltage Characteristics (2)

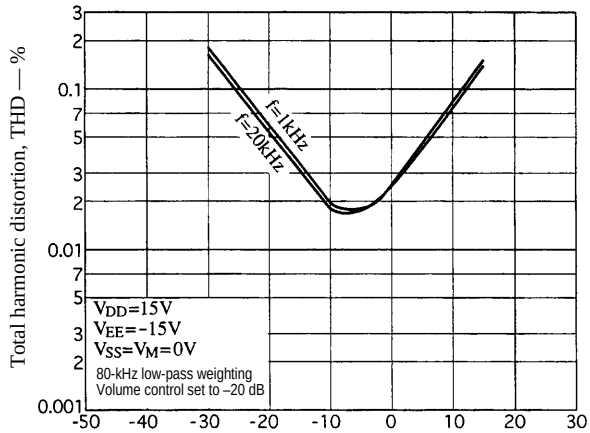


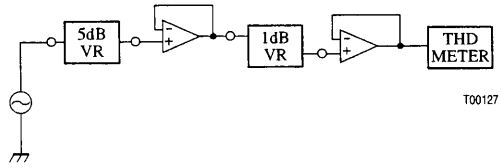
THD – Input Level Characteristics (1)



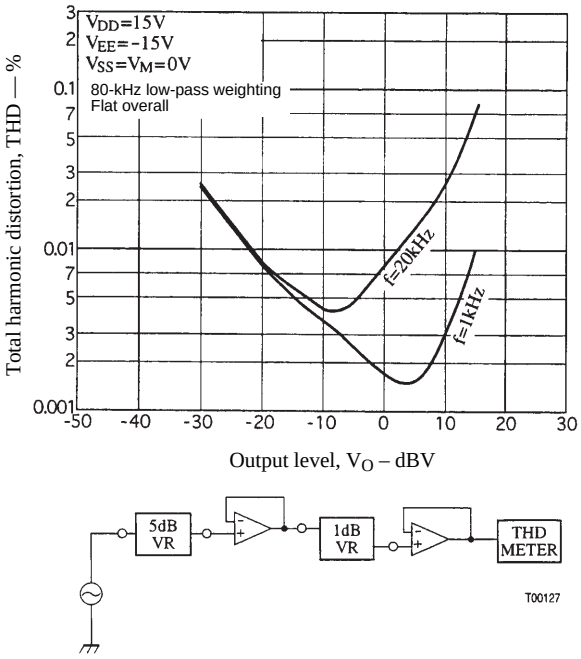


THD – Input Level Characteristics (2)

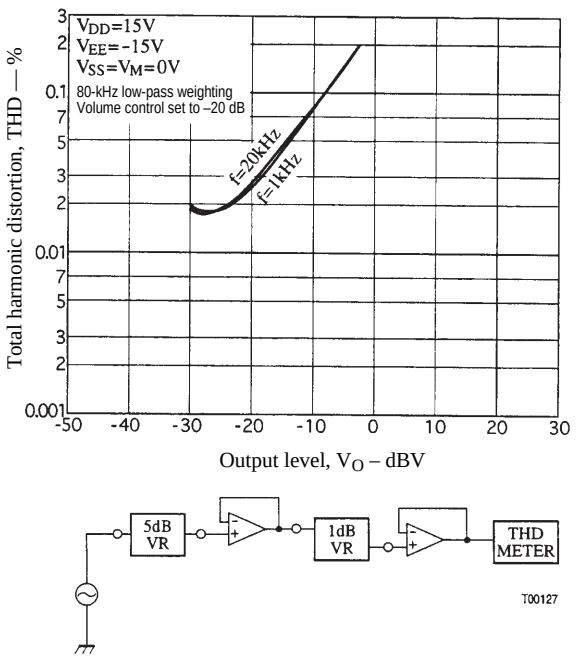




THD – Output Level Characteristics (1)



THD – Output Level Characteristics (2)



Usage Notes

- The state of the internal analog switches are undefined when power is first applied. Applications should apply external muting to the output signal until the control data has been set up.
- To prevent the high-frequency digital signals transmitted over the CL, DI, and CE pin lines from entering the analog signal system, these lines should either be covered by the ground pattern or shielded cables should be used.

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