

**LA76070****NTSC Color Television IC****Overview**

The LA76070 is an NTSC color television IC. In addition to providing IIC bus control based rationalization of IC control and the adjustment manufacturing process associated with the TV tube itself, it also includes all functions actually required in mass-produced television sets. As such, it is an extremely practical bus control IC.

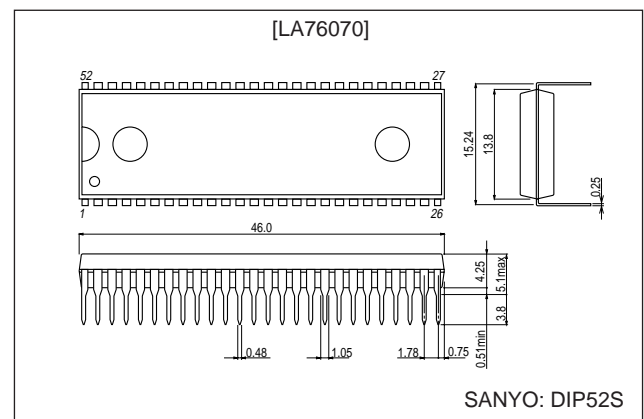
* The LA7840/41 or LA7845N/46N is recommended as the vertical output IC for use with this product.

Functions

- I²C bus control, VIF, SIF, Y, C, and deflection integrated on a single chip.

Package Dimensions

unit: mm

3128-DIP52S**Specifications****Maximum Ratings at Ta = 25°C**

Parameter	Symbol	Conditions	Rating	Unit
Maximum power supply voltage	V4 max		9.6	V
	V26 max		9.6	V
Maximum power supply current	I21 max		25	mA
Allowable power dissipation	Pd max	Ta ≤ 65°C*	1.3	W
Operating temperature	Topr		-10 to +65	°C
Storage temperature	Tstg		-55 to +150	°C

Note: *Provided on a printed circuit board: 83.2 × 86.0 × 1.6 mm, material: Bakelite

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Rating	Units
Recommended power supply voltage	V4		7.6	V
	V26		7.6	V
Recommended power supply current	I21		19	mA
Operating power supply voltage range	V4 op		7.3 to 7.9	V
	V26 op		7.3 to 7.9	V
Operating power supply current range	I21 op		16 to 25	mA

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SANYO Electric Co.,Ltd. Semiconductor Company

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

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Electrical Characteristics at $T_a = 25^\circ\text{C}$, $V_{CC} = V_4 = V_{26} = 7.6\text{ V}$, $I_{CC} = I_{21} = 19\text{ mA}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Circuit Voltages and Currents]						
Horizontal power supply voltage	HV_{CC}		7.2	7.6	8.0	V
IF power supply current (V4)	I4 ($IF_{I_{CC}}$)	IF AGC: 5 V	38	46	54	mA
Video, chroma, and vertical power supply current (V26)	I26 ($YCV_{I_{CC}}$)		79.5	93.5	107.5	mA
[VIF Block]						
AFT output voltage with no signal	$VAFT_n$	With no input signal	2.8	3.8	4.8	Vdc
Video output voltage with no signal	VO_n	With no input signal	4.7	4.9	5.1	Vdc
APC pull-in range (U)	fPU	After APC and PLL DAC adjustment	1.0			MHz
APC pull-in range (L)	fPL	After APC and PLL DAC adjustment	1.0			MHz
Maximum RF AGC voltage	VR_{FH}	CW = 91 dB μ , DAC = 0	7.7	8.2	9.0	Vdc
Minimum RF AGC voltage	VR_{FL}	CW = 91 dB μ , DAC = 63	0	0.2	0.4	Vdc
RF AGC Delay Pt (@DAC = 0)	RF_{AGC0}	DAC = 0	96			dB μ
RF AGC Delay Pt (@DAC = 63)	RF_{AGC63}	DAC = 63			86	dB μ
Maximum AFT output voltage	$VAFT_H$	CW = 93 dB μ , variable frequency	6.2	6.5	7.6	Vdc
Minimum AFT output voltage	$VAFT_L$	CW = 93 dB μ , variable frequency	0.5	0.9	1.2	Vdc
AFT detection sensitivity	$VAFT_S$	CW = 93 dB μ , variable frequency	33	25	17	mV/kHz
Video output amplitude	VO	93 dB μ , 87.5% Video MOD	1.8	2.0	2.2	Vp-p
Synchronization signal tip level	VO_{tip}	93 dB μ , 87.5% Video MOD	2.4	2.6	2.8	Vdc
Input sensitivity	V_i	Output at -3 dB		43	46	dB μ
Video-to-sync ratio (@100 dB μ)	V/S	100 dB μ , 87.5% Video MOD	2.4	2.5	3.0	
Differential gain	DG	93 dB μ , 87.5% Video MOD		2	10	%
Differential phase	DP	93 dB μ , 87.5% Video MOD		2	10	deg
Video signal-to-noise ratio	S/N	CW = 93 dB μ	55	58		dB
920 kHz beat level	I920	V3.58 MHz/V920 kHz			-50	dB
[Video and Switching Block]						
External video gain	AUXG	Stair step, 1 V p-p	5.5	6.0	6.5	dB
External video sync signal tip voltage	AUXS	Stair step, 1 V p-p	-0.2	0.0	+0.2	Vdc
External video crosstalk	AUXC	4.2 MHz, 1Vp-p	60			dB
Internal video output level	INTO	93 dB μ , 87.5% Video MOD	-0.1	0.0	+0.1	Vp-p
[SIF Block]						
FM detector output voltage	SOADJ		464	474	484	mVrms
FM limiting sensitivity	SLS	Output at -3 dB			50	dB μ
FM detector output bandwidth	SF	Output at -3 dB	50		100 k	Hz
FM detector output total harmonic distortion	STHD	FM = ± 25 kHz			0.5	%
AM rejection ratio	SAMR	AM = 30 %	40			dB
SIF signal-to-noise ratio	SSN		60			dB
[Audio Block]						
Maximum gain	AGMAX	1 kHz	-2.5	0.0	+2.5	dB
Adjustment range	ARANGE		60	67		dB
Frequency characteristics	AF	20 kHz	-3.0		+3.0	dB
Muting	AMUTE	20 kHz	75			dB
Total harmonic distortion	ATHD	1 kHz, 400 m Vrms, Vo1: MAX			0.5	dB
Signal-to-noise ratio	ASN	DIN.Audio	65	75		dB
[Chroma Block]						
ACC amplitude characteristics 1	ACCM1	Input: +6 dB/0 dB, 0 dB = 40 IRE	0.8	1.0	1.2	times
ACC amplitude characteristics 2	ACCM2	Input: -14 dB/0 dB	0.7	1.0	1.1	times
B-Y/Y amplitude ratio	CLRBY		100	125	140	%
Color control characteristics 1	CLRMN	Color MAX/NOM	1.6	1.8	2.1	times
Color control characteristics 2	CLRMM	Color MAX/MIN	33	40	50	dB

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Color control sensitivity	CLRSE		1	2	4	%/bit
Tint center	TINCEN	TINT NOM	-15		-3	deg
Tint control maximum	TINMAX	TINT MAX	30	45	60	deg
Tint control minimum	TINMIN	TINT MIN	-60	-45	-30	deg
Tint control sensitivity	TINSE		0.7		2.0	deg/bit
Demodulator output ratio R-Y/B-Y	RB		0.75	0.85	0.95	
Demodulator output ratio G-Y/B-Y	GB		0.28	0.33	0.38	
Demodulator angle B-Y/R-Y	ANGBR		92	99	107	deg
Demodulator angle G-Y/B-Y	ANGGB		227	237	247	deg
Killer operating point	KILL	0 dB = 40 IRE	-42	-37	-30	dB
Chrominance VCO free-running frequency	CVCOF	Deviation from 3.579545 MHz	-350		+350	Hz
Chrominance pull-in range (+)	PULIN+		350			Hz
Chrominance pull-in range (-)	PULIN-				-350	Hz
Auto-flesh characteristic 73°	AF 073		5	10	20	deg
Auto-flesh characteristic 118°	AF 118		-7	0	+7	deg
Auto-flesh characteristic 163°	AF 163		-20	-10	-5	deg
[Video Block]						
Overall video gain (Contrast set to maximum)	CONT63		10	12	14	dB
Contrast adjustment characteristic (Normal/maximum)	CONT32		-7.5	-6.0	-4.5	dB
Contrast adjustment characteristic (Minimum/maximum)	CONT0		-17	-14	-11	dB
Video frequency characteristic Trap & D = 0	Yf0		-6.0	-3.5	0.0	dB
Chrominance trap level Trap & D = 1	Ctrap			-20		dB
DC propagation	ClampG		95	100	105	%
Y delay, f0 = 1	YDLY			430		ns
Maximum black stretching gain	BKSTmax		6	13	20	IRE
Sharpness adjustment range	(normal)	Sharp16	4	6	8	dB
	(max)	Sharp31	9.0	11.5	14.0	dB
	(min)	Sharp0	-6.0	-3.5	-1.0	dB
Horizontal/vertical blanking output level	RGBBLK		1.4	1.6	1.8	V
[OSD Block]						
OSD fast switch threshold	FSTH		0.9	1.2	1.7	V
Red RGB output level	ROSDH		220	250	280	IRE
Green RGB output level	GOSDH		220	250	280	IRE
Blue RGB output level	BOSDH		220	250	280	IRE
Analog OSD R output level gain matching	RRGB		1.5	1.9	2.3	Ratio
Linearity	LRRGB		45	50	60	%
Analog OSD G output level gain matching	GRGB		1.5	1.9	2.3	Ratio
Linearity	LGRGB		45	50	60	%
Analog OSD B output level gain matching	BRGB		1.5	1.9	2.3	Ratio
Linearity	LBRGB		45	50	60	%
[RGB Output (cutoff and drive) Block]						
Brightness control (normal)	BRT64		2.1	2.65	3.2	V
High brightness (maximum)	BRT127		15	20	25	IRE
Low brightness (minimum)	BRT0		-25	-20	-15	IRE

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Parameter		Symbol	Conditions	Ratings			Unit
				min	typ	max	
Cutoff control (Bias control)	(minimum)	Vbias0		2.1	2.65	3.2	V
	(maximum)	Vbias127		2.45	3.0	3.55	V
	Resolution	Vbiasns			4		mV/Bit
Drive adjustment	Maximum output	RBout127			2.9		Vp-p
		Gout127			2.4		Vp-p
	Output attenuation	RBout0		7	9	11	dB
[Deflection Block]							
Sync separator sensitivity	Ssync			3	8	13	IRE
Horizontal free-running frequency deviation	Δf_H			15600	15734	15850	Hz
Horizontal pull-in range	fH PULL			± 400			Hz
Horizontal output pulse saturation voltage	V Hsat			0	0.06	0.4	V
Horizontal output pulse phase	HPHCEN			9.5	10.5	11.5	μ s
Horizontal position adjustment range	HPHrange	4 bits			± 2		μ s
Horizontal position adjustment maximum variability	HPHstep					530	ns
X-ray protection circuit operating voltage	VXRAY			0.54	0.64	0.74	V
[Vertical screen Size Adjustment]							
Vertical ramp output amplitude @32	Vsize32	VSIZE: 100000		0.47	0.82	1.17	Vp-p
Vertical ramp output amplitude @0	Vsize0	VSIZE: 000000		0.13	0.48	0.83	Vp-p
Vertical ramp output amplitude @63	Vsize63	VSIZE: 111111		0.80	1.15	1.50	Vp-p
[Vertical screen Position Adjustment]							
Vertical ramp DC voltage @32	Vdc32	VDC: 100000		3.6	3.8	4.0	Vdc
Vertical ramp DC voltage @0	Vdc0	VDC: 000000		3.2	3.4	3.6	Vdc
Vertical ramp DC voltage @63	Vdc63	VDC: 111111		4.0	4.2	4.4	Vdc

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LA76070 BUS: Initial Conditions

Initial test conditions	
Register	
T Enable	0 HEX
Video Mute	1 HEX
Sync Kill	0 HEX
AFC Gain	0 HEX
Horizontal Phase	4 HEX
IF AGC SW	0 HEX
AFT Defeat	0 HEX
RF AGC Delay	20 HEX

Initial test conditions (continued)	
Register	
Video SW	0 HEX
PLL Tuning	40 HEX
Audio Mute	1 HEX
APC Det Adjust	20 HEX
V CD Mode	0 HEX
Vertical DC	20 HEX
Vertical Kill	0 HEX
Col Kill	0 HEX
Vertical Size	20 HEX
Red Bias	00 HEX
Green Bias	00 HEX
Blue Bias	00 HEX
Blanking Defeat	0 HEX
Red Drive	7F HEX
Blue Drive	7F HEX
Color Difference Mode Enable	0 HEX
Brightness Control	40 HEX
Contrast Test Enable	0 HEX
Contrast Control	40 HEX
Trap & Delay Enable SW	0 HEX
Auto Flesh	0 HEX
Black Stretch Defeat	0 HEX
Sharpness Control	10 HEX
Tint Test Enable	0 HEX
Tint Control	40 HEX
Color Test Enable	0 HEX
Color Control	40 HEX
Vertical Test	0 HEX
Video Level	4 HEX
FM Level	10 HEX
BNI Enable	0 HEX
Audio SW	0 HEX
Volume Control	00 HEX

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LA76070 BUS: Control Register Descriptions

Control register descriptions		
Register name	Bits	General descriptions
T Enable	1	Disable the Test SW & enable Video Mute SW
Video Mute	1	Disable video outputs
Sync Kill	1	Force free-run mode
AFC Gain	1	Select horizontal first loop gain
Horizontal Phase	3	Align sync to flyback phase
IF AGC SW	1	Disable IF and RF AGC
AFT Defeat	1	Disable AFT output
RF AGC Delay	6	Align RF AGC threshold
Video SW	1	Select Video Signal (INT/EXT)
PLL Tuning	7	Align IF VCO frequency
Audio Mute	1	Disable audio outputs
APC Det Adjust	6	Align AFT crossover
V Count Down Mode	1	Select vertical countdown mode
Vertical DC	6	Align vertical DC bias
Vertical Kill	1	Disable vertical output
Color Kill	1	Enable Color Killer
Vertical Size	6	Align vertical amplitude
Red Bias	7	Align Red OUT DC level
Green Bias	7	Align Green OUT DC level
Blue Bias	7	Align Blue OUT DC level
Blanking Defeat	1	Disable RGB output blanking
Red Drive	6	Align Red OUT AC level
Drive Test	1	Enable drive DAC test mode
Blue Drive	6	Align Blue OUT AC level
Color Difference Mode Enable	1	Enable color difference mode
Brightness Control	7	Customer brightness control
Contrast Test	1	Enable Contrast DAC test mode
Contrast Control	7	Customer Contrast control
Trap & Delay-SW	1	Select luma filter mode
Auto Flesh Enable	1	Enable autoflesh function
Black Stretch Defeat	1	Disable black stretch
Sharpness Control	5	Customer sharpness control
Tint Test	1	Enable tint DAC test mode
Tint Control	7	Customer tint control
Color Test	1	Enable color DAC test mode
Color Control	7	Customer color control
Vertical Test	3	Select vertical DAC test modes
Video Level	3	Align IF video level
FM Level	5	Align WBA output level
BNI Enable	1	Enable black noise inverter
Audio SW	1	Select Audio Signal (INT/EXT)
Volume Control	6	Customer volume control

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LA76070 BUS: Control Register Truth Table

Control register truth table		
Register name	0 HEX	1 HEX
T Enable	Test Enable	Test Disable
Audio Mute	Active	Mute
Video Mute	Active	Mute
Sync Kill	Sync active	Sync Killed
AFC Gain	Slow	Fast
IF AGC SW	AGC active	AGC Defeat
AFT Defeat	AFT active	AFT Defeat
BNI Enable	BNI active	BNI Defeat
Count Down Mode	Standard	Non-Stand
Vertical Kill	Vrt active	Vrt Killed
F0 Select	3.58 trap	8.00 APF
Auto Flesh Enable	AF Off	AF On
Overload Enable	Ovid Off	Ovid On
Tint DAC Test	Normal	Test Mode
Color DAC Test	Normal	Test Mode
Contrast DAC Test	Normal	Test Mode
Drive DAC Test	Normal	Test Mode
Black Stretch Defeat	Blk Str On	Blk Str Off
Blanking Defeat	Blanking	No Blank
Color Diff Mode Enable	RGB Mode	C Diff Mode
Vertical Test	Normal	Ver Size Test

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LA76070 Bit Map ('96.08.01)

IC address: BAH (101111010)

Sub address D0....D7	MSB	DATA						LSB
	DA0	DA1	DA2	DA3	DA4	DA5	DA6	DA7
\$00 (tr0)	*	*	*	*	T_Enable 0	*	Vid_Mute 1	Sync_Kill 0
\$01 (tr1)	*	*	*	*	AFC Gain 0	H_Phase 1 0 0		
\$02 (tr2)	IFAGC SW 0	AFT DEF 0	RF_AGC_Delay 1 0 0 0 0 0					
\$03 (tr3)	VIDEO SW 0	PLL TUNING 1 0 0 0 0 0 0						
\$04 (tr4)	*	Aud_Mute 1	APC DET ADJUST 1 0 0 0 0 0					
\$05 (tr5)	V CD MODE 0	*	Ver_dc 1 0 0 0 0 0					
\$06 (tr6)	Ver_kill 0	Col_kill 0	Ver_Size 1 0 0 0 0 0					
\$07 (tr7)	*	R_Bias 0 0 0 0 0 0 0						
\$08 (tr8)	*	G_Bias 0 0 0 0 0 0 0						
\$09 (tr9)	*	B_Bias 0 0 0 0 0 0 0						
\$0A (tr10)	BLK_DEF 0	R_Drive 1 1 1 1 1 1 1						
\$0B (tr11)	Drv_Test 0	B_Drive 1 1 1 1 1 1 1						
\$0C (tr12)	C_Diff 0	Bright 1 0 0 0 0 0 0						
\$0D (tr13)	Cot_Test 0	Contrast 1 0 0 0 0 0 0						
\$0E (tr14)	Trap & D_SW 0	A Fresh 0	Black ST 0	Sharpness 1 0 0 0 0				
\$0F (tr15)	Tint_Test 0	Tint 1 0 0 0 0 0 0						
\$10 (tr16)	Col_Test 0	Color 1 0 0 0 0 0 0						
\$11 (tr17)	*	*	*	*	*	V_test 0 0 0		
\$12 (tr18)	VIDEO LEVEL 1 0 0			FM LEVEL 1 0 0 0 0				
\$13 (tr19)	N/I SW 0	AUDIO SW 0	VOLUME 0 0 0 0 0 0					





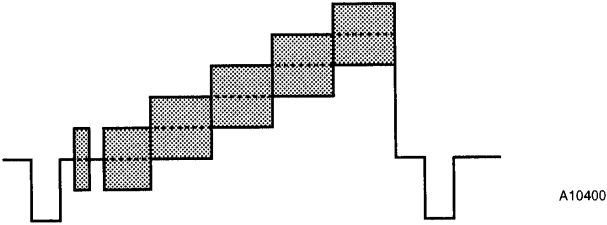
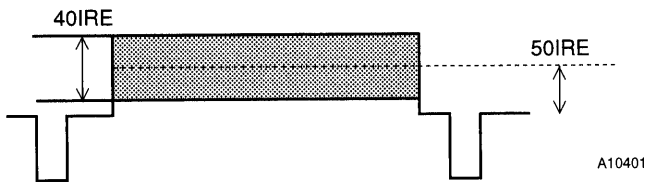
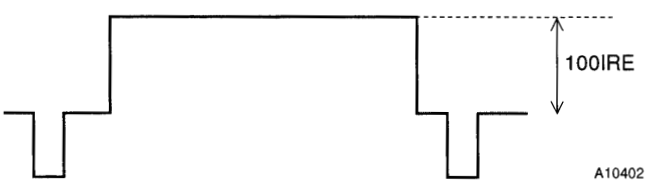
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Measurement Conditions at $T_a = 25^\circ\text{C}$, $V_{CC} = V_4 = V_{26} = 7.6\text{ V}$, $I_{CC} = I_{21} = 19\text{ mA}$

Parameter	Symbol	Measurement point	Input signal	Measurement method	Bus conditions
[Circuit Voltages and Currents]					
Horizontal power supply voltage	HV_{CC}	21		Apply a 19mA current to pin 21 and measure the pin 21 voltage at that time	Initial conditions
IF power supply current (pin 4)	I_4 (IF_{CC})	4	No signal	Apply a voltage of 7.6 V to pin 4 and measure (in mA) the DC current that flows into the IC. (Apply 5 V to the IF AGC.)	Initial conditions
Video/vertical power supply current (pin 26)	I_{26} (DEF_{CC})	26		Apply a voltage of 7.6 V to pin 26 and measure (in mA) the DC current that flows into the IC	Initial conditions

VIF Block Input Signals and Measurement Conditions

1. All input signals are applied to PIF IN (pin 10) as shown in the measurement circuit diagrams.
2. The input signal voltage values are all the value of VIF IN (pin 10) as shown in the measurement circuit diagrams.
3. The table below lists the input signals and their levels.

Input signal	Waveform	Condition
SG1	 CW A10396	45.75 MHz
SG2	 CW A10397	42.17 MHz
SG3	 CW A10398	41.25 MHz
SG4	 CW A10399	Variable frequency
SG5	 A10400	45.75 MHz 87.5 % video modulation 10-step staircase waveform (Subcarrier: 3.58 MHz)
SG6	 A10401	45.75 MHz 87.5 % video modulation Sweep signal (APL: 50 IRE Sweep signal level: 40 IRE)
SG7	 A10402	45.75 MHz 87.5 % video modulation Flat field signal

4. Perform the following D/A converter adjustments in the order listed before testing.

Item	Measurement point	Input signal	Adjustment
APC DAC	(13)	No signal, IF.AGC.DEF = 1	Set up the DAC value so that the pin 13 DC voltage is as close to 3.8 V as possible
PLL DAC	(13)	SG1, 93 dBμ	Set up the DAC value so that the pin 13 DC voltage is as close to 3.8 V as possible
Video possible	(45)	SG7, 93 dBμ	Set up the DAC value so that the pin 45 output level is as close to 2.0 V p-p as possible

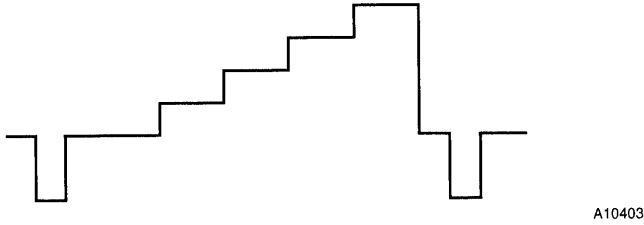

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Parameter	Symbol	Measurement point	Input signal	Measurement procedure	Bus conditions
[VIF Block]					
AFT output voltage with no signal	VAFTn	13	No signal	Measure the pin 13 DC voltage when IF.AGC. DEF is "1"	After performing the adjustments described in section 4
Video output voltage with no signal	VOn	45	No signal	Measure the pin 45 DC voltage when IF.AGC. DEF is "1"	After performing the adjustments described in section 4
APC pull-in range (U), (L)	fPU, fPL	45	SG4 93 dB μ	Connect an oscilloscope to pin 45 and modify the SG4 signal to be a frequency above 45.75 MHz so that the PLL circuit becomes unlocked. (Beating will occur in this state.) Gradually lower the SG4 frequency and measure the frequency at which the PLL circuit locks. Similarly, modify the frequency to a value below 45.75 MHz so that the PLL circuit becomes unlocked. Gradually raise the SG4 frequency and measure the frequency at which the PLL circuit locks.	After performing the adjustments described in section 4
Maximum RF AGC voltage	V _{RFH}	6	SG1 91 dB μ	Set the RF AGC DAC to 0 and measure the pin 6 DC voltage	After performing the adjustments described in section 4
Minimum RF AGC voltage	V _{RFL}	6	SG1 91 dB μ	Set the RF AGC DAC to 63 and measure the pin 6 DC voltage	After performing the adjustments described in section 4
RF AGC Delay Pt (@DAC = 0)	RFAGC0	6	SG1	Set the RF AGC DAC to 0 and determine the input level such that the pin 6 DC voltage becomes 3.8 V \pm 0.5 V	After performing the adjustments described in section 4
RF AGC Delay Pt (@DAC = 63)	RFAGC63	6	SG1	Set the RF AGC DAC to 63 and determine the input level such that the pin 4 DC voltage becomes 3.8 V \pm 0.5 V	After performing the adjustments described in section 4
Maximum AFT output voltage	VAFTH	13	SG4 93 dB μ	Set the SG4 signal frequency to 44.75 MHz and input that signal. Measure the pin 13 DC voltage at that time.	After performing the adjustments described in section 4
Minimum AFT output voltage	VAFTL	13	SG4 93 dB μ z	Set the SG4 signal frequency to 46.75 MHz and input that signal. Measure the pin 13 DC voltage at that time.	After performing the adjustments described in section 4
AFT detection sensitivity	VAFTS	13	SG4 93 dB μ z	Modify the SG4 frequency to determine the frequency deviation (Δ f) such that the pin 13 DC voltage changes from 2.5 V to 5.0 V. VAFTS = 2500/ Δ f [mV/kHz]	After performing the adjustments described in section 4
Video output amplitude	VO	45	SG7 93 dB μ	Observe pin 45 with an oscilloscope and measure the p-p value of the waveform	After performing the adjustments described in section 4
Synchronization signal tip level	VOtip	45	SG1 93 dB μ	Measure the pin 45 DC voltage	After performing the adjustments described in section 4
Input sensitivity	Vi	45	SG7	Observe pin 45 with an oscilloscope and measure the peak-to-peak value of the waveform. Next, gradually lower the input level to determine the input level such that the output becomes -3 dB below the video signal amplitude VO.	After performing the adjustments described in section 4
Video-to-sync ratio (@ 100 dB μ)	V/S	45	SG7 100 dB μ	Observe pin 45 with an oscilloscope and determine the value of the Vy/Vs ratio by measuring the peak-to-peak value of the sync waveform (Vs) and the peak-to-peak value of the luminance signal (Vy).	After performing the adjustments described in section 4
Differential gain	DG	45	SG5 93 dB μ	Measure pin 45 with a vectorscope	After performing the adjustments described in section 4
Differential phase	DP	45	SG5 93 dB μ	Measure pin 45 with a vectorscope	After performing the adjustments described in section 4
Video signal-to-noise ratio	S/N	45	SG1 93 dB μ	Pass the noise voltage that occurs on pin 45 through a 10 kHz to 4 MHz bandpass filter, measure that voltage (Vsn) with an rms voltmeter. Use that value to calculate 20 \times log (1.43/Vsn).	After performing the adjustments described in section 4
920 kHz beat level	1920	45	SG1 SG2 SG3	Input SG1 at 93 dB μ and measure the pin 12 DC voltage (V12). Mix three signals: SG1 at 87 dB μ , SG2 at 82 dB μ , and SG3 at 63 dB μ , and input that signal to VIF IN. Now, apply the V12 voltage to pin 12 using an external power supply. Measure the difference between the 3.58 MHz component and the 920 kHz component with a spectrum analyzer.	After performing the adjustments described in section 4

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Video Switch Block - Input Signals and Measurement Conditions

1. Unless otherwise indicated, these measurements are to be performed with no signal applied to PIF IN (pin 10) and with the D/A converter IF.ACG.SW set to "1".
2. The table below lists the input signals and their labels.

Input signal	Waveform	Condition
SG8		10-step staircase waveform 1 V p-p
SG9		4.2 MHz 1 Vp-p

Parameter	Symbol	Measurement point	Input signal	Measurement procedure	Bus conditions
[VIF Block]					
External video gain	AUXG	42	Pin 1 SG8	Observe pin 42 with an oscilloscope, measure the peak-to-peak value of the waveform, and perform the following calculation. $AUXG = 20 \times \log (Vp-p) [dB]$	VIDEO.SW = "1"
External video sync signal tip voltage	AUXS	42	Pin 1 SG8	Observe pin 42 with an oscilloscope and measure the synchronizing signal tip voltage in the waveform. Determine the voltage difference between this measured value and synchronizing signal tip level (VOTip) measured in the VIF block.	VIDEO.SW = "1"
External video crosstalk	AUXC	42	Pin 1 SG8	Measure the 4.2 MHz component in the pin 42 signal with a spectrum analyzer. Convert this measurement to a V peak-to-peak value and perform the following calculation. $AUXC = 20 \times \log (1.4/Vp-p) [dB]$	VIDEO.SW = "0"
Internal video output level	INTO	42	Pin 10 SG7 (VIF block) 93 dBμ	Observe pin 45 with an oscilloscope and measure the peak-to-peak value of the waveform. Determine the difference between this measured value and the video output amplitude (VO) measured in the VIF block.	After performing the adjustments described in section 4 IF. AGC. SW = "0" VIDEO. SW = "0"

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SIF Block (FM Block) - Input Signals and Measurement Conditions

Unless otherwise indicated, set up the following conditions for each of the following measurements.

1. Bus control condition: IF.AGC.DEF = 1
2. SW: IF1 = off
3. Apply the input signal to pin 49 and use a 4.5 MHz carrier signal.

Parameter	Symbol	Measurement point	Input signal	Measurement procedure	Bus conditions
FM detector output voltage	SOADJ	7	90 dB μ , fm = 1 kHz, FM = \pm 25 kHz	Adjust the DAC (FM.LEVEL) so that the pin 7 FM detector output 1kHz component is as close to 474 mV rms as possible, and measure the output at that time in mV rms. Record this measurement as SV1.	
FM limiting sensitivity	SLS	7	fm = 1 kHz, FM = \pm 25 kHz	Determine the input level (in dB μ) such that the pin 7 FM detector output 1kHz component is -3 dB down from the SV1 value	FM.LEVEL = adjusted value
FM detector output bandwidth	SF	7	90 dB μ , FM = \pm 25 kHz	Determine the modulation frequency bandwidth (Hz) that is -3 dB or higher relative to the pin 7 FM detector output SV1 value	FM.LEVEL = adjusted value
FM detector output total harmonic distortion	STHD	7	90 dB μ , fm = 1 kHz, FM = \pm 25 kHz	Determine the total harmonic distortion in the pin 7 FM detector output 1kHz component	FM.LEVEL = adjusted value
AM rejection ratio	SAMR	7	90 dB μ , fm = 1 kHz, AM = 30%	Measure the pin 7 FM detector output 1kHz component (in mV rms). Record this measured value as SV2 and perform the following calculation. SAMR = $20 \times \log (SV1/SV2)$ [dB]	FM.LEVEL = adjusted value
SIF signal-to-noise ratio	SSN	7	90 dB μ , CW	Set SW1:IF1 to the "ON" Measure the pin 7 noise level (in mV rms). Record this measured value as SV3 and perform the following calculation. SSN = $20 \times \log (SV1/SV3)$ [dB]	FM.LEVEL = adjusted value

Audio Block - Input Signals and Test Conditions

Parameter	Symbol	Measurement point	Input signal	Measurement procedure	Bus conditions
Maximum gain	AGMAX	51	1 kHz, CW 400m Vrms	Measure the output pin 1kHz component (V1: mV rms) and perform the following calculation. AGMAX = $20 \times \log (V1/400)$ [dB]	VOLUME = "111111" AUDIO.MUTE = "0"
Variability range	ARANGE	51	1 kHz, CW 400m Vrms	Measure the output pin 1kHz component (V2: mV rms) and perform the following calculation. AGMAX = $20 \times \log (V1/V2)$ [dB]	VOLUME = "000001" AUDIO.MUTE = "0"
Frequency characteristics	AF	51	20 kHz, CW 400m Vrms	Measure the output pin 20kHz component (V3: mV rms) and perform the following calculation. AF = $20 \times \log (V3/V1)$ [dB]	VOLUME = "111111" AUDIO.MUTE = "0"
Muting	AMUTE	51	20 kHz, CW 400m Vrms	Measure the output pin 20kHz component (V4: mV rms) and perform the following calculation. AMUTE = $20 \times \log (V3/V4)$ [dB]	VOLUME = "000000" AUDIO.MUTE = "0"
Total harmonic distortion	ATHD	51	1 kHz, CW 400m Vrms	Determine the total harmonic distortion in output pin 1kHz component	VOLUME = "111111" AUDIO.MUTE = "0"
Signal-to-noise ratio	ASN	51	No signal	Measure the noise level (DIN.AUDIO) on the output pin (V5: mV rms) and perform the following calculation. ASN = $20 \times \log (V1/V5)$ [dB]	VOLUME = "111111" AUDIO.MUTE = "0"

Chrominance Block - Input Signals and Measurement Conditions

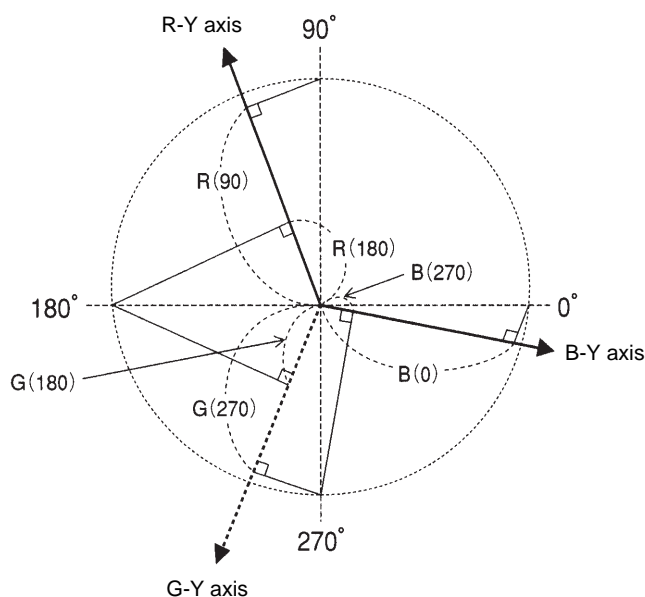
Unless otherwise indicated, set up the following conditions for each of the following measurements.

1. VIF and SIF blocks: No signal
2. Deflection block: Input a horizontal and vertical composite synchronizing signal, and assure that the deflection block is locked to the synchronizing signal. (Refer to the "Deflection Block - Input Signals and Measurement Conditions" section.)
3. Bus control conditions: All conditions set to the initial conditions unless otherwise specified.
4. Y input: No signal
5. C input: The C1IN input (pin 40) must be used.
6. The following describes the method for calculating the demodulation angle.

$$\text{B-Y axis angle} = \tan^{-1} (B(0)/B(270) + 270^\circ)$$

$$\text{R-Y axis angle} = \tan^{-1} (R(180)/R(90) + 90^\circ)$$

$$\text{G-Y axis angle} = \tan^{-1} (G(270)/G(180) + 180^\circ)$$



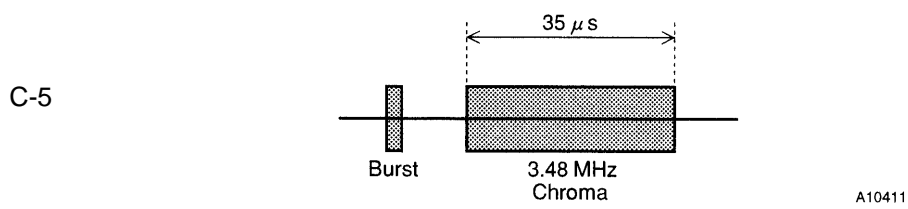
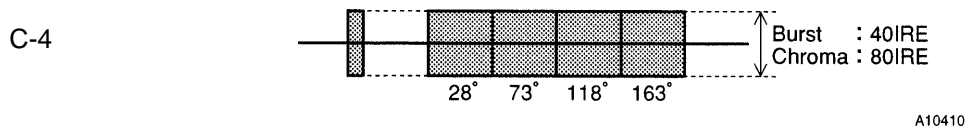
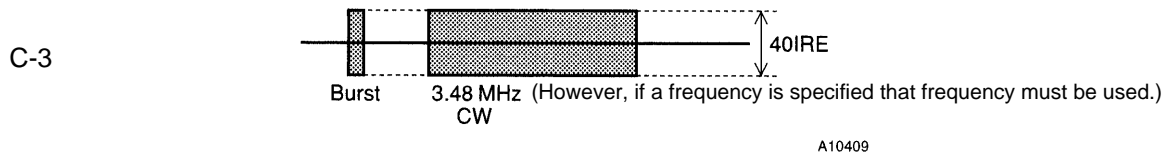
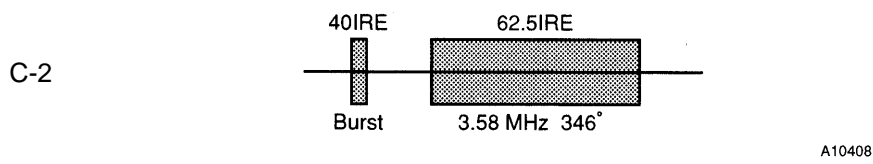
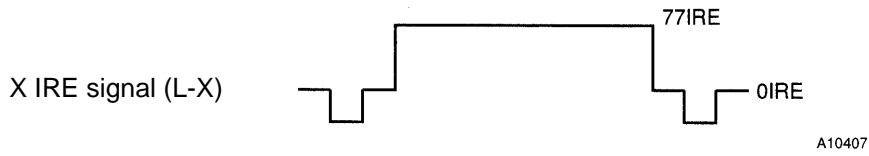
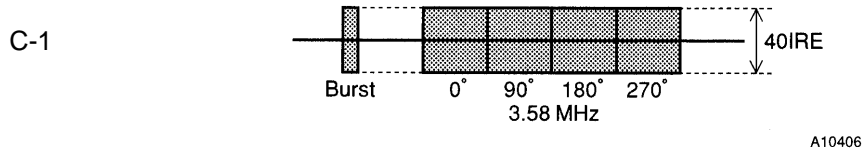
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7. The following describes the method for calculating the AF angle.
BR ... The ratio between the B-Y and R-Y demodulator outputs.
 θ ANGBR: The B-Y/R-Y demodulation angle

$$\text{AFXXX} = \tan^{-1} \left[\frac{\text{R-Y/B-Y} \times \text{BR} - \text{Cos} \theta}{\text{Sin} \theta} \right]$$

8. Attach a TV crystal externally to pin 15.

Chrominance Input Signals



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Parameter	Symbol	Measurement point	Input signal	Measurement procedure	Bus and other conditions
[Chroma Block]					
ACC amplitude characteristic 1	ACCM1	Bout 30	C-1 0 dB +6 dB	Measure the output amplitudes when the chrominance signal input is 0 dB and when that input is +6 dB and calculate the ratio. $ACCM1 = 20 \times \log (+6 \text{ dBdata}/0\text{dBdata})$	
ACC amplitude characteristic 2	ACCM2	Bout 30	C-1 -14 dB	Measure the output amplitude when the chrominance signal input is -14 dB and calculate the ratio. $ACCM2 = 20 \times \log (-14 \text{ dBdata}/0\text{dBdata})$	
B-Y/Y amplitude ratio	CLRBY	30	YIN: L77 C-1: No signal	Measure the Y output level (Record this measurement as V1)	
			C-2	Next, input a signal to CIN, and (with YIN a sync-only signal) measure the output level. (Record this measurement as V2) Calculate CLRBY from the following formula. $CLRBY = 100 \times (V2/V1) + 15\%$	
Color control characteristic 1	CLRMN	30	C-3	Measure V1: the output amplitude when the color control is maximum, and V2: the output amplitude when the color control is nominal. Calculate CLRMN as $V1/V2$.	TR24: Saturation 01111111 Saturation 01000000
Color control characteristic 2	CLRMN	30	C-3	Measure V3: the output amplitude when the color control is minimum. Calculate CLRMN as $CLRMN = 20 \times \log (V1/V3)$.	TR28: Saturation 00000000
Color control sensitivity	CLRSE	30	C-3	Measure V4: the output amplitude when the color control is 90, and V5: the output amplitude when the color control is 38. Calculate CLRSE from the following formula. $CLRSE = 100 \times (V4 - V5)/(V2 \times 52)$	TR24: Saturation 01011010 Saturation 00100110
Tint center	TINCEN	30	C-1	Measure all sections of the output waveform and calculate the B-Y axis angle	TR23: Tint 00111111
Tint control maximum	TINMAX	30	C-1	Measure all sections of the output waveform, calculate the B-Y axis angle, and calculate TINMAX from the following formula. $TINMAX = \langle \text{the B-Y axis angle} \rangle - TINCEN$	TR23: Tint 01111111
Tint control minimum	TINMIN	30	C-1	Measure all sections of the output waveform, calculate the B-Y axis angle, and calculate TINMIN from the following formula. $TINMIN = \langle \text{the B-Y axis angle} \rangle - TINCEN$	TR23: Tint 00000000
Tint control sensitivity	TINSE	30	C-1	Measure A1: the angle when the tint control is 85, and A2: the angle when the tint control is 42, and calculate TINSE from the following formula. $TINSE = (A1 - A2) / 43$	TR23: Tint 01010101 00101010
Demodulation output ratio R-Y/B-Y	RB	30 28	C-3	Measure Vb: the B _{OUT} output amplitude, and Vr: the R _{OUT} output amplitude. Determine $RB = Vr/Vb$.	TR24: Saturation 01000000
Demodulation output ratio G-Y/B-Y	GB	29	C-3	Measure Vg: the G _{OUT} output amplitude and determine $GB = Vg/Vb$	TR24: Saturation 01000000

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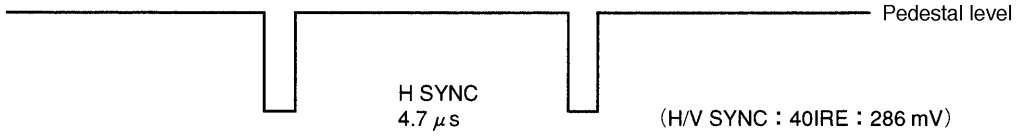
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Parameter	Symbol	Measurement point	Input signal	Measurement procedure	Bus and other conditions
Demodulation angle B-Y/R-Y	ANGBR	30 28	C-1	Measure the B_{OUT} and R_{OUT} output levels, calculate the angles of the B-Y and R-Y axes, and determine ANGBR as <the R-Y angle> – <the B-Y angle>.	
Demodulation angle B-Y/G-Y	ANGBG	29	C-1	Measure the G_{OUT} output level, calculate the angle of the G-Y axis, and determine ANGBG as <the G-Y angle> – <the B-Y angle>	
Killer operating point	KILL	30	C-3	Gradually lower the input signal level, and measure the input signal level at the point the output level falls under 150 mV p-p	
Chrominance VCO free-running frequency	CVCOF	15	CIN No signal	Measure the oscillator frequency f , and determine CVCOF from the following formula. $CVCOF = f - 3579545$ (Hz)	
Chrominance pull-in range (+)	PULIN +	30	C-1	Gradually lower the input signal subcarrier frequency starting from 3.57545 MHz + 2000 Hz, and measure the frequency when the output waveform locks	
Chrominance pull-in range (-)	PULIN -	30	C-1	Gradually raise the input signal subcarrier frequency starting from 3.57545 MHz – 2000 Hz, and measure the frequency when the output waveform locks	
Auto flesh characteristic 73°	AF073	30 28	C-4	With Auto Flesh = 0, measure the level that corresponds to 73° for the B_{OUT} and R_{OUT} output waveforms, and calculate the angle AF073A. With Auto Flesh = 1, determine the angle AF073B in the same way. Calculate AF073 from the following formula. $AF073 = AF073B - AF073A$	TR22: Auto flesh: 0***** TR22: Auto flesh: 1*****
Auto flesh characteristic 118°	AF118	30 28	C-4	With Auto Flesh = 0, measure the level that corresponds to 118° for the B_{OUT} and R_{OUT} output waveforms, and calculate the angle AF118A. With Auto Flesh = 1, determine the angle AF118B in the same way. Calculate AF118 from the following formula. $AF118 = AF118B - AF118A$	TR22: Auto flesh: 0***** TR22: Auto flesh: 1*****
Auto flesh characteristic 163°	AF163	30 28	C-4	With Auto Flesh = 0, measure the level that corresponds to 163° for the B_{OUT} and R_{OUT} output waveforms, and calculate the angle AF163A. With Auto Flesh = 1, determine the angle AF163B in the same way. Calculate AF163 from the following formula. $AF163 = AF163B - AF163A$	TR22: Auto flesh: 0***** TR22: Auto flesh: 1*****

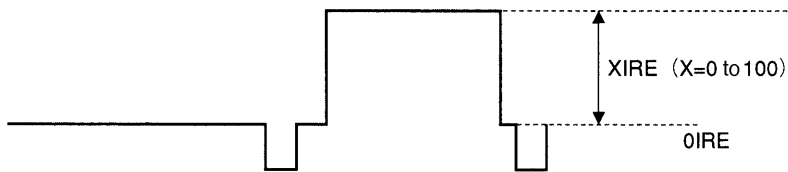
Video Block - Input Signals and Measurement Conditions

- C IN input signal * chrominance burst signal: 40 IRE
- Y IN input signal 100 IRE: 714 mV
- *0 IRE signal (L-0): Standard NTSC synchronizing signal



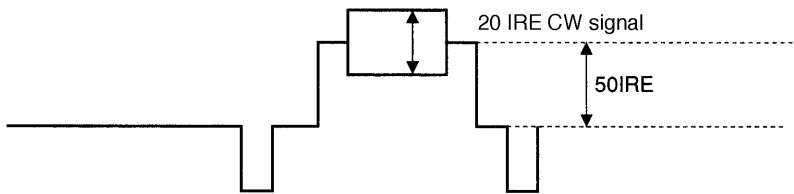
A10412

XIRE signal (L-X)



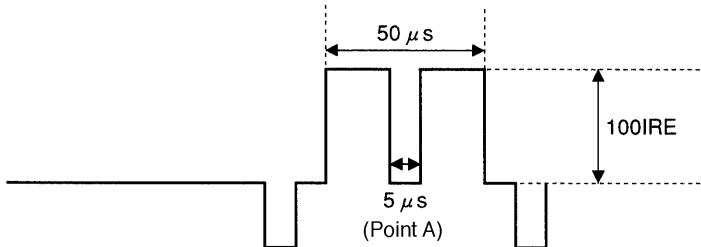
A10413

CW signal (L-CW)



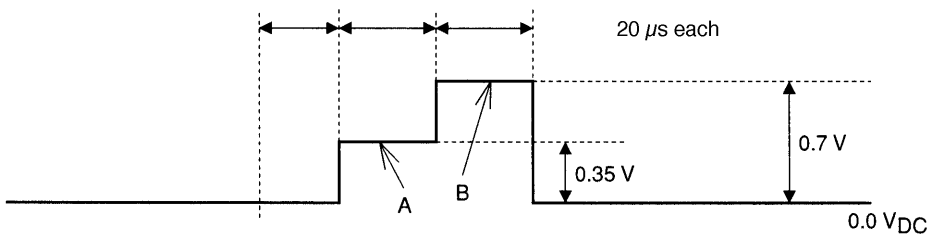
A10414

Black stretch 0 IRE signal (L-BK)



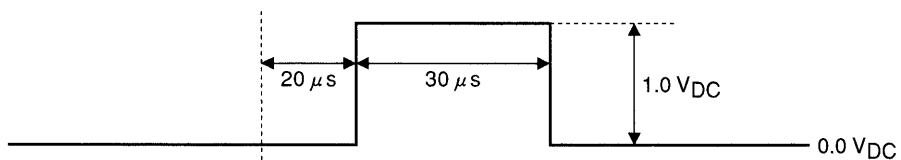
A10415

- R/G/B input signal
- RGB input signal 1 (O-1)



A10416

RGB input signal 2 (O-2)



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Parameter	Symbol	Measurement point	Input signal	Measurement procedure	Bus conditions and input signals
[Video Block]					
Overall video gain (contrast: maximum)	CONT127	30	L-50	Measure the output signal 50 IRE amplitude (CNTHB V p-p) and calculate CONT127 as $20 \times \log(\text{CNTHB}/0.357)$.	Contrast max 1111111
Contrast adjustment characteristics (normal/maximum)	CONT63	30	L-50	Measure the output signal 50 IRE amplitude (CNTCB V p-p) and calculate CONT63 as $20 \times \log(\text{CNTCB}/\text{CNTHB})$.	Contrast center 0111111
Contrast adjustment characteristics (minimum/maximum)	CONT0	30	L-50	Measure the output signal 50 IRE amplitude (CNTLB V p-p) and calculate CONT0 as $20 \times \log(\text{CNTLB}/\text{CNTHB})$.	Contrast min 0000000
Video frequency characteristics		30			
DC propagation	ClampG	30	L-0	Measure the output signal 0 IRE DC level (BRTPL V)	Brightness min 0000000 Contrast max 1111111
			L-100	Measure the output signal 0 IRE DC level (DRVPH V) and the 100 IRE amplitude (DRVH V p-p), and calculate ClampG as $100 \times (1 + (\text{DRVPH} - \text{BRTPL})/\text{DRVH})$.	Brightness min 0000000 Contrast max 1111111
Y delay	YDLY	30			
Maximum black stretching gain	BKSTmax	30	L-BK	Measure the output signal 0 IRE DC level at point A when the black stretch function is defeated (off). Record this value as BKST1 (V).	BKST defeat on (1)
			L-BK	Measure the output signal 0 IRE DC level at point A when the black stretch is enabled (on). Record this value as BKST2 (V).	BKST defeat off (0)
			L-BK	Calculate BKSTmax from the following formula. $\text{BKSTmax} = 2 \times 50 \times (\text{BKST1} - \text{BKST2})/\text{CNTHB}$	
Sharpness (peaking)		30	L-CW		
			L-CW		
			L-CW		
Horizontal/vertical blanking output level	RGB _{BLK}	30	L-100	Measure the output signal blanking period DC level. Record that value as RGB _{BLK} V.	

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Parameter	Symbol	Measurement point	Input signal	Measurement procedure	Bus conditions and input signals
[OSD Block]					
OSD fast switch threshold	FS _{TH}	30	L-0 O-2	Apply a voltage to pin 36 and determine the pin 36 voltage when the output signal switches to the OSD signal	Pin 35: Apply O-2
Red RGB output level	R _{OSDH}	28	L-50	Measure the output signal 50 IRE amplitude (CNTCR V p-p)	
			L-0 O-2	Measure the OSD output amplitude (OSDHR V p-p)	Pin 36: 2.0 V Pin 33: Apply O-2
				Calculate R _{OSDH} as 50 × (OSDHR/CNTCR)	
Green RGB output level	G _{OSDH}	29	L-50	Measure the output signal 50 IRE amplitude (CNTCG V p-p)	
			L-0 O-2	Measure the OSD output amplitude (OSDHG V p-p)	Pin 36: 2.0 V Pin 34: Apply O-2
				Calculate G _{OSDH} as 50 × (OSDHG/CNTCG)	
Blue RGB output level	B _{OSDH}	30	L-50	Measure the output signal 50 IRE amplitude (CNTCB V p-p)	
			L-0 O-2	Measure the OSD output amplitude (OSDHB V p-p)	Pin 36: 2.0 V Pin 35: Apply O-2
				Calculate B _{OSDH} as 50 × (OSDHB/CNTCB)	
Analog OSD R output level		28	L-0 O-1	Measure the amplitude of points A (the 0.35 V section in the input signal O-1) and B (the 0.7 V section in the input signal O-1) in the output signal and record those values as RGBLR and RGBHR V p-p, respectively	Pin 36: 2.0 V Pin 33: Apply O-1
Gain matching	R _{RGB}			Calculate R _{RGB} as RGBLR/CNTCR	
Linearity	LR _{RGB}			Calculate LR _{RGB} as 100 × (RGBLR/RGBHR)	
Analog OSD G output level		29	L-0 O-1	Measure the amplitude of points A (the 0.35 V section in the input signal O-1) and B (the 0.7 V section in the input signal O-1) in the output signal and record those values as RGBLG and RGBHG V p-p, respectively	Pin 36: 2.0 V Pin 34: Apply O-1
Gain matching	G _{RGB}			Calculate G _{RGB} as RGBLG/CNTCG	
Linearity	LG _{RGB}			Calculate LG _{RGB} as 100 × (RGBLG/RGBHG)	
Analog OSD B output level		30	L-0 O-1	Measure the amplitude of points A (the 0.35 V section in the input signal O-1) and B (the 0.7 V section in the input signal O-1) in the output signal and record those values as RGBLB and RGBHB V p-p, respectively	Pin 36: 2.0 V Pin 35: Apply O-1
Gain matching	B _{RGB}			Calculate B _{RGB} as RGBLB/CNTCB	
Linearity	LB _{RGB}			Calculate LB _{RGB} as 100 × (RGBLB/RGBHB)	

Parameter	Symbol	Measurement point	Input signal	Measurement procedure	Bus conditions and input signals
[RGB Output Block] (Cutoff and Drive Blocks)					
Brightness control (normal)	BRT63	28	L-0	Measure the output signal 0 IRE DC levels for the R output (28), G output (29), and B output (30). Record these values as BRTPCR, BRTPCG, and BRTPCB V, respectively.	Contrast max 1111111
		29			
		30			
(max)	BRT127			Measure the output signal 0 IRE DC levels for the B output (30). Record this value as BRTPHB.	Brightness max 1111111
				Calculate BRT127 as 50 × (BRTPHB – BRTPCB)/CNTHB	
(min)	BRT0	30		Measure the output signal 0 IRE DC levels for the B output (30). Record this value as BRTPLB.	Brightness min 0000000
				Calculate BRT0 as 50 × (BRTPLB – BRTPCB)/CNTHB	

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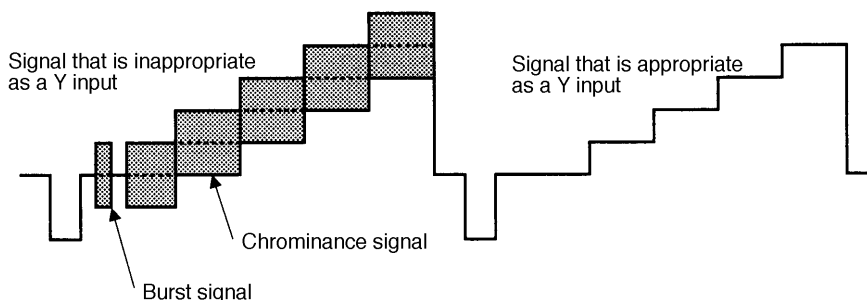
Parameter	Symbol	Measurement point	Input signal	Measurement procedure	Bus and other conditions
[RGB Output Block] (Cutoff and Drive Blocks)					
(minimum)	Vbias0	28	L-50	Measure the output signal 0 IRE DC levels for the R output (pin 28), G output (pin 29), and B output (pin 30). Record these values as Vbias0*(V). Here, * is R, G, and B, respectively.	Contrast max 1111111
(maximum)	Vbias127			Measure the output signal 0 IRE DC levels for the R output (pin 28), G output (pin 29), and B output (pin 30). Record these values as Vbias128*(V). Here, * is R, G, and B, respectively.	R bias max 1111111 G bias max 1111111 B bias max 1111111 Contrast max 1111111
Bias (cutoff) control					
Bias (cutoff) control resolution	Vbiasns	29		Measure the output signal 0 IRE DC levels for the R output (pin 28), G output (pin 29), and B output (pin 30). Record these values as BAS80*. Here, * is R, G, and B, respectively.	R bias: 1010000 G bias: 1010000 B bias: 1010000 Contrast max 1111111
		30		Measure the output signal 0 IRE DC levels for the R output (pin 28), G output (pin 29), and B output (pin 30). Record these values as BAS48*(V). Here, * is R, G, and B, respectively.	R bias: 0110000 G bias: 0110000 B bias: 0110000 Contrast max 1111111
Vbiasns* = (BAS80* - BAS48*)/32					
Drive adjustment: Maximum output	RGBout127	28	L-100	Measure the output signal 100 IRE amplitudes for the R output (pin 28), G output (pin 29), and B output (pin 30). Record these values as DRVH* (V p-p). Here, * is R, G, and B, respectively.	Contrast max 1111111 Brightness min 0000000
Output attenuation	RGBout0			29	Measure the output signal 100 IRE amplitudes for the R output (pin 28), G output (pin 29), and B output (pin 30). Record these values as DRVL* (V p-p). Here, * is R, G, and B, respectively.
		30			
RGBout0* = 20 × log (DRVH*/DRVL*)					

Deflection Block - Input Signals and Measurement Conditions

Unless otherwise indicated, set up the following conditions for each of the following measurements.

1. VIF and SIF blocks: No signal
2. C input: No signal
3. SYNC input: Horizontal and vertical composite synchronizing signal (40 IRE and other conditions, such as timing, must conform to the FCC broadcast standards.)

Caution: The burst and chrominance signals must not be below the pedestal level.



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4. Bus control conditions: All conditions set to the initial conditions unless otherwise specified.
5. The delay between the rise of the horizontal output (the pin 23 output) and the rise of the F.B.P IN (the pin 24 input) must be 9 μ s.
6. Unless otherwise specified, pin 25 (the X-ray protection circuit input) must be connected to ground.

Caution:

Perform the following operation if horizontal pulse output has stopped.

1. The bus data T_ENABLE bit must be temporarily set to 0 and then set to 1.
(If the X-ray protection circuit operates, an IC internal latch circuit will be set. To reset that latch circuit, the T_ENABLE bit must be temporarily set to 0, even if there is no horizontal output signal being output.)

Notes on Video Muting

If horizontal pulse output has stopped, perform the operation described in item 1. above and then set the video mute bit set to 0.

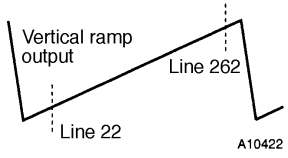
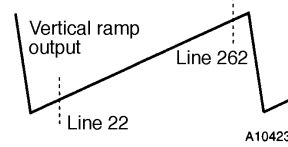
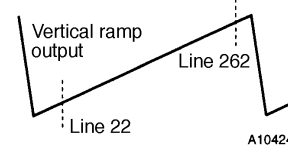
(This is because the video mute bit is forcibly set to the mute setting when the T_ENABLE bit is set to 0 or when the X-ray protection circuit operates. This also applies when power is first applied.)

Parameter	Symbol	Measurement point	Input signal	Measurement procedure	Bus conditions
[Deflection Block]					
Sync separator circuit sensitivity	Ssync	37	SYNC IN: horizontal and vertical synchronizing signal	Gradually lower the level of the synchronizing signal input to Y IN (pin 37) and measure the level of the synchronizing signal at the point synchronization is lost	
Horizontal free-running frequency deviation	ΔfH	23	SYNC IN: No signal	Connect a frequency counter to the pin 23 output (Hout) and measure the horizontal free-running frequency. Calculate the deviation from the following formula. $\Delta fH = \text{<measured value>} - 15.734 \text{ kHz}$	
Horizontal pull-in range	fH PULL	37	SYNC IN: horizontal and vertical synchronizing signal	Monitor the horizontal synchronizing signal input to Y IN (pin 37) and the pin 23 output (Hout), and measure the pull-in range by modifying the horizontal synchronizing signal frequency	
Horizontal pulse output saturation voltage	V Hsat	23	SYNC IN: horizontal and vertical synchronizing signal	Measure the voltage during the low-level period in the pin 23 horizontal output pulse	

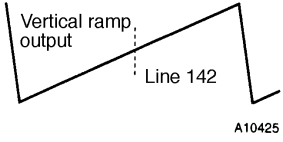
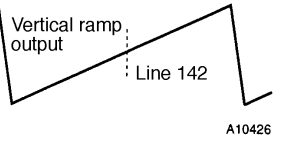
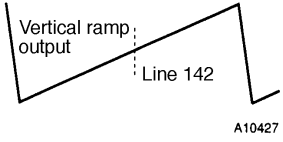
LA76070

Parameter	Symbol	Measurement point	Input signal	Measurement procedure	Bus conditions
Horizontal output pulse phase	HPHCEN	23 37	SYNC IN: horizontal and vertical synchronizing signal	<p>Measure the delay between the rise of the pin 23 horizontal output pulse and the fall of the Y IN horizontal synchronizing signal</p> <p>A10419</p>	
Horizontal position adjustment range	HPHrange	23 37	SYNC IN: horizontal and vertical synchronizing signal	<p>Measure the delay between the rise of the pin 23 horizontal output pulse and the fall of the Y IN horizontal synchronizing signal when HPHASE is set to 0 and when it is set to 7, and calculate the difference between those measurements and HPHCEN</p> <p>A10420</p>	Hphase: 000 Hphase: 111
Horizontal position adjustment maximum deviation	HPHstep	23 37	SYNC IN: horizontal and vertical synchronizing signal	<p>Measure the delay between the rise of the pin 23 horizontal output pulse and the fall of the SYNC IN horizontal synchronizing signal as HPHASE is set to each value from 0 to 7, and calculate the amount of the change at each step. Find the step size with the largest change.</p> <p>A10421</p>	Hphase: 000 to Hphase: 111
X-ray protection circuit operating voltage	V _{XRAY}	23 25	SYNC IN: horizontal and vertical synchronizing signal	<p>Connect a DC voltage source to pin 25 and gradually increase the voltage starting at 0 V. Measure the pin 25 DC voltage at the point that the pin 23 horizontal pulse output stops.</p>	

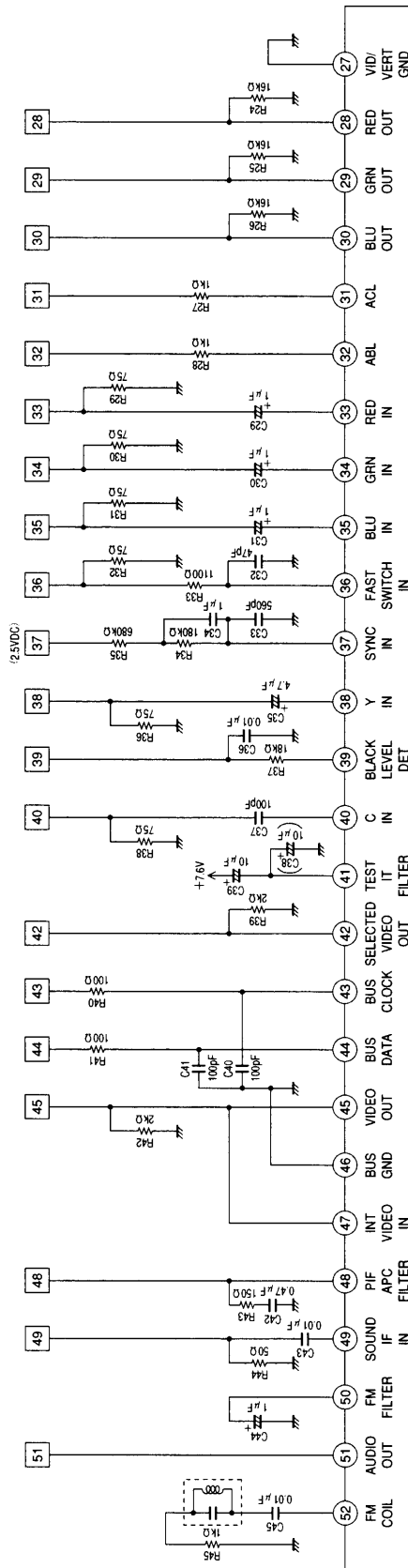
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Parameter	Symbol	Measurement point	Input signal	Measurement procedure	Bus conditions
[Vertical screen Size Adjustment]					
Vertical ramp output amplitude @32	Vsize32	17	SYNC IN: horizontal and vertical synchronizing signal	Monitor the pin 17 vertical ramp output and measure the voltages at the line 22 and line 262. Calculate Vsize32 from the following formula. $Vsize32 = Vline262 - Vline22$ 	
Vertical ramp output amplitude @0	Vsize0	17	SYNC IN: horizontal and vertical synchronizing signal	Monitor the pin 17 vertical ramp output and measure the voltages at the line 22 and line 262. Calculate Vsize32 from the following formula. $Vsize0 = Vline262 - Vline22$ 	VSIZE: 0000000
Vertical ramp output amplitude @63	Vsize63	17	SYNC IN: horizontal and vertical synchronizing signal	Monitor the pin 17 vertical ramp output and measure the voltages at the line 22 and line 262. Calculate Vsize32 from the following formula. $Vsize63 = Vline262 - Vline22$ 	VSIZE: 1111111

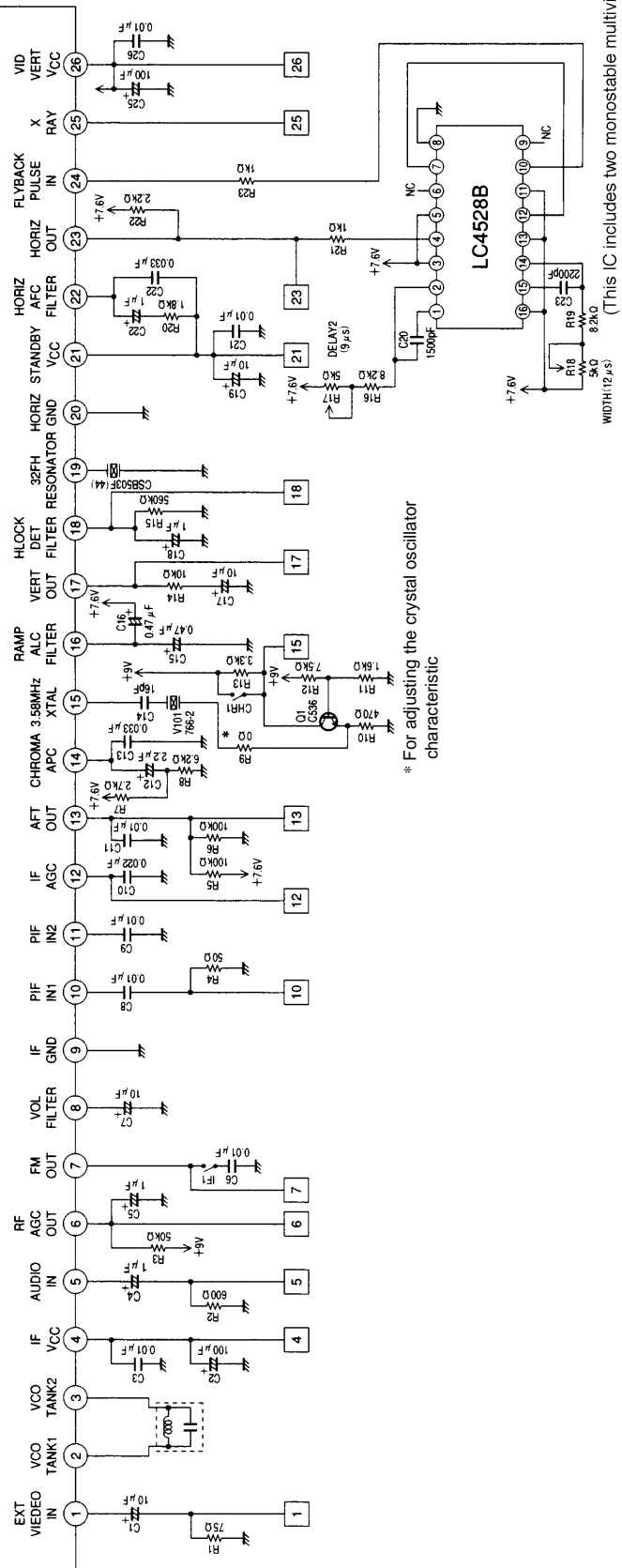
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Parameter	Symbol	Measurement point	Input signal	Measurement procedure	Bus conditions
[Vertical screen Position Adjustment]					
Vertical ramp DC voltage @32	Vdc32	17	SYNC IN: horizontal and vertical synchronizing signal	Monitor the pin 17 vertical ramp output and measure the voltage at line 142 	
Vertical ramp DC voltage @0	Vdc0	17	SYNC IN: horizontal and vertical synchronizing signal	Monitor the pin 17 vertical ramp output and measure the voltage at line 142 	VDC: 0000000
Vertical ramp DC voltage @63	Vdc63	17	SYNC IN: horizontal and vertical synchronizing signal	Monitor the pin 17 vertical ramp output and measure the voltage at line 142 	VDC: 1111111

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* For adjusting the crystal oscillator characteristic

(This IC includes two monostable multivibrators.)
AC0996

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