Ordering number : EN6089

CMOS IC

LC7536M

Serially Controlled Electronic Volume Control that Handles High Voltages

Overview

The LC7536M is an electronic volume control that implements volume, balance, and loudness functions with a minimum number of external components, and can be controlled electronically with serial data.

Functions

- Volume: 81 positions from 0 to –79 dB (in 1-dB steps) and –∞. Since the left and right channels can be controlled separately, a balance function can be implemented easily.
- Loudness: A tap is output from the –20 dB position of a 5 dB step volume control resistor ladder. A loudness function can be implemented by connecting an external RC circuit.
- S (select): Up to two LC7536M ICs can be used on the same bus.
- Serial data input: The LC7536M supports control and communication in the CCB format.

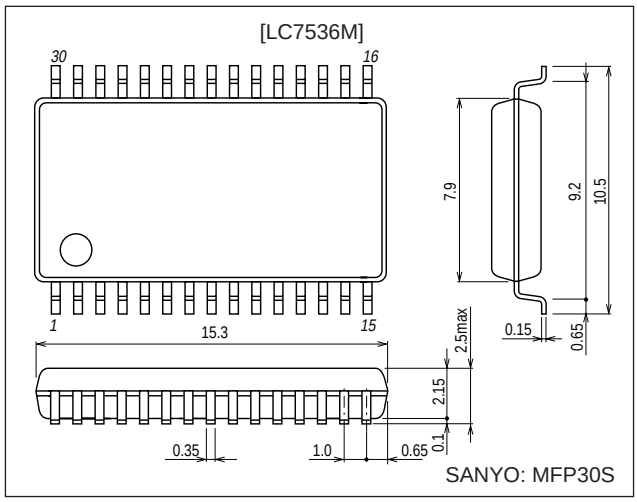
Features

- High voltage handling capability: ±16 V.

Package Dimensions

unit: mm

3216A-MFP30S



- **CCB is a trademark of SANYO ELECTRIC CO., LTD.**
- **CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.**

SANYO Electric Co.,Ltd. Semiconductor Company

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41399RM (OT) No. 6089-1/10

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	$V_{EE} \le V_{SS} < V_{CC} < V_{DD}$	V_{SS} to V_{SS} + 18	V
	V_{EE} max	$V_{EE} \le V_{SS} < V_{CC} < V_{DD}$	V_{SS} – 18 to V_{SS}	V
	V_{CC} max	$V_{EE} \le V_{SS} < V_{CC} < V_{DD}$	V_{SS} to V_{SS} + 7	V
Maximum input voltage	V_{IN} max1	CL, DI, CE	0 to V_{CC} + 0.3	V
	V_{IN} max2	L5dBIN, R5dBIN, L1dBIN, R1dBIN	V_{EE} – 0.3 to V_{DD} + 0.3	V
	V_{IN} max3	S	V_{CC} – 0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max	Ta ≤ 75°C	250	mW
Operating temperature	Topr		–30 to +75	°C
Storage temperature	Tstg		–40 to +125	°C

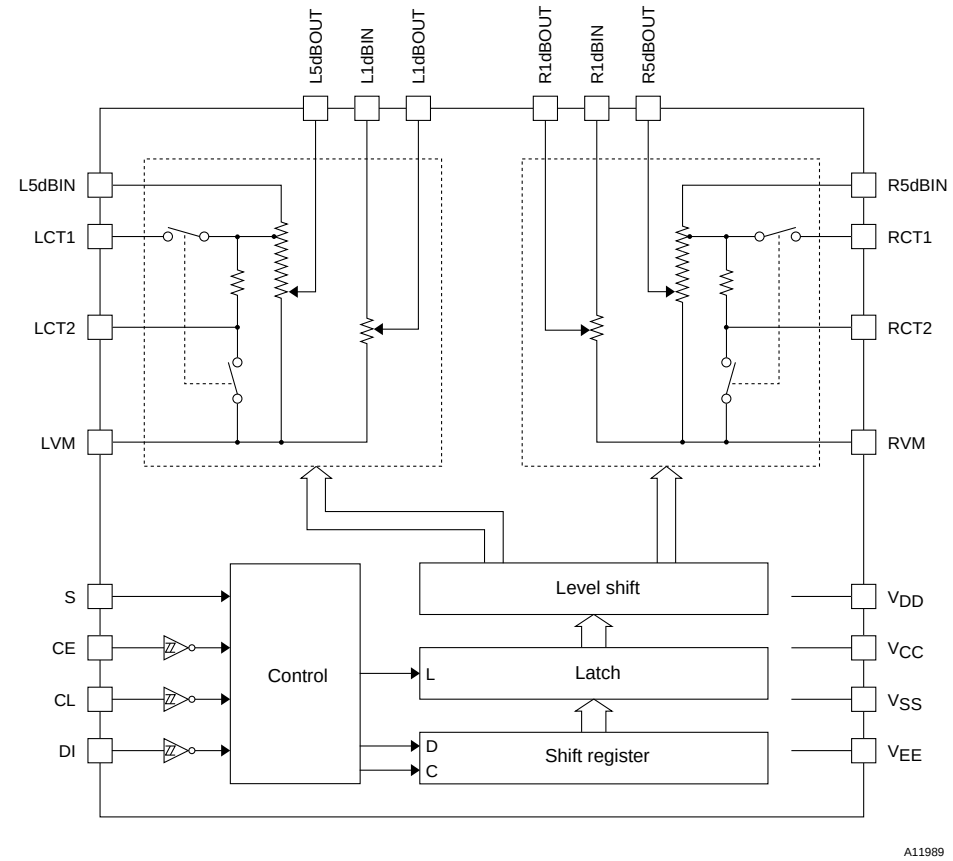
Allowable Operating Ranges at Ta = –30 to +75°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}	V_{DD}	V_{CC} + 4.5		16	V
	V_{EE}	V_{EE}	–16		0	V
	V_{CC}	V_{CC}	4.5	5	5.5	V
High-level input voltage	$V_{IH}1$	CL, DI, CE	0.8 V_{CC}		V_{CC}	V
	$V_{IH}2$	S	$0.8 \times (V_{DD} - V_{CC}) + V_{CC}$		V_{DD}	V
Low-level input voltage	$V_{IL}1$	CL, DI, CE	V_{SS}		0.2 V_{CC}	V
	$V_{IL}2$	S	V_{CC}		$0.2 \times (V_{DD} - V_{CC}) + V_{CC}$	V
Input voltage amplitude	V_{IN}	L5dBIN, R5dBIN, L1dBIN, R1dBIN	V_{EE}		V_{DD}	Vp-p
Input pulse width	tøW	CL	1			µs
Setup time	t_{setup}	CL, DI, CE	1			µs
Hold time	t_{hold}	CL, DI, CE	1			µs
Operating frequency	fopg	CL			500	kHz

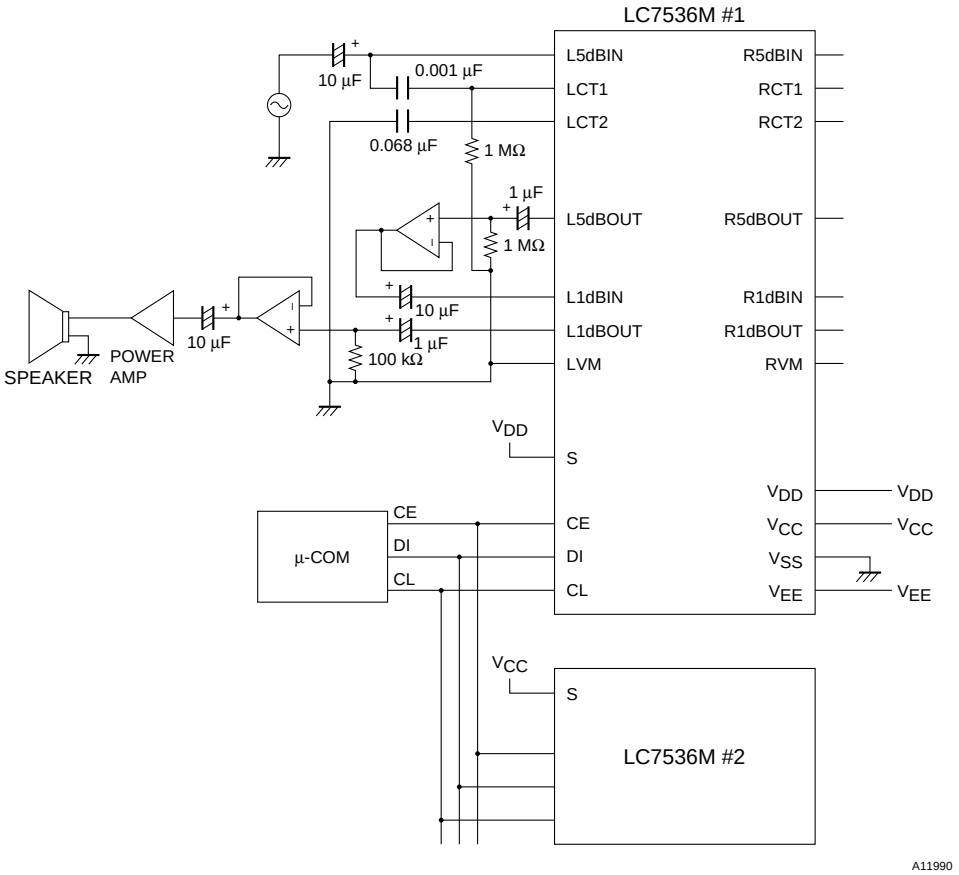
Electrical Characteristics at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Total harmonic distortion	THD1	V_{IN} = 1 Vrms, f = 1 kHz, all controls flat overall, $V_{DD} - V_{EE}$ = 32 V		0.004		%
	THD2	V_{IN} = 0.1 Vrms, f = 1 kHz, all controls flat overall, $V_{DD} - V_{EE}$ = 32 V		0.02		%
Crosstalk	C_T	V_{IN} = 1 Vrms, f = 1 kHz, $V_{DD} - V_{EE}$ = 32 V, All controls flat overall, Rg = 1 kΩ		–75	–60	dB
Output at maximum attenuation	Vo min	V_{IN} = 1 V rms, f = 20 kHz, volume control set at –∞, $V_{DD} - V_{EE}$ = 32 V		–98		dB
Output noise voltage	V_N	All controls flat overall, Rg = 1 kΩ, IHF–A, $V_{DD} - V_{EE}$ = 32 V		2	10	µV
Total resistance	Rvol1	The 5-dB step volume block		75		kΩ
	Rvol2	The 1-dB step volume block		20		kΩ
Output off leakage current	I_{OFF}	L5dBIN, R5dBIN, LCT1, RCT1, LCT2, RCT2, L5dBOUT, R5dBOUT, L1dBIN, R1dBIN, L1dBOUT, R1dBOUT, LVM, RVM	–10		+10	µA
High-level input current	I_{IH}	CL, DI, CE, $V_{IN} = V_{CC}$			+10	µA
Low-level input current	I_{IL}	CL, DI, CE, $V_{IN} = V_{SS}$	–10			µA
Current drain	I_{DD}	V_{DD} = 16 V			1	mA
	I_{CC}	V_{DD} = 5.5 V			1	mA

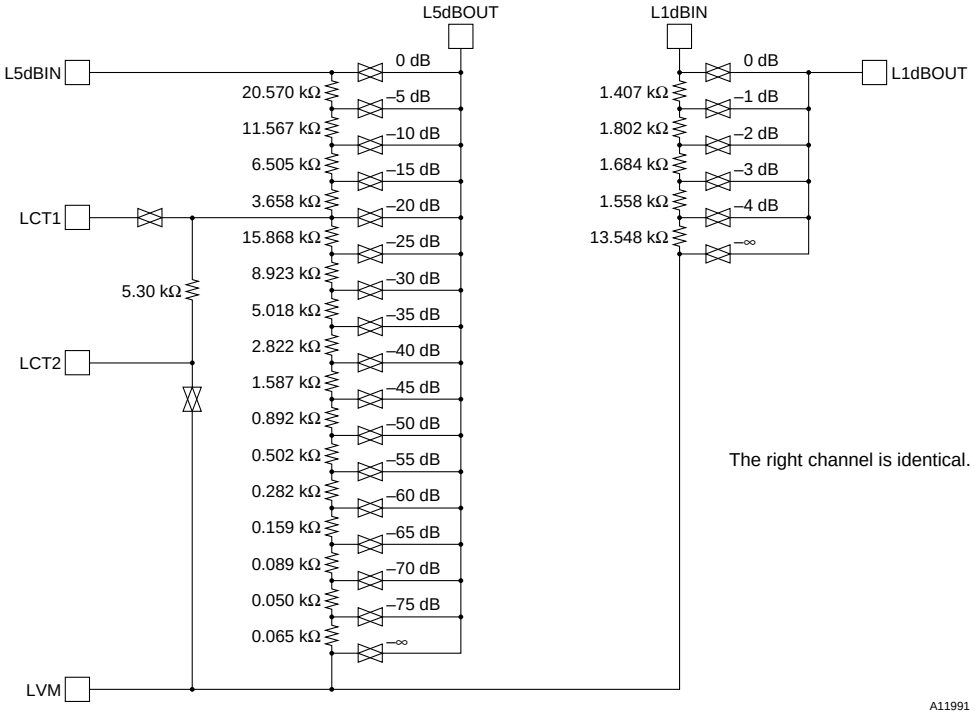
Equivalent Circuit



Sample Application Circuit

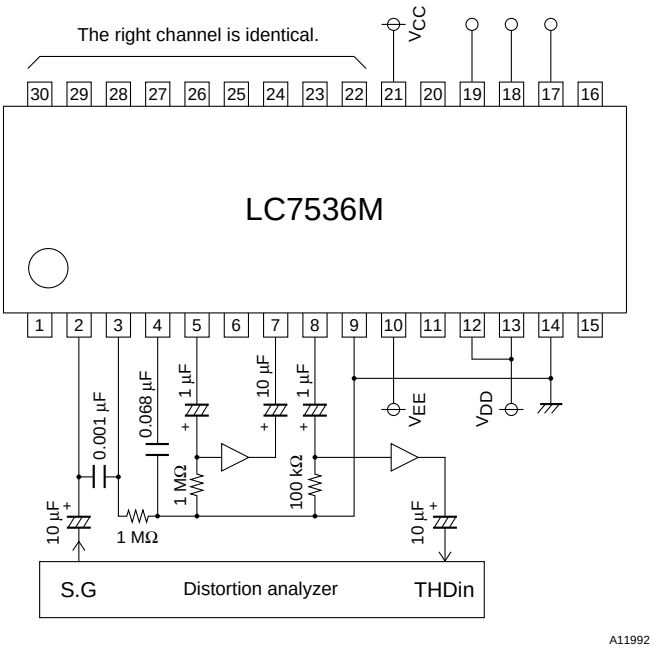


Internal Resistor Equivalent Circuit

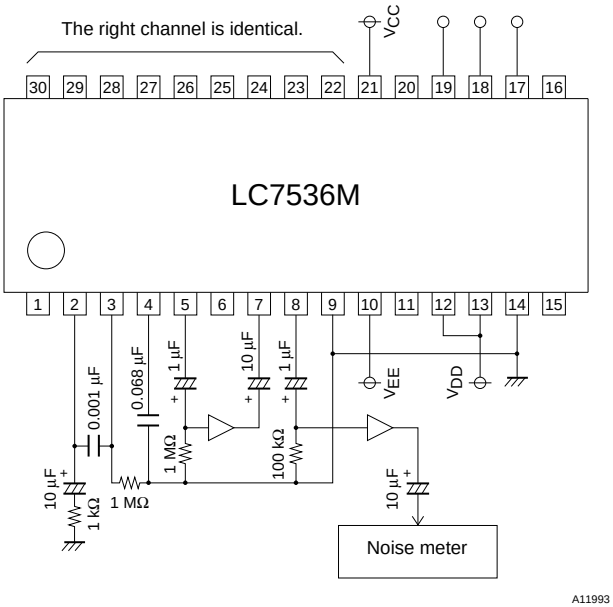


Test Circuit

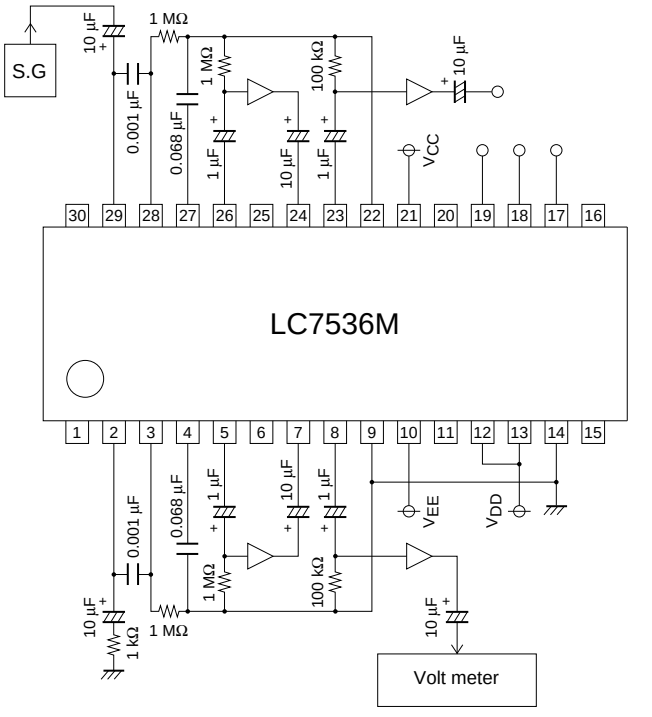
• Total harmonic distortion



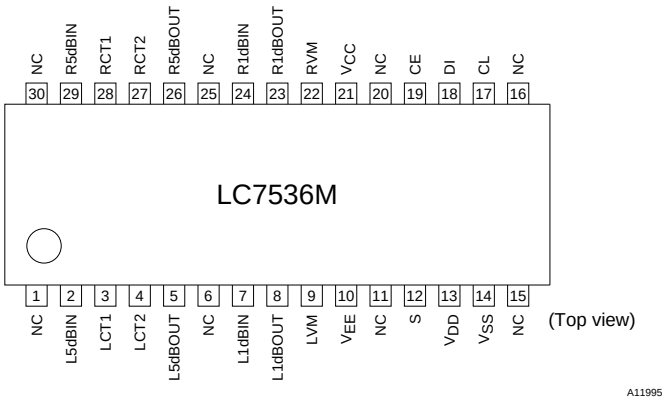
• Output noise voltage



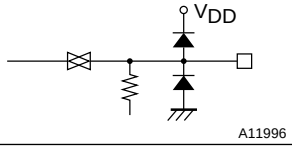
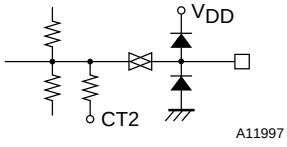
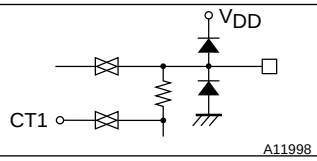
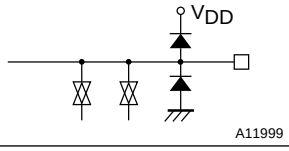
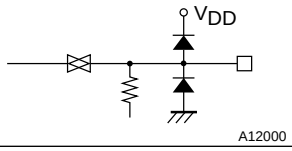
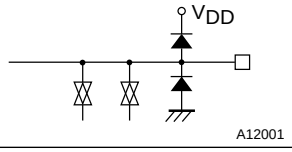
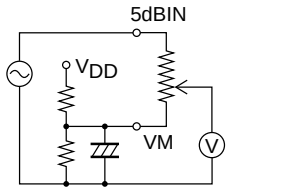
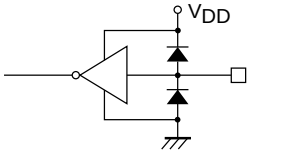
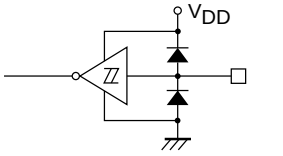
• Crosstalk



Pin Assignment

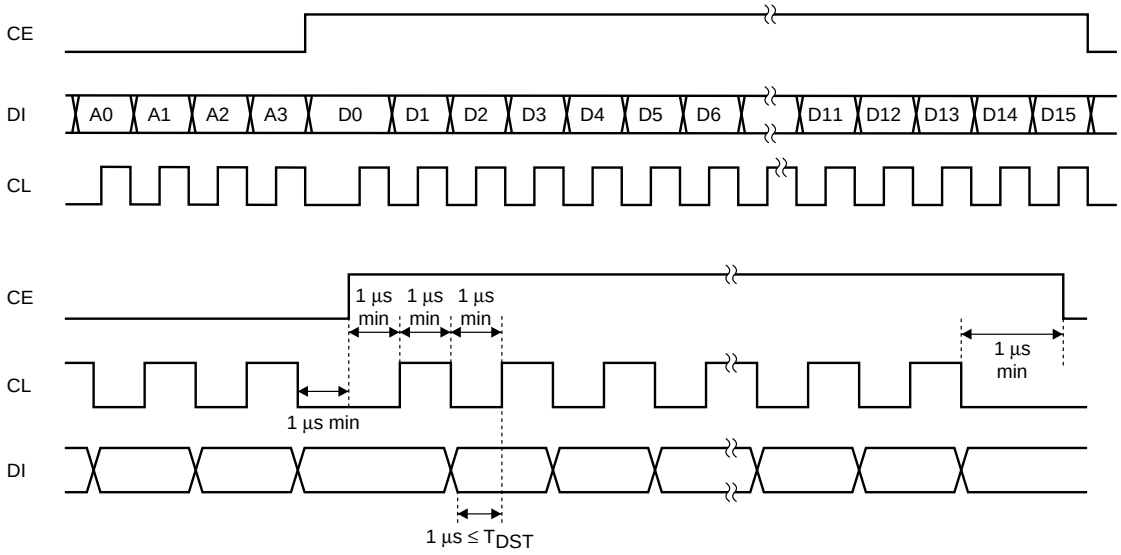


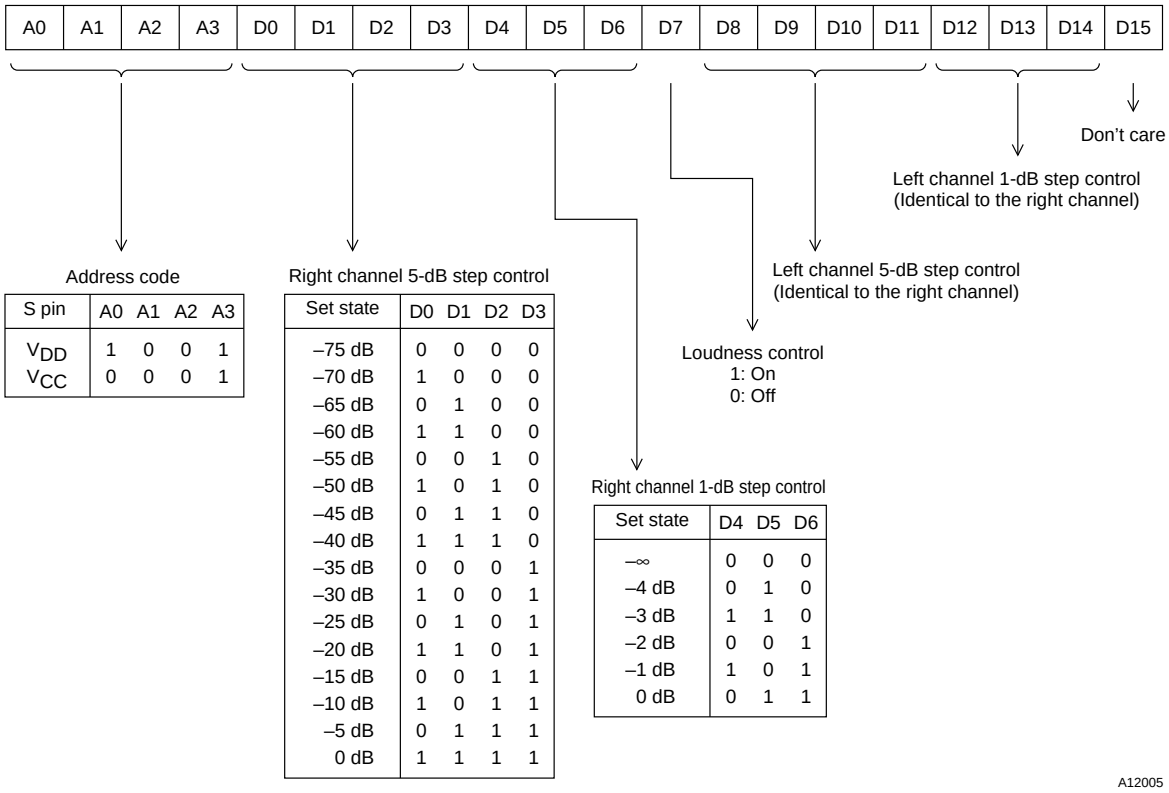
Pin Functions

Pin No.	Pin	Function	Equivalent circuit
2 29	L5dBIN R5dBIN	• 5-dB step attenuator inputs These inputs must be driven by low-impedance circuits.	
3 28	LCT1 RCT1	• Loudness circuit connections Connect high-band compensation capacitors between the CT1 and 5dBIN pins, and connect low-band compensation capacitors between the CT2 and VM pins.	
4 27	LCT2 RCT2		
5 26	L5dBOUT R5dBOUT	• 5-dB step attenuator outputs These signals should be received by loads of about 47 kΩ to 1 MΩ.	
7 24	L1dBIN R1dBIN	• 1-dB step attenuator inputs These inputs must be driven by low-impedance circuits.	
8 23	L1dBOUT R1dBOUT	• 1-dB step attenuator outputs These signals should be received by loads of about 47 kΩ to 1 MΩ.	
9 22	LVM RVM	• Common pins for the volume controls. The printed circuit board pattern for these pins should be designed to have as low an impedance as possible. Since LVM, RVM, and V_{SS} are not connected internally in the IC, they may be connected to separate external circuits that meet their individual specifications. Since the capacitors between the VM pins and the power supply when a single power supply is used become the residual resistance components at maximum attenuation, care is required in determining the values of these capacitors.	
12	S	• Selects the address code of data during formatted. When this pin is connected to V_{DD}, the IC accepts data when the address code is 9, and when connected to V_{CC}, it accepts data when the address code is 8.	
17 18 19	CL DI CE	• Inputs for the serial data that controls the IC. The input signals must have an amplitude of 0 to 5 V.	
10 13 14 21	V_{EE} V_{DD} V_{SS} V_{CC}	• Power supply connections. These pins must be connected to the corresponding power supply. Applications must be designed so that V_{CC} is not applied before V_{DD}.	
1, 6, 11, 15, 16, 20, 25, 30	NC	• Unused pins. These pins must be left open.	

Control System Timing and Data Format

To control the LC7536M, apply the stipulated data signals to the CL, DI, and CE pins. The data consists of 20 bits, of which 4 bits are the address and 16 bits are the data.



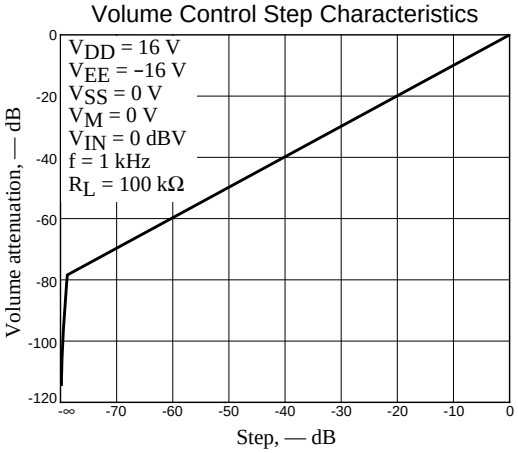


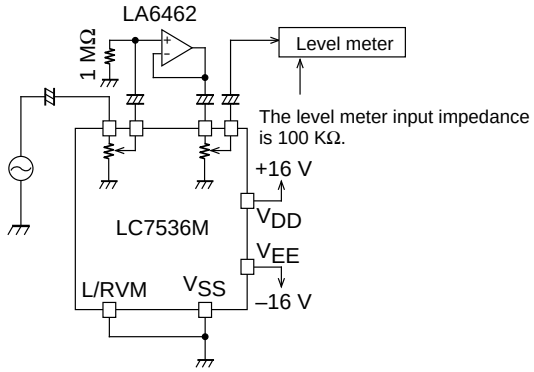
S pin	A0	A1	A2	A3
V_{DD}	1	0	0	1
V_{CC}	0	0	0	1

Set state	D0	D1	D2	D3
–75 dB	0	0	0	0
–70 dB	1	0	0	0
–65 dB	0	1	0	0
–60 dB	1	1	0	0
–55 dB	0	0	1	0
–50 dB	1	0	1	0
–45 dB	0	1	1	0
–40 dB	1	1	1	0
–35 dB	0	0	0	1
–30 dB	1	0	0	1
–25 dB	0	1	0	1
–20 dB	1	1	0	1
–15 dB	0	0	1	1
–10 dB	1	0	1	1
–5 dB	0	1	1	1
0 dB	1	1	1	1

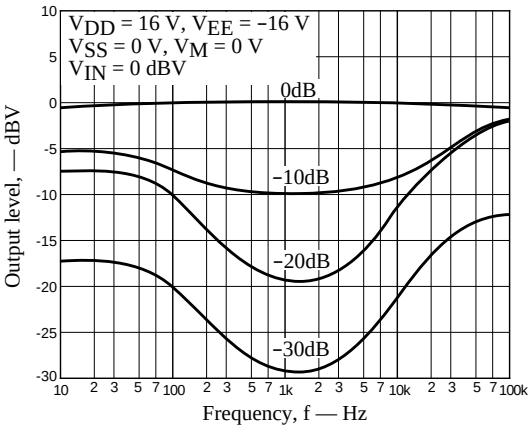
Set state	D4	D5	D6
–∞	0	0	0
–4 dB	0	1	0
–3 dB	1	1	0
–2 dB	0	0	1
–1 dB	1	0	1
0 dB	0	1	1

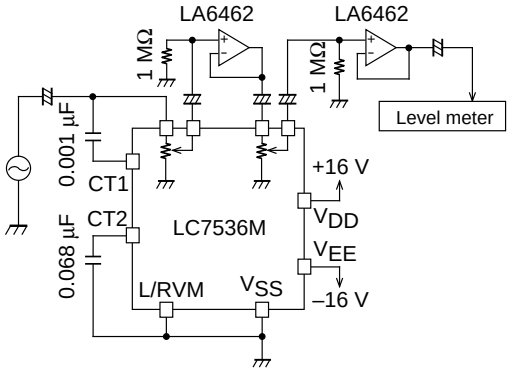
Volume Control Step Characteristics



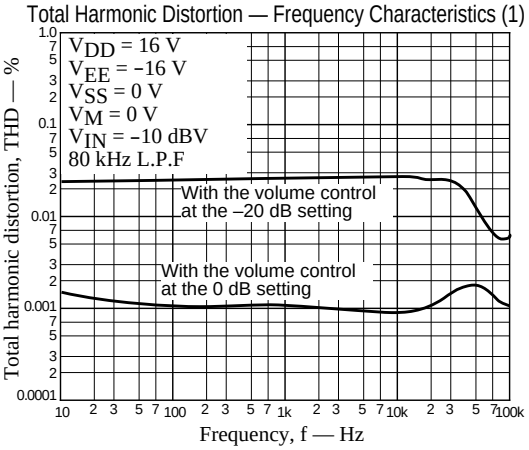


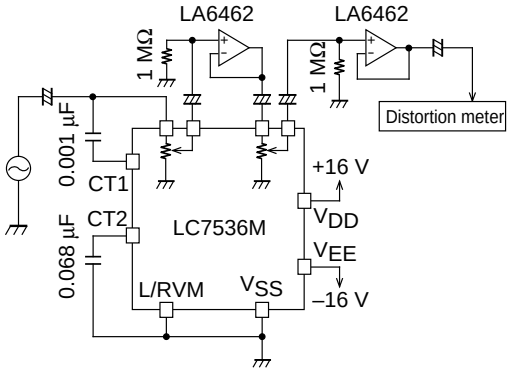
Loudness Characteristics



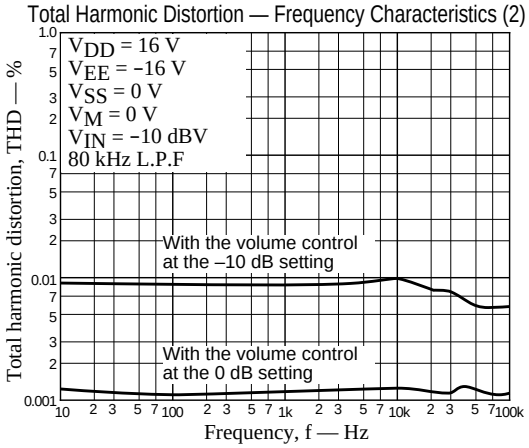


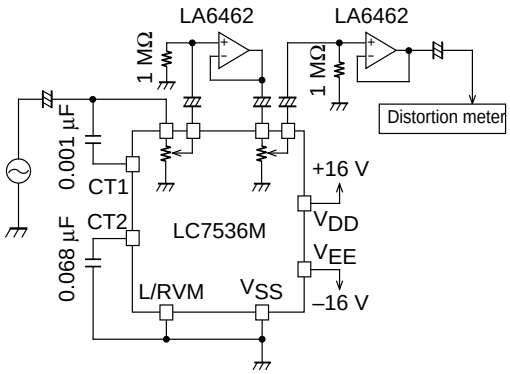
Total Harmonic Distortion — Frequency Characteristics (1)



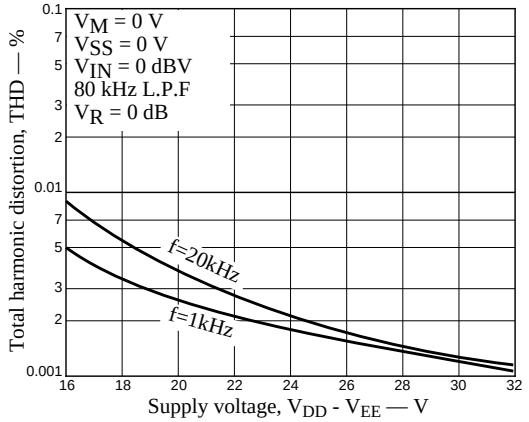


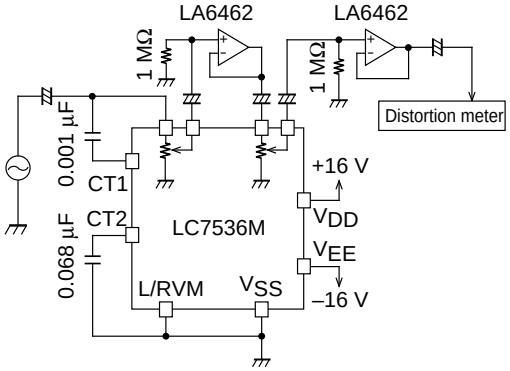
Total Harmonic Distortion — Frequency Characteristics (2)



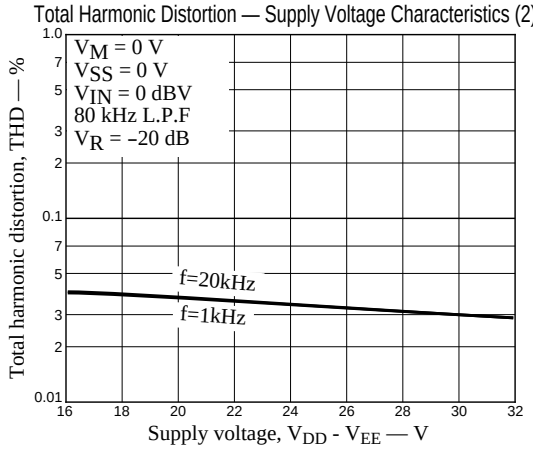


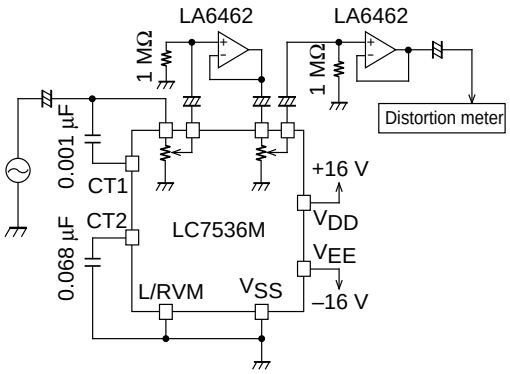
Total Harmonic Distortion — Supply Voltage Characteristics (1)



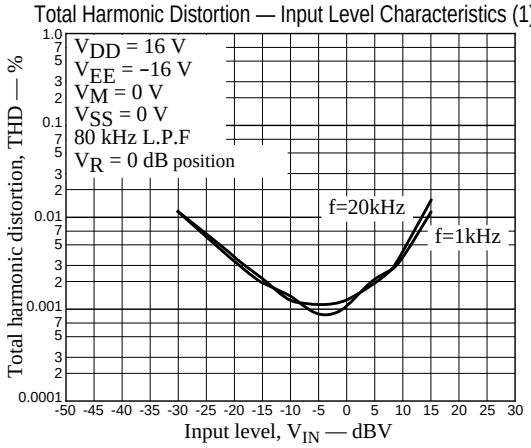


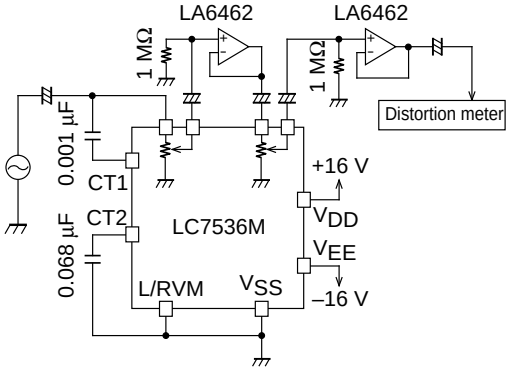
Total Harmonic Distortion — Supply Voltage Characteristics (2)



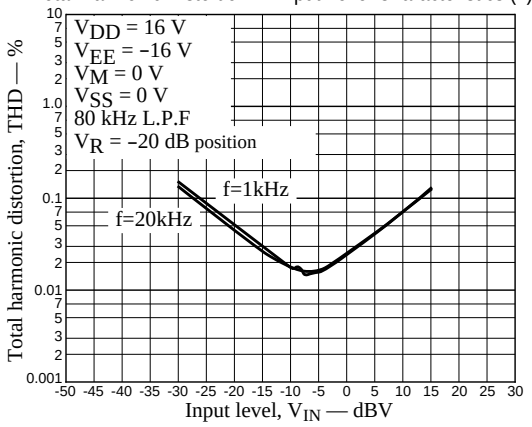


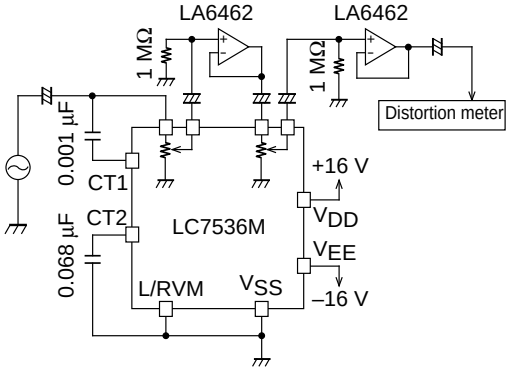
Total Harmonic Distortion — Input Level Characteristics (1)





Total Harmonic Distortion — Input Level Characteristics (2)





Usage Notes

- The states of the internal analog switches are undefined when power is first applied. Applications should apply muting to the analog signal system externally until control data has been transferred to the IC.
- To prevent noise from the high-frequency digital signals on the CL, DI, and CE pin lines from entering the analog signal system, either shielded lines should be used for these lines, or they should be covered by the ground pattern.