Ordering number: ENN6522

Monolithic Linear IC

LA17000M

Tuner System IC with Built-in PLL for Car Audio Applications

Overview

The LA17000M is an all-in-one car tuner IC that incorporates a PLL frequency synthesizer and all functions of an AM/FM tuner in a single chip. By combining two chips, a PLL (LC72144 equivalent) and an FM tuner IC (LA1781M equivalent) into a single chip (*PLL + AM (up conversion) + FMFE + IF + NC + MCP + MRC), and as a result of optimal chip partitioning, the LA17000M improves the performance of car tuner systems, eliminates adjustments, and provides high reliability, all at a lower cost.

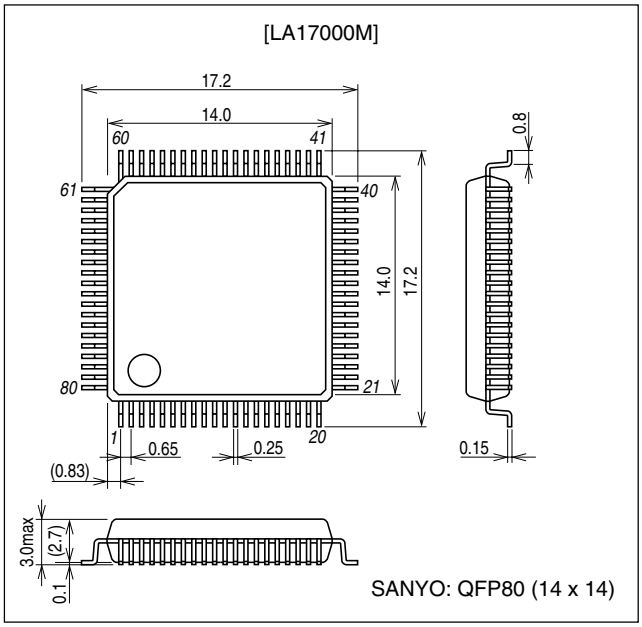
Features

- PLL on chip
  - ADC (6 bits, 1 channel)
  - IF counter and I/O port on chip permit simplification of the interface.
  - Supports AM double conversion.
- Enhanced noise countermeasures
  - Excellent tri-signal characteristics
  - Improved medium and weak electric field NC characteristics
  - Improved separation characteristics
  - Anti-birdie filter on chip (analog/digital output)
  - Multipath sensor output (analog/digital output)
- Cost-saving features
  - AM double conversion (Up conversion method)
  - Enhanced FM-IF circuit
    (When there is interference from adjacent frequencies, the software handles switching of the CF between wide and narrow automatically.)
  - Because deviations in IF gain are only 1/3 that of earlier devices, adjustment is simplified when this IC is incorporated into a set; this IC also includes a shifter pin for VSM adjustment.
- Suited for smaller devices
  - Permits high-frequency signal line processing in a tuner pack.
  - Easily conformes to FCC standards

Package Dimensions

unit: mm

3255-QFP80



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Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC}1$ max	Pins 6, 56, and 77	8.7	V
	$V_{CC}2$ max	Pins 7, 61, 70, 75, and 76	12.0	V
	V_{DD} max	Pin 19	6.0	V
Allowable power dissipation	Pd max	Ta ≤ 85°C, * With board	950	mW
Operating temperature	Topr		–40 to +85	°C
Storage temperature	Tstg		–40 to 150	°C

* Specified board: $114.3 \times 76.1 \times 1.6$ mm^3, glass epoxy

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}	Pins 6, 7, 56, 61, 70, 75, 76, and 77	8.0	V
		Pin 19	5.0	V
Operating supply voltage range	V_{CC} op		7.5 to 8.5	V
	V_{DD} op		4.5 to 5.5	V

Tuner Block

Operating Characteristics at Ta = 25°C, V_{CC} = 8.0 V, V_{DD} = 5.0 V, in the specified Test Circuit

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[FM characteristics] FM IF input						
Current drain	I_{CCO}-FM	No input, I56 + I61 + I70 + I75 + I76 + I79	60	98	110	mA
Demodulated output		10.7 MHz, 100 dBμV, 1 kHz, 100%mod, pin 15 output	220	330	445	mVrms
Channel balance	CB	10.7 MHz, 100 dBμV, 1 kHz, ratio of pin15 and pin 16	–1	0	+1	dB
Total harmonic distortion	THD-FMmono	10.7 MHz, 100 dBμV, 1 kHz, 100% mod, pin 15		0.4	1	%
Signal-to-noise ratio IF	S/N-FM IF	10.7 MHz, 100 dBμV, 1 kHz, 100% mod, pin 15	75	82		dB
AM suppression ratio IF	AMR IF	10.7 MHz, 100 dBμ, 1 kHz, fm = 1 kHz, pin 15 at 30% AM	55	68		dB
Muting attenuation	Att-1	10.7 MHz, 100 dBμV, 1 kHz, attenuation on pin 15 when V49 = 0 → 2 V	3	8	13	dB
	Att-2	10.7 MHz, 100 dBμV, 1 kHz, attenuation on pin 15 when V49 = 0 → 2 V *Note 1	13	18	23	dB
	Att-3	10.7 MHz, 100 dB μV, 1 kHz, attenuation on pin 15 when V49 = 0 → 2 V *Note 2	26	31	36	dB
Separation	Separation	10.7 MHz, 100 dBμ, L + R = 90%, pilot = 10%, pin 15 output ratio	25	35		dB
Stereo ON level	ST-ON	Pilot modulation at which V17 < 0.5 V		4.1	6.6	%
Stereo OFF level	ST-OFF	Pilot modulation at which V17 > 3.5 V	1.2	3.1		%
Main total harmonic distortion	THD-Main L	10.7 MHz, 100 dBμV, L + R = 90%, pilot = 10%, pin 15		0.4	1.2	%
Pilot cancellation	PCAN	10.7 MHz, 100 dBμV, pilot = 10%, pin 15 signal/PILOT-LEVEL leak DIN AUDIO	12	22		dB
SNC output attenuation	AttSNC	10.7 MHz, 100 dBμV, L – R = 90%, pilot = 10%, V44 = 3 V → 0.6 V, pin 15	1	5	9	dB
HCC output attenuation	AttHCC-1	10.7 MHz, 100 dBμV, 10 kHz, L + R = 90%, pilot = 10%, V45 = 3 V → 0.6 V, pin 15	1	5	9	dB
	AttHCC-2	10.7 MHz, 100 dBμV, 10 kHz, L + R = 90%, pilot = 10%, V45 = 3 V → 0.1 V, pin 15	6	10	14	dB

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input limiting voltage	V_{IN}-LIM	10.7 MHz, 100 dBμV, 30% mod, IF input that decreases the input reference output by –3 dB	29	36		dBμV
Muting sensitivity	V_{IN}-MUTE	IF input level non-mod when V49 = 2 V	19	27	35	dBμV
SD sensitivity	SD-sen1 FM	IF input non-mod (at least 100 mVrms) at which the IF count buffer output turns on	48	56	64	dBμV
	SD-sen2 FM		48	56	64	dBμV
IF counter buffer output	$V_{IFBUFF-FM}$1	10.7 MHz, 100 dBμV, non-mod, pin 38 output, during SEEK	145	245	330	mVrms
	$V_{IFBUFF-FM}$2	10.7 MHz, 100 dB μV, non-mod, pin 38 output, during RDS mode	145	245	330	mVrms
Signal meter output	V_{SM} FM-1	No input, pin 42 DC output non-mod	0.0	0.1	0.3	V
	V_{SM} FM-2	50 dBμ, pin 42 DC output non-mod	0.65	1.6	2.4	V
	V_{SM} FM-3	70 dBμ, pin 42 DC output non-mod	2.4	3.2	4.2	V
	V_{SM} FM-4	100 dBμ, pin 42 DC output non-mod	4.9	5.8	6.5	V
Muting bandwidth	BW-MUTE	100 dBμV, when V49 = 2 V Bandwidth non-mod	140	210	280	kHz
Muting drive output	V_{MUTE}-100	100 dBμV, 0 dBμ, pin 49 DC output non-mod	0.00	0.1	0.3	V
[FM FE Block]						
N-AGC on input	V_{NAGC}	83 MHz, non-mod, input at which pin 2 is 2.0 V or less	72	79	86	dBμV
W-AGC on input	V_{WAGC}	83 MHz, non-mod, input at which pin 2 is 2.0 V or less (when KEYED-AGC is 4.0 V)	90	97	104	dBμV
Conversion gain	A. V1	83 MHz, 80 dBμ, non-mod, FECF output	9	13	17	dB
	A. V2	83 MHz, 80 dBμ, non-mod, 5 V applied to CF (pin 10), FECF output	13	17	21	dB
Oscillator buffer output	$V_{OSCBUFFFM}$	No input, pin 5 output	51	67	102	mVrms
[NC Block] NC input (pin 30)						
Gate time	τGATE	f = 1 kHz, 1 μs, 100 mVp-o pulse input		15		μs
Noise sensitivity	SN	1 kHz, 1 μs pulse input that starts noise canceller operation. Measured at Pin 30.		18		mVp-o
[MRC Block]						
MRC output	V_{MRC}	V42 = 5 V	2.1	2.25	2.4	V
MRC operating level	MRC-ON	Input level on pin 48 that is below pin 42 = 5 V and pin 43 = 2 V, f = 70 kHz	22	33	44	mVrms
MRC sensor output	V_{MRC}-sensor1	V42 = 5 V, pin 34 output		1.5	1.9	V
	V_{MRC}-sensor2	V42 = 5 V, pin 48 output, f = 70 kHz, 100 mVrms	2.1	2.9		V
[AM Characteristics] AM ANT input						
Practical sensitivity	S/N-30	1 MHz, 30 dBμV, fm = 1 kHz, 30% mod, pin 15	15			dB
Detection output	V_O-AM	1 MHz, 74 dBμV, fm = 1 kHz, 30% mod, pin 15	105	160	220	mVrms
AGC-F.O.M	$V_{AGC-FOM}$	1 MHz, 74 dBμV, output reference, input width at which output drops by 10 dB, pin 15	50	55	60	mVrms
Signal-to-noise ratio	S/N-AM	1 MHz, 74 dBμV, fm = 1 kHz, 30% mod	47	52		dB
Total harmonic distortion	THD-AM	1 MHz, 74 dBμV, fm = 1 kHz, 80% mod		0.5	1.2	%
Signal meter output	V_{SM}AM-1	1 MHz, 30 dBμV, non - mod	0.6	1	1.4	V
	V_{SM}AM-2	1 MHz, 120 dBμV, non - mod	3.4	4.5	5.9	V
Oscillator buffer output	$V_{OSCBUFF}$AM-1	No input, pin 5 output	170	210		mVrms
Wideband AGC sensitivity	W-AGCsen1	1.4 MHz, input when V62 = 0.7 V	87	93	99	dBμV
	W-AGCsen2	1.4 MHz, input when V62 = 0.7 V (during SEEK)	78	84	90	dBμV

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
SD sensitivity	SD-sen1AM	1 MHz, ANT input level at which IF count output turns on	27	33	39	dBμV
	SD-sen2AM	1 MHz, ANT input level at which SD pin turns on	27	33	39	dBμV
IF buffer output	$V_{IFBUFF-AM}$	1 MHz, 74 dBμV, non-mod, pin 38 output	150	220		mVrms

PLL Block

Allowable Operating Ranges at Ta = –40 to +85°C, V_{DD} = 5 V, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
High-level input voltage	$V_{IH}1$	CE, CL, DI, I/O-1, I/O-2	2.2		V_{DD} + 0.3	V
Low-level Input voltage	$V_{IL}1$	CE, CL, DI, I/O-1, I/O-2, SDSTSW	0		0.8	V
Output voltage	V_O1	DO	0		6.5	V
	V_O2	I/O-1, I/O-2	0		13	V
Input amplitude	$f_{IN}1$	X_{IN}; Sine wave, capacitor coupled	1		8	MHz
	$f_{IN}2$	PLL_{IN}; Sine wave, capacitor coupled	10		160	MHz
	$f_{IN}3$	HCTR; Sine wave, capacitor coupled	0.4		25	MHz
Guaranteed crystal oscillator ranges	X'tal	X_{IN}, X_{OUT}; CI ≤ 70 Ω (X'tal: 10.25, 10.35 MHz); Note 1	10.1		10.5	MHz
Input amplitude	$V_{IN}1$	X_{IN}	200		1500	mVrms
	$V_{IN}2$-1	PLL_{IN}; 10 ≤ f < 130 MHz; Note 2	40		1500	mVrms
	$V_{IN}2$-2	PLL_{IN}; 130 ≤ f <160 MHz; Note 2	70		1500	mVrms
	$V_{IN}3$-1	HCTR; 0.4 ≤ f < 25 MHz: Serial data; CTC = 0: Note 3	40		1500	mVrms
	$V_{IN}3$-2	HCTR; 8 ≤ f <12MHz: Serial data; CTC = 1: Note 4	70		1500	mVrms
Data setup time	t_{SU}	DI, CL: Note 5	0.45			μs
Data hold time	t_{HD}	DI, CL: Note 5	0.45			μs
Clock low-level time	t_{CL}	CL: Note 5	0.45			μs
Clock high-level time	t_{CH}	CL: Note 5	0.45			μs
CE wait time	t_{EL}	CE, CL: Note 5	0.45			μs
CE setup time	t_{ES}	CE, CL: Note 5	0.45			μs
CE hold time	t_{EH}	CE, CL: Note 5	0.45			μs
Data latch change time	t_{LC}	Note 5			0.45	μs
Data output time	t_{DC}	DO, CL; Dependent on pull-up resistance, board capacity: Note 5			0.2	μs
	t_{DH}	DO, CL; Dependent on pull-up resistance, board capacity: Note 5			0.2	μs

Note 1: Recommended CI value for crystal oscillator
CI ≤ 70 Ω (X'tal: 10.25, 10.35 MHz)
However, because the characteristics of the X'tal oscillation circuit depend on the board and circuit constants, we recommend requesting that the X'tal manufacturer perform the evaluation.

Note 2: Refer to the program divider configuration.

Note 3: Serial data: CTC = 0

Note 4: Serial data: CTC = 1

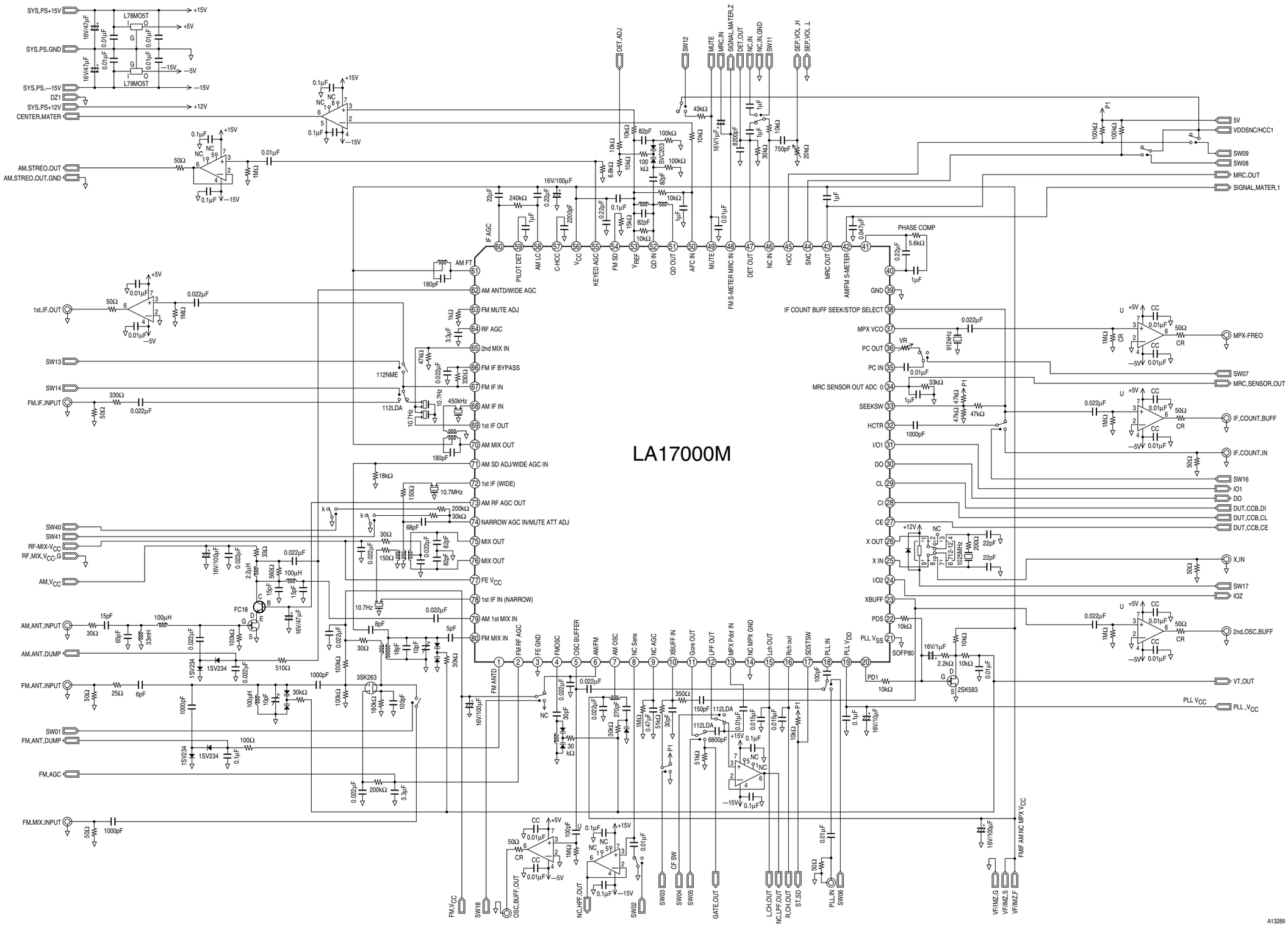
Note 5: Refer to the serial data timing.

PLL Characteristics

Electrical Characteristics at Ta = 25°C, V_{DD} = 5 V, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Built-in feedback resistors	Rf1	X_{IN}		1		MΩ
	Rf2	PLL_{IN}		500		kΩ
	Rf3	HCTR		250		kΩ
Hysterisis width	V_{HIS}	CE, CL, DI		$0.1V_{DD}$		V
High-level output voltage	$V_{OH}1$	PD1, PDS, SEEKSW; I_O = –1 mA	V_{DD}–1.0			V
	$V_{OH}2$	XBUF; I_O = –0.5 mA	V_{DD}–1.5			V
Low-level output voltage	$V_{OL}1$	PD1, PDS, SEEKSW; I_O = –1 mA			1	V
	$V_{OL}2$	XBUFF; I_O = –0.5 mA			1.5	V
	$V_{OL}3$	I/O-1 to I/O-2; I_O = 1.0 mA			0.2	V
		I/O-1 to I/O-2; I_O = 2.5 mA			0.5	V
		I/O-1 to I/O-2; I_O = 5.0 mA			1	V
		I/O-1 to I/O-2; I_O = 9.0 mA			1.8	V
	$V_{OL}4$	DO; I_O = 5.0 mA			1	V
High-level input current	$I_{IH}1$	CE, CL, DI; V_{IN} = 6.5 V			5	μA
	$I_{IH}2$	I/O-1 to I/O-2; V_{IN} = 13 V			5	μA
	$I_{IH}3$	X_{IN}; V_{IN} = V_{DD}	2		11	μA
	$I_{IH}4$	PLL_{IN}; V_{IN} = V_{DD}	4		22	μA
Low-level input current	$I_{IL}1$	CE, CL, DI; V_{IN} = 0 V			5	μA
	$I_{IL}2$	I/O-1 to I/O-2; V_{IN} = 0 V			5	μA
	$I_{IL}3$	X_{IN}; V_{IN} = 0 V	2		11	μA
	$I_{IL}4$	PLL_{IN}; V_{IN} = 0 V	4		22	μA
Output off leakage current	$I_{OFF}1$	I/O-1 to I/O-2; V_O = 13 V			5	μA
	$I_{OFF}2$	DO; V_O = 6.5 V			5	μA
High-level 3-state off leakage current	I_{OFFH}	PD1, PDS; V_{IN} = V_{DD}		0.01	200	nA
Low-level 3-state off leakage current	I_{OFFL}	PD1, PDS; V_{IN} = 0 V		0.01	200	nA
Input capacitance	C_{IN}			6		pF
A/D converter linearity error	Err	MRC SENSOR AUTO ADJ (MOS)	–0.5		+0.5	LSB
Pull-down transistor on resistance	Rpd1	PLL_{IN}	80	200	600	kΩ
Supply current	$I_{DD}1$	V_{DD}; X'tal = 10.25 MHz, $f_{IN}2$ = 160 MHz, $V_{IN}2$ = 70 mVrms, $f_{IN}3$ = 25 MHz, $V_{IN}3$ = 40 mVrms		10	15	mA
	$I_{DD}2$	V_{DD}; PLL block halt (PLL INHIBIT), X'tal OSC operation (10.25 MHz)		5	10	mA
	$I_{DD}3$	V_{DD} ; PLL block halt, X'tal OSC halt			3	mA

Test Circuit



[FM IF Selectivity Switching Circuit]

Features

1) Comprises an FM/AM one-chip system.
2) Up conversion method is adopted for AM.
3) Uses an IF filter with a center frequency that is the same as the middle frequency of FM.
4) Uses a narrowband filter in AM mode.
5) Uses a narrowband filter in FM mode only during SEEK or when there is interference from adjacent frequencies.
6) Uses a wideband filter for normal reception in FM mode.
7) For an RDS AF search, switches to a narrowband filter and detects SD.
8) High sensitivity for detecting interference from adjacent frequencies.

Advantages

1) This FM/AM one-chip tuner system (an IC that includes a microcontroller interface) allows for improved adjacent frequency interference characteristics without increased cost.
2) Prevents SD and IF count misdetection (station detection) during seek search, RDS AF search, and auto memory operations.
3) Permits adoption of an IC for certain functions without increasing the number of IC pins.
4) CF selectivity can be switched by the software in the microcontroller that controls the tuner, making it easy to achieve performance differentiation through the software.
   (The software can freely set the CF switching timing and conditions.)
5) Detects the radio wave status in the field through detection of SD, desired station field intensity, IF count output, and adjacent station field intensity. This IC offers improved adjacent frequency interference characteristics by switching the CF automatically when interference is being generated from an adjacent frequency.

[IF Band Switching Circuit]

Purpose

This AM/FM one-chip tuner IC automatically switches the FM selectivity, prevents misdetection during SEEK operations, and offers improved adjacent frequency interference characteristics without any increase in cost.

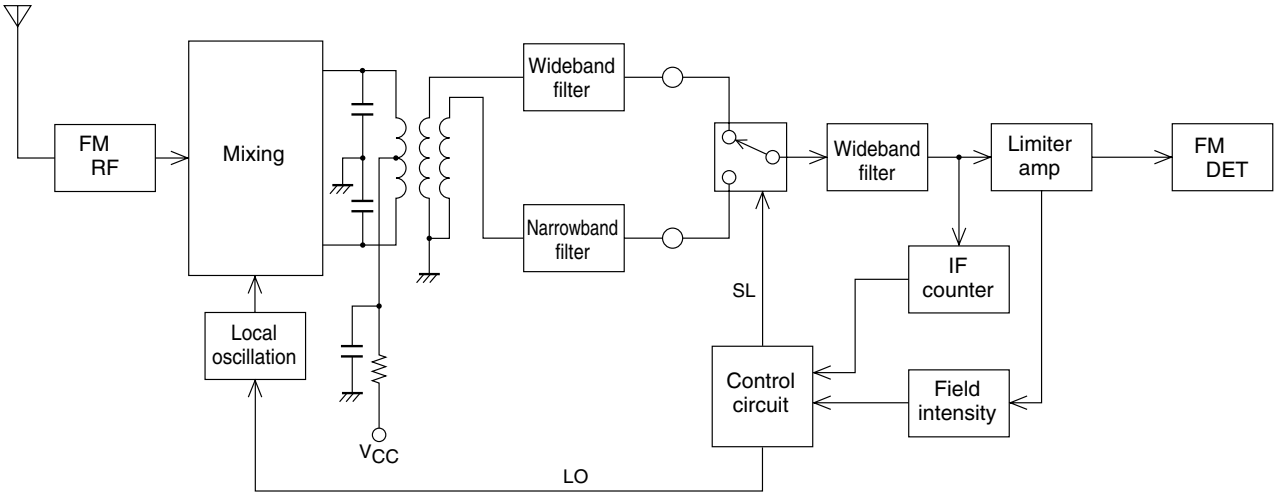
New Technological Features

1. Comprises an AM/FM one-chip IC.
2. Because the narrowband CF that is used by the AM UP conversion system is also used for FM, additional external components required by earlier systems can be eliminated.
3. Uses a wideband CF during normal FM reception for high sound quality.
4. Uses a narrowband CF for AM reception, and if interference is being generated from adjacent frequencies during FM reception.
5. Uses a narrowband CF during SEEK and RDSAF search operations, preventing misdetection of SD and IF count due to adjacent stations.
6. CF switching is performed at the first IF amp input, and the amp gain is adjusted automatically to a suitable level according to the CF band form AM/FM or FM.
7. Switching of the CF input and the first IF amp gain is controlled by a microcontroller through the interface. The pins that are controlled are connected to the I/O ports of the microcontroller, and are controlled by the microcontroller's internal software.
8. Detection of adjacent frequency interference during FM reception is based on S-meter output, SD, and IF count output. The IF count buffer frequency fluctuates when interference is being generated from adjacent frequencies. This fluctuation is used to make the detection of interference from adjacent frequencies possible. (Related patents have been applied for.)

Conventional Technologies

1. Comprised of a dedicated IC for IF band switching, or of multiple ICs.
2. None of the AM/FM all-in-one chip systems include the functions provided by the LA17000M.
3. Requires a narrowband CF especially for FM, resulting in increased costs. (Does not share the AM narrowband CF.)
4. Because CF switching control is handled by analog circuits or logic circuits, the switching timing can only be controlled through uniform conditions. Control by software is not possible.

Conceptual Diagram of the FM-IF Band Switching System



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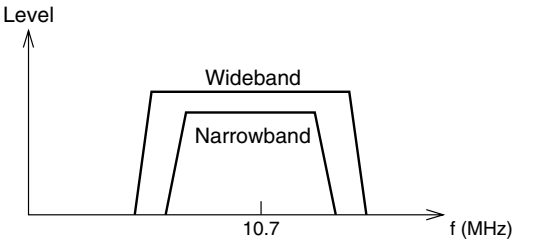

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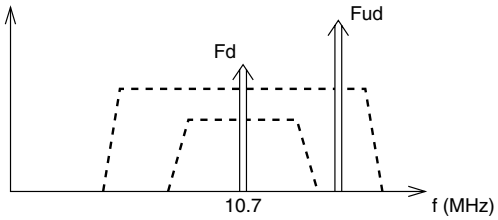

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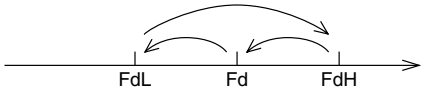

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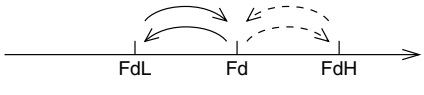

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I/O Port Assignment Table

I/O-0 DI data	OUTPUT PLL output port	L: Reception mode H: Seek mode
	INPUT PLL input port	OPEN: RDS
I/O-1		Unused
I/O-2 DI data	OUTPUT PLL output port	H: Dx mode L: Lo mode
I/O-3 DO data	INPUT I/O-3 = 0 (input port) OUT3 = 1 (OPEN or high) PLL input port Cannot be set as output port	When reception mode is set H: Monaural L: Stereo When seek mode is set H: SD ON L: SD OFF

The MRC sensor reads DO data from the PLL microcontroller's 6-bit A/D converter.

Currently, aside from the CCB data lines, only three lines are connected to the controller microcontroller: CF/SW, AUDIO mute, and AM/FM band switching port.

Selectivity Switching Evaluation Software State-based Data Switching Table

I/O port state \ Tuner processing		Seek	Manual preset	Receiving	Remarks
CF switching	WIDE		○	○	
	NARROW	○	○	○	
AUDIO mute output	ON	○	○		Switchable but fixed by software
	OFF			○	Switchable but fixed by software
Lo/Dx	Lo	○	○	○	Processing is performed according to the setting
	Dx	○	○	○	Processing is performed according to the setting
Mode switching	Seek mode	○		○	I/O-3 is SD output
	Reception mode		○	○	I/O-3 is monaural/stereo output
	RDS mode			○	I/O-3 is SD output
IF count	Output ON	○		○	Seek mode RDS mode
	Output OFF		○		Reception mode

Additional Settings (Added to the LC72144M)

Output (DI)

	Mode	Settings	When set
Tuner mode switch	Seek mode	DI data IN2 I/O-0 = 1 (output port) OUT0 = 1 (Hi)	For seek
	Reception mode	DI data IN2 I/O-0 = 1 (output port) OUT0 = 0 (Lo)	For seek-stop and for receiving
	RDS mode	DI data IN2 I/O-0 = 0 (input port) OUT0 = 1 (OPEN)	For AF search
Lo/Dx switch	Lo mode	DI data IN2 I/O-2 = 0 (output port) OUT2 = 0 (Lo)	When setting Lo mode
	Dx mode	DI data IN2 I/O-2 = 1 (output port) OUT2 = 1 (Hi)	When setting Dx mode
Hard mute *1	Mute ON	DI data IN2 I/O-0 = 1 (output port) OUT1 = 1 (Hi)	For tuning processing
	Mute OFF	DI data IN2 I/O-0 = 1 (output port) OUT1 = 1 (Lo)	When switching reception mode

Note: *1. Depends on the I/O ports usage.

Input (DO)

		DO data	Conditions
Sensor	Monaural/stereo	OUT data I3 = 1 (Hi) Monaural state OUT data I3 = 0 (Lo) Stereo state	When the tuner mode is set to reception mode *2
	SD	OUT data I3 = 1 (Hi) SD ON OUT data I3 = 0 (Lo) SD OFF	When the tuner mode is set to seek or RDS mode *2
MRC output		OUT data ADC0 AD00 to AD05 6 bit	Start AD conversion and then read after conversion is completed. 3.3 V at 6-bit resolution

Note: *2. I/O-3 = 0 (input port) and OUT3 = 1 (Hi) must already be set in the DI data (IN2) settings.

Other settings

	In the LA17000	Setting	When set
CF switch	Pin 10	Hi: Wide (wideband setting) Lo: Narrow (narrowband setting)	For normal operation When there is interference from adjacent frequencies
Soft mute (AUDIO mute)	Pin 49	Hi: Forced mute Lo: Mute off	When setting mute When cancelling mute
AM/FM switch	Pin 6	Lo: AM Hi: FM	For AM reception For FM reception

Correspondence of Pins Between the LA17000M, the LA1781M, and the LC72144M

LA1781 Pin No.	Pin Function	LA17000M Pin No.	Pin Function	LC72144M Pin No.
1	FN ANTD	1		
2	FM RF AGC	2		
3	FE GND	3		
4	FM OSC	4		
5	AM/FM OSC buff.	5		
6	FE V_{CC}	6		
7	AM V_{CC}	7		
8	Noise AGC-Sense	8		
9	Noise AGC-ADJ	9		
10	AM 2nd OSC	10		
11	Gate Out	11		
12	Memory circuit pin	12		
13	Pilot In	13		
14	NC, MPX GND	14		
15	MPX L-Out	15		
16	MPX R-Out	16		
26	Seek → AM/FM SD Stop → FM ST IND	17	Both I/O-3 and SD/ST-IND	23
		18	FMIN	16
		19	V_{DD}	17
		20	PD1	18
		21	V_{SS}	19
		22	PDS	20
		23	XBUF	22
		24	I/O-2	8
		25	XIN	24
		26	XOUT	1
		27	CE	2
		28	DI	3
		29	CL	4
		30	DO	5
		31	I/O-1	9
		32	HCTR/I-6	11
		33	I/O-0	12
19	MRC sensor output	34	Both ADC0 and MRC sensor output	7
17	Pilot Can. ADJ	35		
18	Pilot Can. ADJ	36		
20	MPX VCO	37		
23	IF count buffer and seek/stop switch	38		
25	GND	39		
21	PHASE COMP.	40		
22	PHASE COMP.	41		
24	AM/FM S-meter	42		
27	MRC OUT	43		

Continued on next page.

Continued from preceding page.

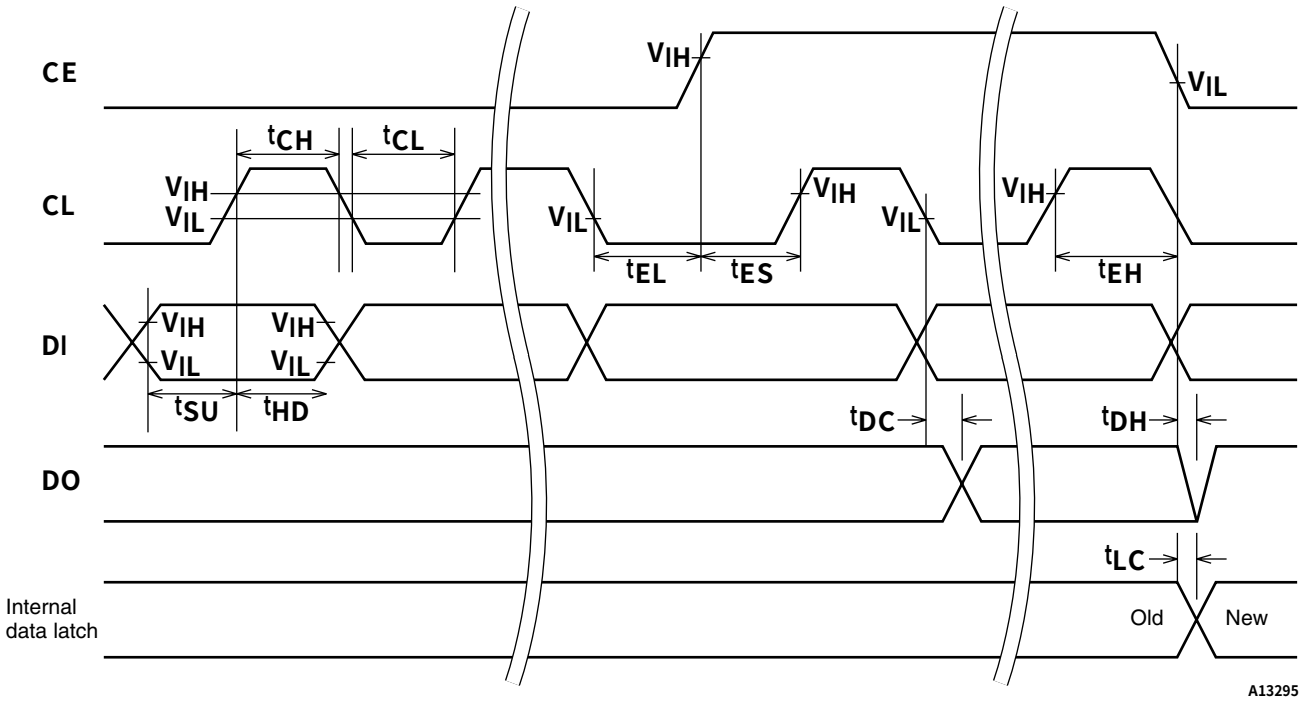
LA1781 Pin No.	Pin Function	LA17000M Pin No.	Pin Function	LC72144M Pin No.
28	SNC control input	44		
29	HCC control input	45		
30	Noise canceller IN	46		
31	AM/FM detector output	47		
32	FM S-meter output	48		
33	MUTE drive	49		
34	AFC IN	50		
35	QD OUT	51		
36	CD IN	52		
37	VREF	53		
38	FMSD	54		
39	GND Keyed AGC	55		
40	V_{CC}	56		
41	HCC capacitor	57		
42	AM L.C.	58		
43	Pilot detector	59		
44	IF AGC	60		
45	AM IFT (IF output)	61		
46	AM ANTD W-AGC IN	62		
47	FM Mute ON ADJ	63		
48	RF AGC	64		
49	AM 2nd MIX IN	65		
50	FM IF BYPASS	66		
51	FM IF IN	67		
52	AM IF IN	68		
53	1st IF amplifier output	69		
54	AM MIX OUT	70		
55	W-AGC IN AM SD ADJ	71		
56	1st IF IN	72		
57	AM RF AGC OUT	73		
58	N-AGC IN	74		
59	1st MIX OUT	75		
60	1st MIX OUT	76		
61	F.E.V_{CC}	77		
64	FM MIX IN	78	1st IF narrow IN	
62	AM MIX IN	79		
63	FM MIX IN	80		

PLL Block Functions

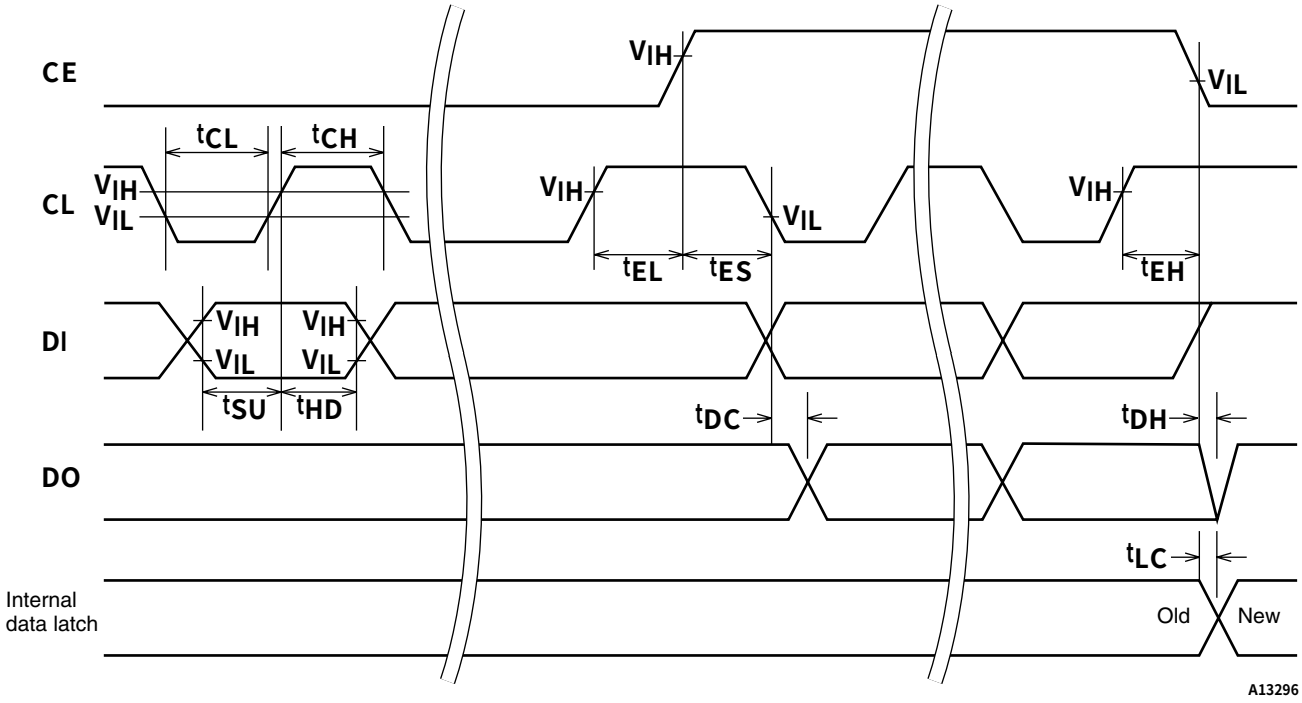
- High-speed programmable divider
  - FMIN : 10 to 160 MHz ..... Pulse swallower method
- General-purpose counter
  - HCTR : 0.4 to 25.0 MHz ..... Frequency measurement
- Crystal oscillator : Two frequencies selectable: 10.35/10.25 MHz
- Reference frequencies : 12 frequencies selectable:
  50, 30, 25, 12.5, 6.25, 3.125, 10, 9, 3, 5, and 1kHz
  *1 *1 *1
  *1: Not available when using the 10.25 MHz crystal oscillator

- Phase comparator
  - Dead zone can be controlled
  - Unlock detection circuit
  - Sub-charge pump for high-speed locking
  - Deadlock clear circuit on chip
- A/D converter ..... 6 bits: 1 input (linked directly to MRC sensor output)
- Serial data I/O
  Communications with controller possible in CCB format
- Power-on reset circuit
- On-chip crystal oscillator output buffer
- 2nd IF injection signal for AM up conversion (10.35/10.25 MHz)
- I/O port ..... General-purpose I/O: four ports

Serial Data Timing

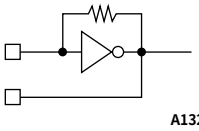
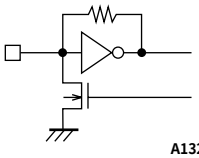
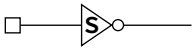
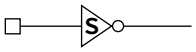
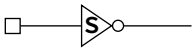
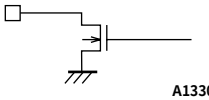
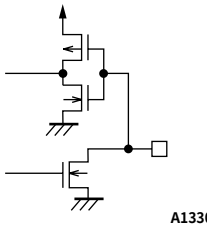
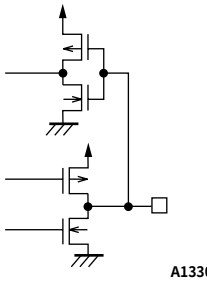
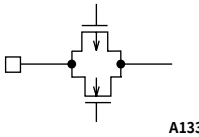


When CL is Stopped at the low level



When CL is Stopped at the high level

PLL Block Pin Description

Symbol	Pin No.	Description	Function	Pin Circuit
XIN XOUT	25 26	X'tal OSC	• For connecting the crystal oscillator. (10.35, 10.25, 7.2 or 4.5 MHz)	 A13297
PLL IN	18	Local oscillator signal input	• FMIN is selected when DVS in the serial data input is set to 1. • The input frequency range is from 10 to 160 MHz. • The signal is transmitted to the swallow counter. • The divisor can be set to a value in the range 272 to 65535.	 A13298
CE	27	Chip enable	• This pin is set high during serial data input to the PLL (DI) or during serial data output (DO).	 A13299
CL	29	Clock	• This pin is the clock for data synchronization during serial data input to the PLL (DI) or during serial data output (DO).	 A13300
DI	28	Input data	• This is the input pin for serial data that is transferred from the controller to the PLL.	 A13301
DO	30	Output data	• This is the output pin for serial data that is transferred from the controller to the PLL.	 A13302
V_{DD}	19	Power supply	• This is the PLL power supply pin. Supply 4.5 V to 5.5 V to this pin when the PLL is operating. • When power is first applied to this pin, the power-on reset circuit operates.	
V_{SS}	21	Ground	• This is the PLL ground pin.	
I/O-1 I/O-2 STSD SW	31 24 17	General-purpose I/O ports	• These are general-purpose I/O ports. • The output circuits open-drain. • During a power-on reset, I/O-1 and I/O-2 become input ports. STSD SW becomes an output port, and is fixed low. • These ports can be switched between input and output according to the serial data that is transferred from the controller (I/O-1, I/O-2, STSD SW).	 A13303
SEEK SW	33	General-purpose I/O port	• This is a general-purpose I/O port. • The output circuits are complementary circuits. • During a power-on reset, this port becomes an input port. • This port can be specified as an input or output port by the serial data that is transferred from the controller.	 A13304
ADC0	34	ADC input	• This is the A/D converter input pin. The converter is a 6-bit successive-approximation A/D converter. For details, refer to the page that describes the A/D converter configuration.	 A13305

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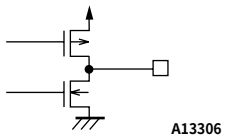
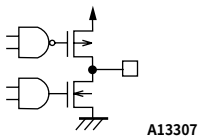
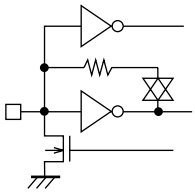
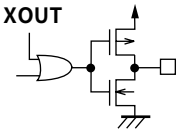
Symbol	Pin No.	Description	Function	Pin Circuit
PD1	20 0	Main charge pump output	• This is the PLL charge pump output pin. When the frequency of the local oscillation signal frequency is divided by N is higher than the reference frequency, a high level signal is output from the PD1 pin. When the frequency is lower, a low level signal is output. If the frequencies match, the pin goes to high impedance.	 A13306
PDS	22	Sub-charge pump output	• A high-speed lockup circuit can be formed by using this pin in combination with the main charge pump. • For details, refer to page that describes the charge pump configuration.	 A13307

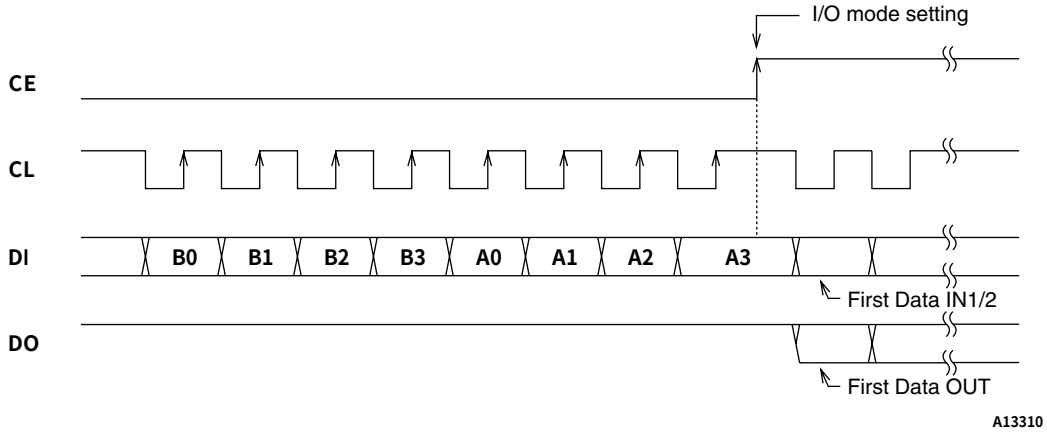
HCTR	32	General-purpose counter	• Serial data: HCTR is selected if CTS1 = 1 is set.
			  • The input frequency is 0.4 to 25 MHz.
			  • The signal is passed through to the general-purpose counter internally, via the 1/2 frequency divider. An integrating count can also be kept.
			  • The count result is output from the MSB of the general-purpose counter through the output pin DO.
			  • For details, refer to page that describes the general-purpose counter configuration.
			• Serial data: Prohibited when HCTR = 0.
				
				A13308

XBUF	23	X'tal oscillator buffer	• This is the output buffer for the crystal oscillator circuit. • Serial data: When XB = 1 is set, the output buffer operates and the crystal oscillator signal (pulse) is output. When XB = 0, this pin outputs a low level. (When a power-on reset is executed, XB = 0 and the output buffer is fixed at the low level.)	 XOUT A13309

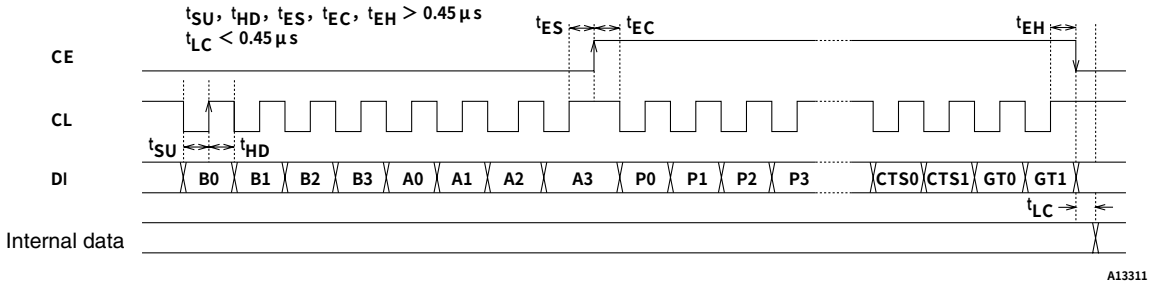
Procedures for Input and Output of Serial Data

Data I/O is handled through the Computer Control Bus (CCB), SANYO's audio IC serial bus format. This IC uses CCB with 8-bit addressing.

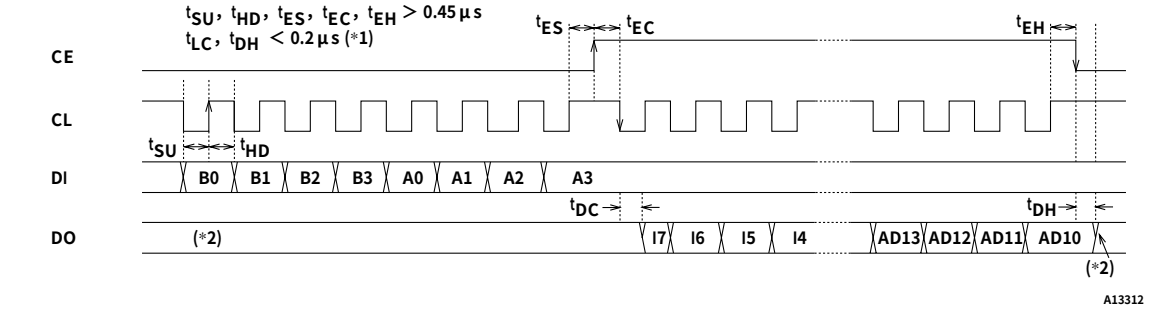
	I/O mode	Address								Description
		B0	B1	B2	B3	A0	A1	A2	A3	
[1]	IN1	0	0	0	1	0	1	0	0	• Control data input (serial data input) mode. • 32-bit data input
[2]	IN2	1	0	0	1	0	1	0	0	• Control data input (serial data input) mode. • 32-bit data input
[3]	OUT	0	1	0	1	0	1	0	0	• Data output (serial data output) mode. • The bit count output is equal to the clock cycle count.



i) Serial Data Input (IN1/IN2)



ii) Serial data output (OUT)

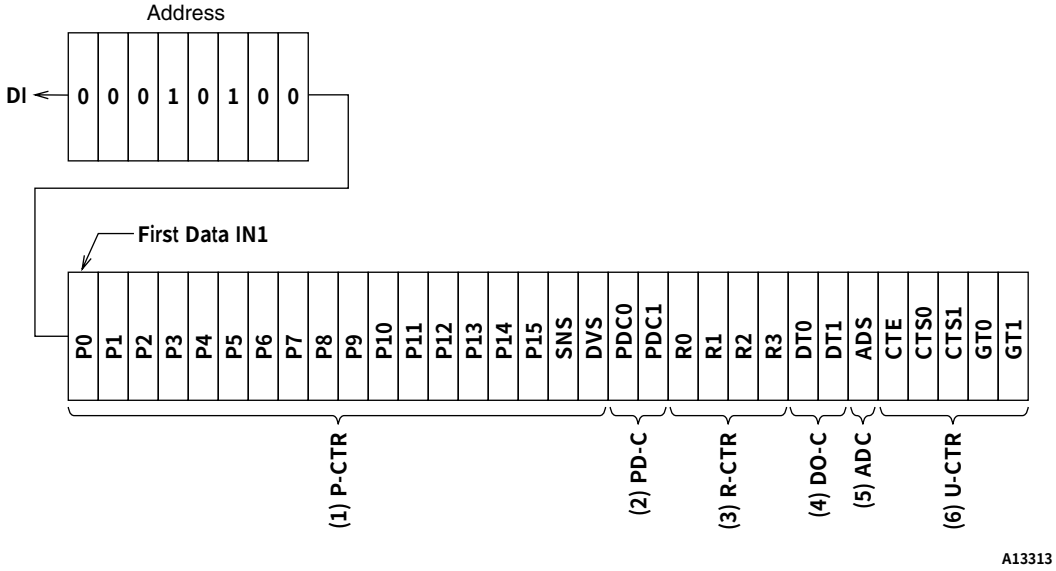


*1: Because the DO pin is an N-channel open drain pin, the data transition time varies according to the pull-up resistance and the board capacitance.

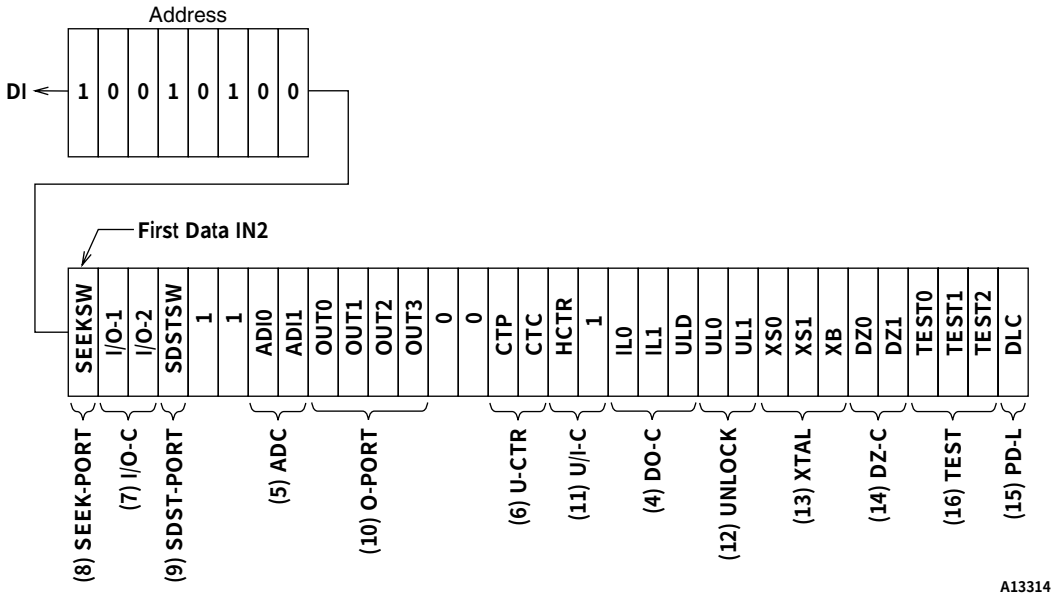
*2: The DO pin is normally open.

DI Control Data (Serial Data Input) Configuration

[1] IN1



[2] IN2 Mode



Description of DI Control Data

<table>
<tr><th>No.</th><th>Control block/Data</th><th>Description</th><th>Related data</th></tr>
<tr><td>(1)</td><td>Programmable divider data

P0 to P15

DVS, SNS</td><td>• This data sets divisor for the programmable divider. P15 is a binary value that is designated as the MSB. The LSB changes depending on DVS and SNS.
<table>
<tr><th>DVS</th><th>SNS</th><th>ISB</th><th>Divisor setting (N)</th></tr>
<tr><td>1</td><td>1</td><td>P0</td><td>272 to 65535</td></tr>
</table>
* DVS = 1 (DVS = 0: Prohibited)

• These values select the signal input pin (PLL IN) for the programmable divider, and switch the input frequency range.
<table>
<tr><th>DVS</th><th>SNS</th><th>Input pin</th><th>Input pin frequency range</th></tr>
<tr><td>1</td><td>1</td><td>PLLIN</td><td>10 to 160 MHz</td></tr>
</table>
* For details, refer to “Programmable Divider Configuration.”</td><td></td></tr>
<tr><td>(2)</td><td>Sub-charge pump control data

PDC, PDC1</td><td>• This data controls the sub-charge pump.
<table>
<tr><th>PDC1</th><th>PDC0</th><th>Subcharge pump status</th></tr>
<tr><td>0</td><td>*</td><td>High impedance</td></tr>
<tr><td>1</td><td>0</td><td>Charge pump on (when unlocked)</td></tr>
<tr><td>1</td><td>1</td><td>Charge pump on (normal operation)</td></tr>
</table>
* The sub-charge pump can be used to form a high-speed lockup circuit in combination with PD0 and PD1 (main charge pump).
• For details, refer to the page on charge pump.</td><td>UL0, UL1, DLC</td></tr>
<tr><td>(3)</td><td>Reference divider data

R0 to R3</td><td>• This is the reference frequency (fref) selection data.
<table>
<tr><th>R3</th><th>R2</th><th>R1</th><th>R0</th><th>Reference frequency</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Prohibited</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>50</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>25</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>25</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>12.5</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>6.25</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>3.125</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>3.125</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>10</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>9 *1</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>5</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>9 *1</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>30 *1</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>*2 PLL INHIBIT + X’tal OSC STOP</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>*2 PLL INHIBIT</td></tr>
</table>
*1: Prohibited when X’tal OSC = 10.25 MHz.
*2: PLL INHIBIT (backup mode)
The programmable divider block stops, the PLL IN pin is pulled down to GND, and the charge pump output goes to the floating state.</td><td></td></tr>
</table>

Continued on next page.

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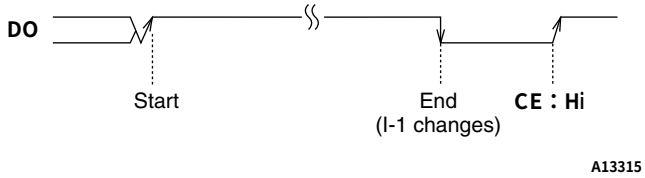
<table>
<tr><th>No.</th><th>Control block/Data</th><th>Description</th><th>Related data</th></tr>
<tr><td>(4)</td><td>DO, I/O-5 pin control data

ULD
DT0, DT1
IL0, IL1</td><td>• This data determines the output on the DO pin and the I/O-5 pin.
<table>
<tr><th>ULD</th><th>DT1</th><th>DT0</th><th>DO pin</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Low when unlocked</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>end-AD</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>end-UC</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>IN (*1)</td></tr>
</table>
end-AD: End of conversion by the A/D converter
end-UC: End of conversion by the general-purpose counter


* 1
<table>
<tr><th>IL1</th><th>IL</th><th>IN</th></tr>
<tr><td>0</td><td>0</td><td>Open</td></tr>
<tr><td>0</td><td>1</td><td>I-1 (pin status)</td></tr>
<tr><td>1</td><td>0</td><td>I-2 (pin status)</td></tr>
<tr><td>1</td><td>1</td><td>If I-1 changes, DO goes low. (Note)</td></tr>
</table>
* However, if the I/O-1 and I/O-2 pins are specified as output ports, these pins are open.
Note: Cannot be used when X'tal OSC is set to STOP. (DO does not change.)
[When the reference divider data: R3 = R2 = R1 = 1 and R0 = 0]</td><td>I/O-1
I/O-2</td></tr>
<tr><td>(5)</td><td>A/D converter control data

ADS
ADI0</td><td>• A/D converter conversion start data.
ADS = 1: A/D conversion reset and start
0: A/D conversion reset
<table>
<tr><th>ADI1</th><th>ADI0</th><th>AD input pin</th></tr>
<tr><td>1</td><td>1</td><td>Stopped</td></tr>
<tr><td>1</td><td>0</td><td>ADC0</td></tr>
<tr><td>0</td><td>1</td><td>Not usable</td></tr>
<tr><td>0</td><td>0</td><td>Not usable</td></tr>
</table></td><td></td></tr>
</table>

Continued on next page.

Continued from preceding page.

<table>
<tr><th>No.</th><th>Control block/Data</th><th>Description</th><th>Related data</th></tr>
<tr><td>(6)</td><td>General-purpose counter control data

CTS0, CTS1
CTE
GT0, GT1

CTP
CTC</td><td>• This data sets the general-purpose counter input pin (HCTR).
<table>
<tr><th>CTS1</th><th>Measurement time</th><th>Measurement mode</th></tr>
<tr><td>1
0</td><td>HCTR
—</td><td>Frequency
Not measured</td></tr>
</table>
• General-purpose counter measurement start data
CTE = 1: Count start
= 0: Count reset
• This data determines the measurement time (frequency mode) and number of periods (period mode) for the general-purpose counter.
<table>
<tr><th rowspan="2">GT1</th><th rowspan="2">GT0</th><th colspan="3">Frequency measurement mode</th><th rowspan="2">Period measurement mode</th></tr>
<tr><th>Measurement time (ms)</th><th>Wait time (ms)
CTP = 0</th><th>Wait time (ms)
CTP = 1</th></tr>
<tr><td>0</td><td>0</td><td>4</td><td>3 to 4</td><td>1 to 2</td><td>1 period</td></tr>
<tr><td>0</td><td>1</td><td>8</td><td>3 to 4</td><td>1 to 2</td><td>1 period</td></tr>
<tr><td>1</td><td>0</td><td>32</td><td>7 to 8</td><td>1 to 2</td><td>2 periods</td></tr>
<tr><td>1</td><td>1</td><td>64</td><td>7 to 8</td><td>1 to 2</td><td>2 periods</td></tr>
</table>
• CTP = 0: When a count reset is executed (CTE = 0), the general-purpose counter input is pulled down.
= 1: When a count reset is executed (CTE = 0), the general-purpose counter input is not pulled down, and the wait time is reduced. However, immediately after CTP = 1 is set, the start of the count must wait until the general purpose counter input pin is biased.
• The input sensitivity is reduced when CTC = 1. (Sensitivity: 10 to 30 mVrms)</td><td>HCTR</td></tr>
<tr><td>(7)</td><td>I/O port control data

I/O-1 to I/0-2</td><td>• This data specifies whether an I/O port is an input port or an output port.
“data”= 0: Input port
= 1: Output port

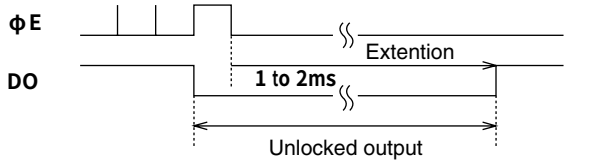
* During a power-on reset, I/O-0 and I/O-2 become input ports.
STSD SW becomes an output port.</td><td>OUT0 to OUT3
ULD</td></tr>
<tr><td>(8)</td><td>SEEK SW</td><td>• This data determines the status of the SEEK SW pin.
“data” = 0: 2.5[V] output
* This pin is open and the midpoint bias is output by an external circuit.
“data” = 1: 0[V] or 5[V] output
* Determined by the OUT0 data.</td><td>I/O-0 to I/O-3
ULD</td></tr>
<tr><td>(9)</td><td>SDST SW</td><td>• AM/FM SD, FM-ST IND output dual-purpose pin
“data” = 0: Fixed
= 1: Prohibited</td><td>I/O-0 to I/O-3
ULD</td></tr>
<tr><td>(10)</td><td>Output port data

OUT0 to OUT2</td><td>• This data determines the output on output ports O-0 through O-3.
“data” = 1: Open or Hi
= 0: Low
* Invalid if specified as an input port or unlocked output.</td><td>I/O-0 to I/O-3
ULD</td></tr>
<tr><td>(11)</td><td>General-purpose counter input control data
HCTR</td><td>• This data converts the general-purpose counter pin to an input port.
HCTR = 0: Prohibited
= 1: HCTR (general-purpose counter)</td><td>CTS1</td></tr>
</table>

Continued on next page.

Continued from preceding page.

<table>
<tr><th>No.</th><th>Control block/Data</th><th>Description</th><th>Related data</th></tr>
<tr><td>(12)</td><td>Unlock detection data

UL1, UL0</td><td>• This data selects the phase error (øE) detection width that is used for evaluating PLL lock.
If a phase error that exceeds the øE detection width in the following table is generated, the signal is deemed to be unlocked. When the signal is unlocked, the detection pin (DO or I/O-5) goes low.
<table>
<tr><th>UL1</th><th>DT0</th><th>øE detection width</th><th>Detection pin output</th></tr>
<tr><td>0</td><td>0</td><td>Stop</td><td>Open</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Direct output of øE</td></tr>
<tr><td>1</td><td>0</td><td>±0.5 µs</td><td>Extend øE by 1 to 2 ms</td></tr>
<tr><td>1</td><td>1</td><td>±1 µs</td><td>Extend øE by 1 to 2 ms</td></tr>
</table>

</td><td>ULD
DT0, DT1</td></tr>
<tr><td>(13)</td><td>Crystal oscillator circuit

XS0, XS1
XB</td><td>• This is the crystal oscillator selection data.
<table>
<tr><th>XS1</th><th>XS0</th><th>X’tal OSC</th></tr>
<tr><td>0</td><td>0</td><td>Prohibited</td></tr>
<tr><td>0</td><td>1</td><td>Prohibited</td></tr>
<tr><td>1</td><td>0</td><td>10.25 MHz</td></tr>
<tr><td>1</td><td>1</td><td>10.35 MHz</td></tr>
</table>
* When a power-on reset is executed, 10.25 MHz is selected.
• Crystal oscillator buffer (XBUF) output control data.
XB = 0: Buffer output: OFF (This mode is selected when a power-on reset is executed.)
XB = 1: Buffer output ON
* For FM reception (using the PD0 pin), XBUF output must be off.</td><td>R0 to R3</td></tr>
<tr><td>(14)</td><td>Phase comparator control data

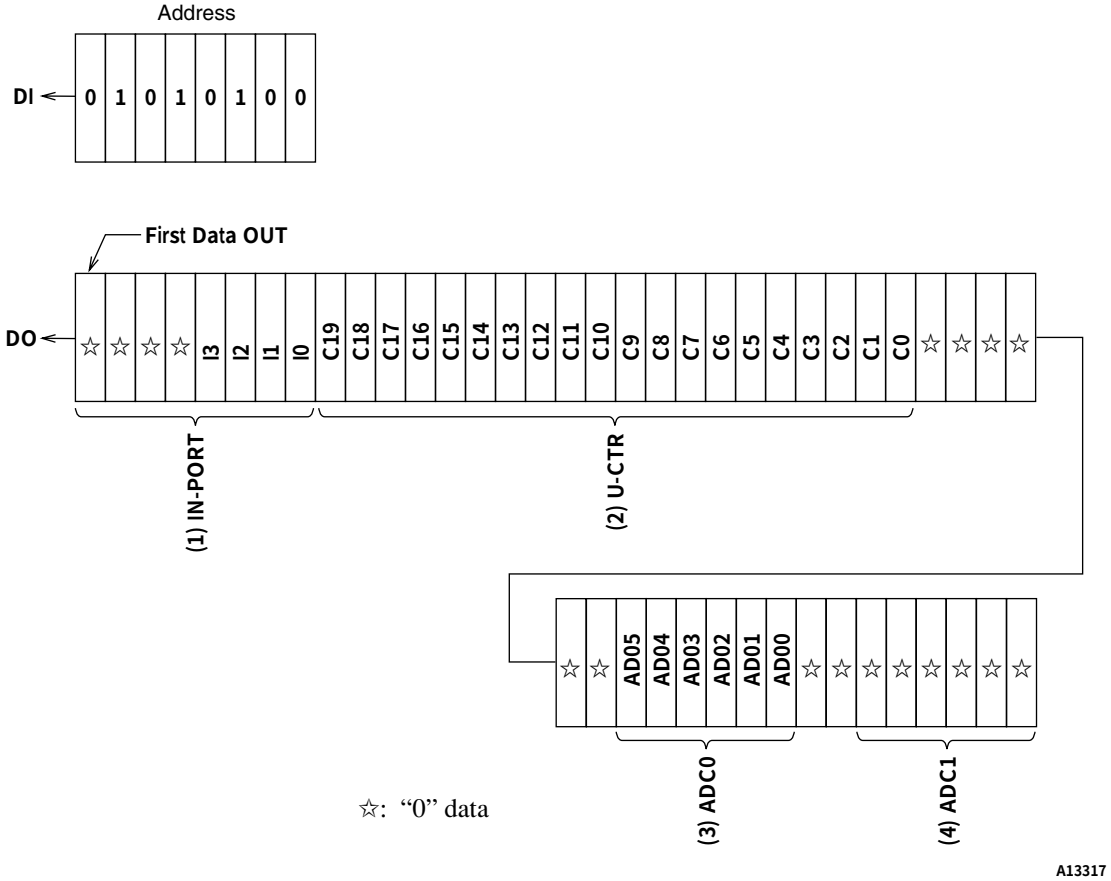
DZ0, DZ1</td><td>• This data controls the phase comparator dead zone.
<table>
<tr><th>DZ1</th><th>DZ0</th><th>Dead zone mode</th></tr>
<tr><td>0</td><td>0</td><td>DZA</td></tr>
<tr><td>0</td><td>1</td><td>DZB</td></tr>
<tr><td>1</td><td>0</td><td>DZC</td></tr>
<tr><td>1</td><td>1</td><td>DZD</td></tr>
</table>
• When a power-on reset is executed, DZA is selected.</td><td></td></tr>
<tr><td>(15)</td><td>Charge pump control data

DLC</td><td>• This data is used to force the charge pump output to the low level (V_{SS} level).
DLC = 1: Low level
= 0: Normal operation
* If a deadlock occurs because the VCO control voltage (Vtune) is 0 V and VCO oscillation is stopped, it is possible to escape the deadlock by forcing the charge pump output to low level and setting Vtune to V_{CC}.
When a power-on reset is executed, normal operation mode is selected.</td><td></td></tr>
<tr><td>(16)</td><td>IC test data

TEST0
TEST1
TEST2</td><td>• This is the IC test data.
Set TEST0 = 0.
TEST1 = 0
TEST2 = 0
* When a power-on reset is executed, all the test data is set to zero.</td><td></td></tr>
</table>

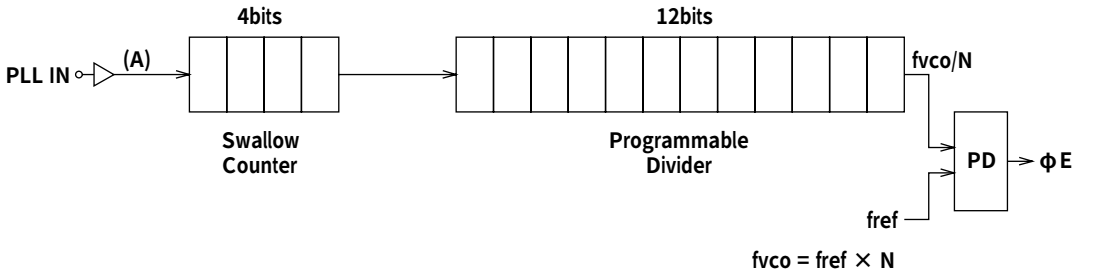
DO Output Data (Serial Data Output) Configuration

[3] OUT mode



No.	Control block/Data	Description	Related data
(1)	I/O port data I3 to I0	• I0 to I3 is the latched data reflecting the status of the input ports: I/O-0 to I/O-3. The data is latched at the point that data output mode is set. The pin status is latched regardless of the input/output specification. Pin status = Hi: 1 Low: 0	I/O-1 to I/O-2 SEEK SW HCTR
(2)	General-purpose counter binary data C19 to C0	• C19 to C0 is the latched data reflecting the contents of the general-purpose counter (a 20-bit binary counter). C19 ← MSB of binary counter C0 ← LSB of binary counter	CTS0 CTS1 CTE
(3)	A/D converter ADC0 data AD05 to AD00	• AD05 to AD00 is the latched data reflecting the results when the ADC0 pin input signal undergoes AD conversion. AD05 ← MSB AD00 ← LSB	ADI1 ADS

Programmable Divider Configuration

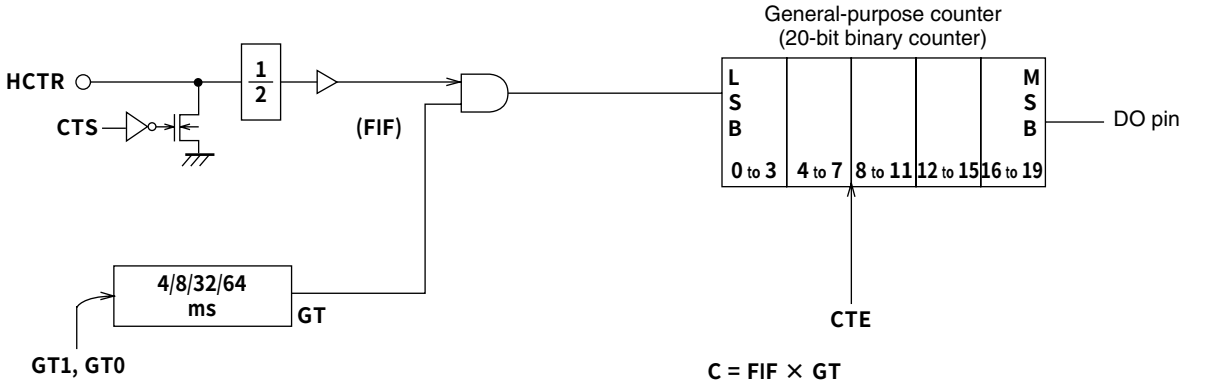


	DVS	SNS	Input pin	Divisor setting (N)	Input frequency range
(A)	1	*	PLL IN	272 to 65535	10 to 160 MHz

	Minimum input sensitivity f[MHz]	
(A) PLL IN	10 ≤ f < 130	130 ≤ f <160
	40 mVrms	70 mVrms

General-purpose Counter Configuration

In the LA17000M, the general-purpose counter consists of a 20-bit binary counter. The count results can be read through the DO pin, MSB first.



When using the general-purpose counter for cycle measurement, the measurement period can be selected from among 4, 8, 32, and 64 ms through the GT0 and GT1 data. The cycle of the signal that is input to the HCTR pin or the LCTR pin can then be measured by counting the number of pulses that are input to the general-purpose counter within this measurement period.

When using the general-purpose counter to measure a cycle, it is also possible to measure the cycle of a signal that is input to the LCTR pin according to the number of check signals (refer to the "Check Signal Frequency" table below) input to the general-purpose counter within one or two cycles of the signal that is input to the LCTR.

Check Signal Frequency

X tal OSC	10.25 MHz	10.35 MHz	
		fref = 30, 9, 3 kHz	fref other than 30, 9, 3 kHz
Check signal	10.25 kHz	1030 kHz	1150 kHz

	CTS1	Input pin	Measurement mode	Frequency range	Input sensitivity
S1	1	HCTR	Frequency	0.4 to 25.0 MHz	40 mVrms *1

*1 CTC = 0: 40 mVrms; however, when CTC = 1, the frequency range is HCTR: 8 to 12 MHz
CTC = 1: 70 mVrms

CTC data: This is the input sensitivity switch data; when CTC = 1, the input sensitivity is degraded.

	HCTR: Minimum input sensitivity standard f [MHz]		
CTC	0.4 ≤ f < 8	8 ≤ f < 12	12 ≤ f < 25
0 (Normal mode)	40 mVrms	40 mVrms (1 to 10 mVrms)	40 mVrms
1 (Degraded mode)	—	70 mVrms (30 to 40 mVrms)	—

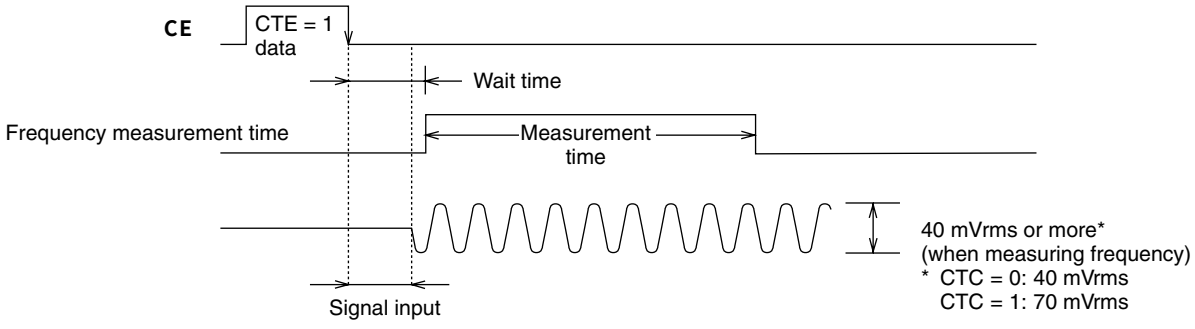
—: Not stipulated (operation not guaranteed)
( ): Actual performance estimates (reference value)

CTP data: This is data that determines the status of the general-purpose counter input pin (HCTR/LCTR) when a general-purpose counter reset (CTE = 0) is executed.
CTP = 0: Pulls down the general-purpose counter input pin.
= 1: Does not pull down the general-purpose counter input pin, reducing the wait time to 1 or 2 ms.
When setting CTP = 1, do so at least 4 ms prior to starting the count (CTE = 1). If the counter is not to be used, set CTP = 0.

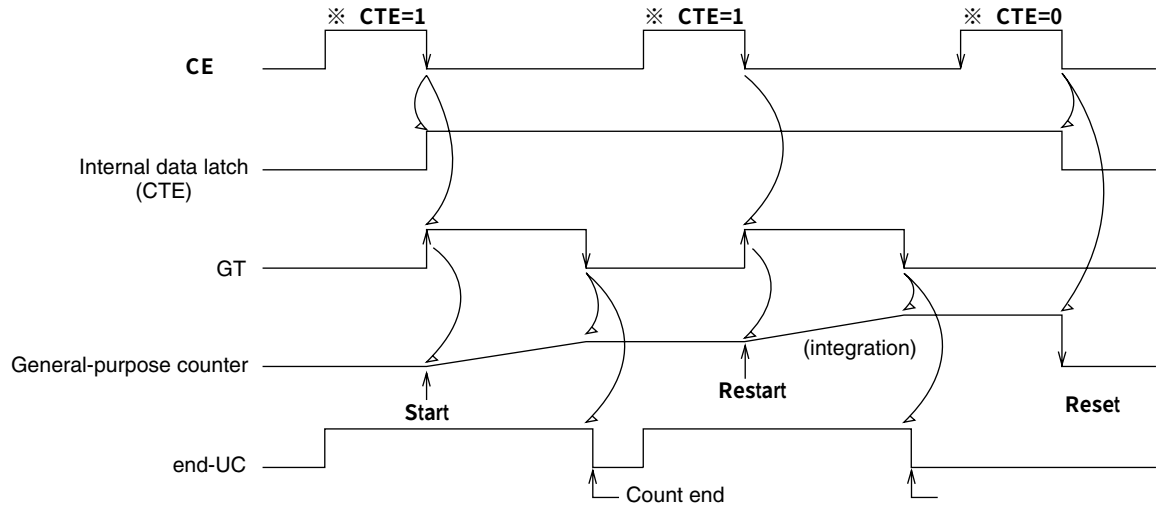
GT1	GT0	Frequency measurement mode			Cycle measurement mode
		Measurement time	Wait time		
			CTP = 0	CTP = 1	
0	0	4 ms	3 to 4 ms	1 to 2 ms	1 cycle
0	1	8			
1	0	32	7 to 8 ms		2 cycles
1	1	64			

IF Counter Operation

Before starting counting with the general-purpose counter, the general-purpose counter must first be reset by setting CTE = 0. The general-purpose counter is made to start counting by setting serial data CTE = 1. The serial data is finalized within the PLL by changing CE from high to low, but input to the HCTR pin must be started within the wait period after CE is sent low at the very latest. After measurement ends, the count results from the general-purpose counter must be read while CTE = 1. (Once CTE is set to zero, the general-purpose counter is reset.) Furthermore, the signal that was input to the HCTR pin is passed through to the general-purpose counter after having been divided by 1/2 internally. Therefore, the general-purpose count results are actually 1/2 the actual frequency of the signal that was input to the HCTR pin.



Integrated Count

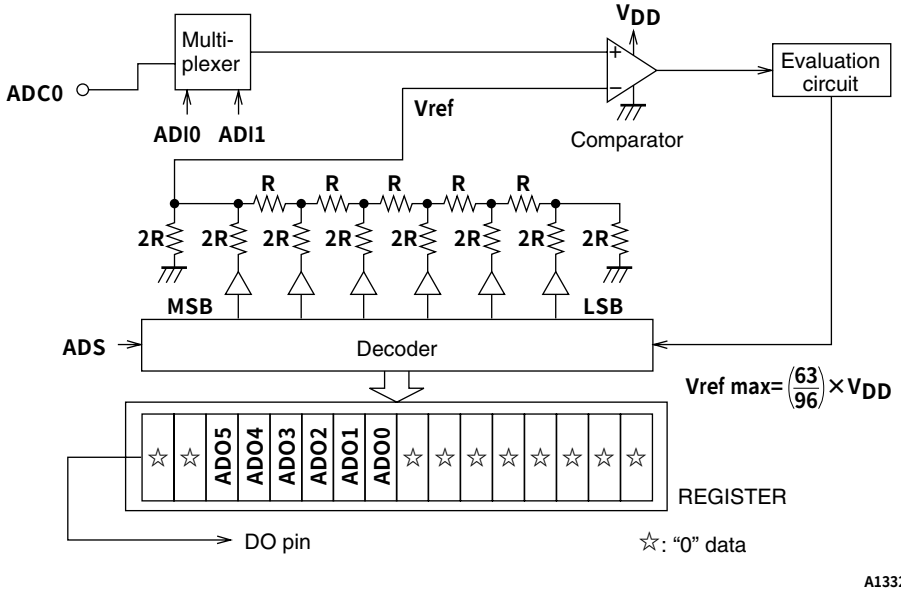


* CTE: 0 → • General-purpose counter reset
1 → • General-purpose counter start
• Setting to "1" again causes a restart.

When using integrated counting, the count value is accumulated in the general-purpose counter.
Be careful about counter overflows.
Count value: 0H to FFFFFH (1048575)
When using integrated counting, resending serial data (IN1) with CTE = 1 restarts measurement with the general-purpose counter, and the count results are added to the previous count results.

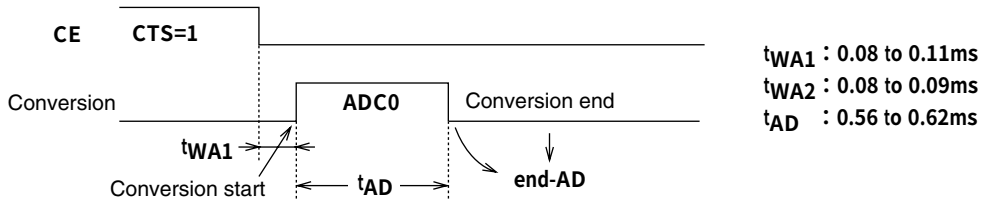
A/D Converter Configuration

This is a 6-bit successive-approximation converter with a conversion time of 0.56 ms. Full scale (when the data is 3FH) is (63/96) x VDD.

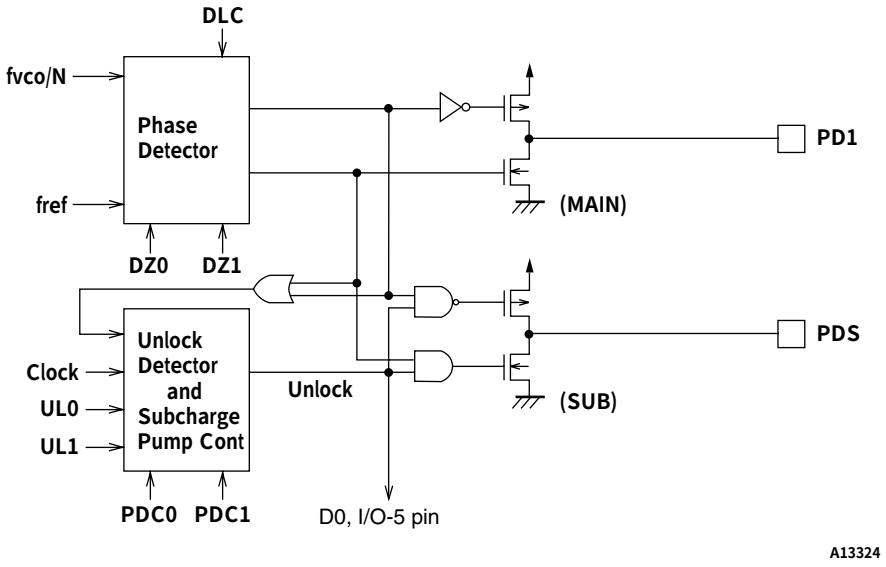


ADI1	ADI0	Input pin
1	1	Prohibited
1	0	ADC0
0	1	Prohibited
0	0	Prohibited

* Since the PLL block in the LA17000M does not provide an external pin for ADI1, the function cannot be used. ADI0 is linked directly to the pin 34 MRC sensor output, and is used exclusively for multipath signal intensity detection.



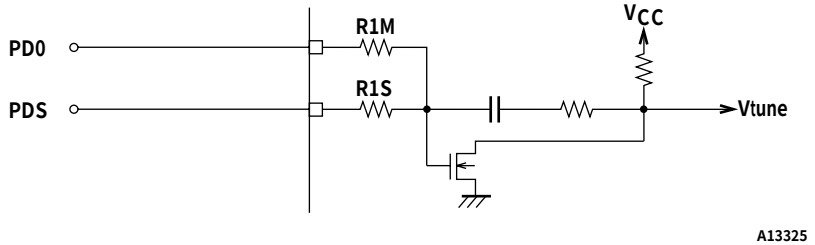
Charge Pump Configuration



PDC1	PDC0	PDS (sub-charge pump status)
0	*	High impedance
1	0	Charge pump on (when unlocked)
1	1	Charge pump on (at all times)

DLC	PD1, PDS
0	Normal operation
1	Forced low

If the unlocked state is detected during a channel change, the PDS (sub-charge pump) operates, R1 ← R1M/R1S, the low-pass filter time constant is reduced, and lockup is accelerated.



* Unlock detection data: UL1 = 1 must be set. This sets the unlock detection width to "±0.5 μs" or "±1 μs" mode; if a phase difference that is greater than the value in question is detected, the signal is unlocked and the sub-charge pump operates. As the locked condition is approached and the phase difference falls to less than the unlocked detection width, the sub-charge pump stops operating (goes to high impedance).

Other Items

[1] Notes on the Phase Comparator Dead Zone

DZ1	DZ0	Dead zone mode	Charge pump	Dead zone
0	0	DZA	ON/OFF	– –0 s
0	1	DZB	ON/ON	–0 s
1	0	DZC	OFF/OFF	+0 s
1	1	DZD	OFF/OFF	++0 s

Since correction pulses are output from the charge pump even if the PLL is locked when the charge pump is in the ON/ON state, the loop can easily become unstable. This point requires special care when designing application circuits.

The following problems may occur in the ON/ON state.
- Side band generation due to reference frequency leakage
- Side band generation due to both the correction pulse envelope and low frequency leakage

Schemes in which a dead zone is present (OFF/ON) have good loop stability, but have the problem that acquiring a high C/N ratio can be difficult. On the other hand, although it is easy to acquire a high C/N ratio with schemes in which there is no dead zone, it is difficult to achieve high loop stability. Therefore, it can be effective to select DZA or DZB, which have no dead zone, in applications which require an FM S/N ratio in excess of 90 to 100 dB, or in which an increased AM stereo pilot margin is desired. On the other hand, we recommend selecting DZC or DZD, which provide a dead zone, for applications which do not require such a high FM signal-to-noise ratio and in which either AM stereo is not used or an adequate AM stereo pilot margin can be achieved.

Dead Zone

The phase comparator compares fp to a reference frequency (fr) as shown in Fig. 1. Although the characteristics of this circuit (see Fig. 2) are such that the output voltage is proportional to the phase difference ø (line A), a region (the dead zone) in which it is not possible to compare small phase differences occurs in actual ICs due to internal circuit delays and other factors (line B). A dead zone as small as possible is desirable for products that must provide a high S/N ratio.

However, since a larger dead zone makes this circuit easier to use, a larger dead zone is appropriate for popularly-priced products. This is because it is possible for RF signals to leak from the mixer to the VCO and modulate the VCO in popularly-priced products in the presence of strong RF inputs. When the dead zone is narrow, the circuit outputs correction pulses and this output can further modulate the VCO and generate beat frequencies with the RF signal.

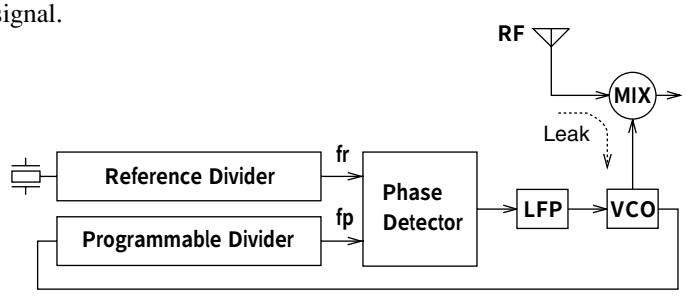


Fig. 1 A13326

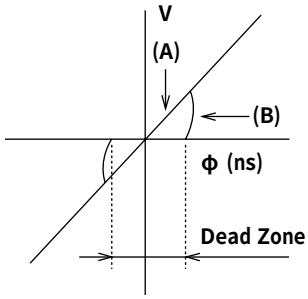


Fig. 2 A13327

[2] Notes on the PLL IN and HCTR pins

Coupling capacitors must be placed extremely close to these pins. The capacitance should be about 100 pF. If a capacitor with a capacitance of 100 pF or less is not used with HCTR in particular, there will be a long wait until the bias level is reached, which may sometimes cause miscounting.

[3] Notes on IF counting

When using the general-purpose counter for IF counting, be certain to have the microcontroller determine whether the IF-IC SD (Station Detector) signal is present or not, and to turn on the IF count buffer output and conduct the count, but only if the SD signal is present. Conducting an auto search using only the IF count is not reliable, since there is a possibility of stopping even where there is no station due to leaked output from the IF count buffer.

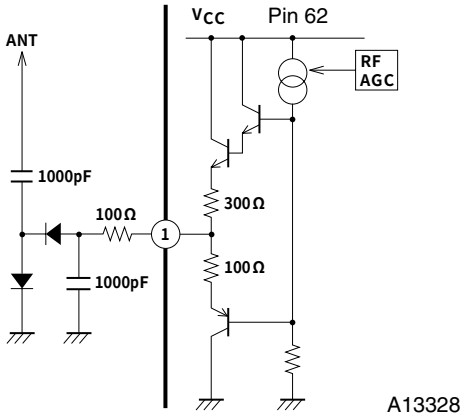
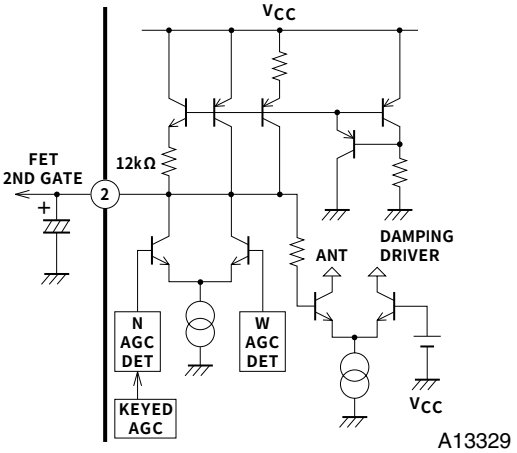
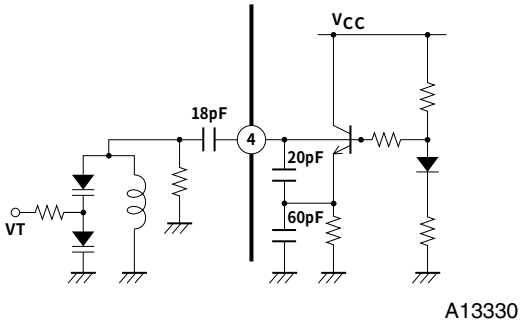
[4] Using the DO pin

Aside from data output mode, the DO pin can also be used to check for the completion of counting by the general-purpose counter, unlock detection output, and to check for changes in the input pins. It is also possible to input the status of the input pins (I/O-1, I/O-2) to the controller, unchanged, via the DO pin.

[5] Cautions concerning the use of XBUF
When the XBUF output is on (AM up conversion is being used), the XBUF signal may leak to the adjacent pins (PD0, I/O-3), so do not use PD0 and I/O-3 for AM reception control. (Use the PD1 pin for the AM reception charge pump.) When using PD0 and I/O-3 for FM reception control, the XBUF output must be turned off (XB data = 0).

[6] Power supply pins
To filter out noise, insert a capacitor of at least 2000 pF between the power supply pins V_{DD} and V_{SS}. The capacitor must be located as close to the pins as possible.

Tuner Block Pin Description

Pin No.	Function	Equivalent circuit	Description
1	Antenna damping drive pin.		The antenna damping current flows to this pin when the pin 2: RF AGC voltage is V_{CC}-V_D.
2	RF AGC		FET 2nd gate voltage control pin.
3	F.E.GND		
4	OSC		OSC pin with built-in Tr. capacitor for oscillator circuit.

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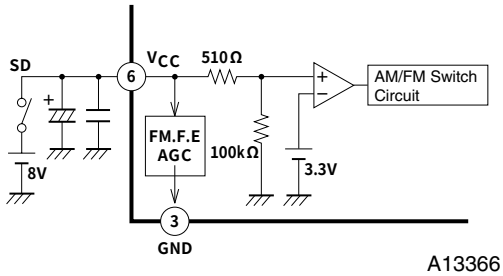
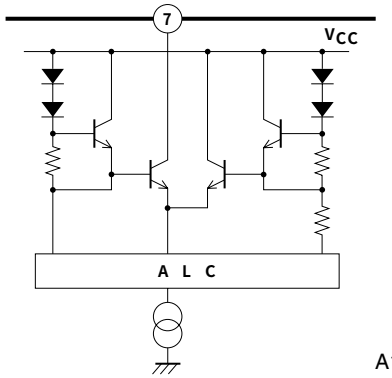
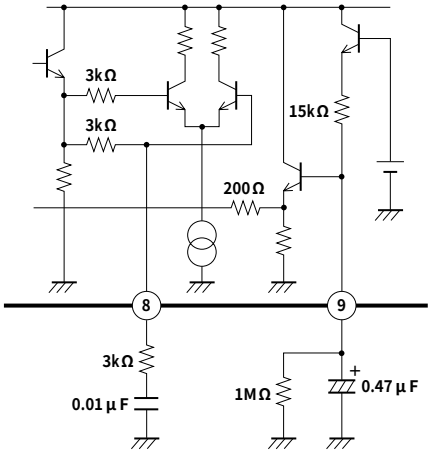
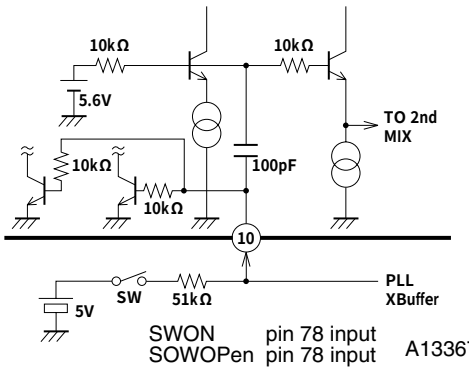
Pin No.	Function	Equivalent circuit	Description
6	F.E.V_{CC}, AM/FM switch pin	 A13366	Pin 6 is shared for FM F.E.V_{CC} and the AM/FM SW circuit. V6 voltage → Mode 8V → FM OPEN → AM
7	AM OSC	 A13331	First OSC for AM. Permits oscillation up to the SW band. ALC circuit connected.
8 9	Noise AGC sensitivity AGC adjusting pin	 A13332	Pin 8 is the noise sensitivity setting pin. After setting a moderate field (approximately 50 dBμ), use the pin 9 AGC adjusting pin to make the setting for weak fields (approximately 20 to 30 dBμ).
10	AM 2nd OSC	 SWON pin 78 input SOWOPen pin 78 input A13367	Shared pin. CF selectivity switch. Select either 10.7 MHz 1st IF input pin 72 or pin 78. • A second local oscillation signal is injected by the PLL XBuffer. * The PLL X'tal is as follows: AM 9 kHz step 10.35 MHz AM 10 kHz step 10.25 MHz (NDK AT-51 type: XTAL oscillator)

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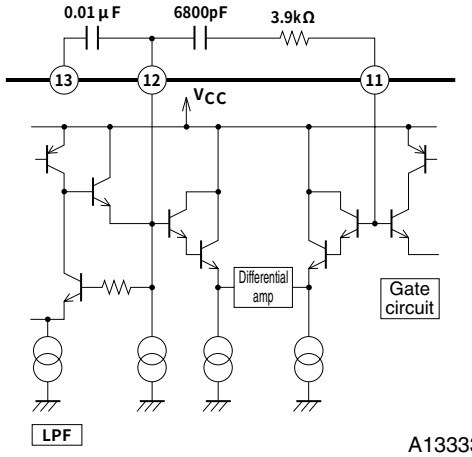
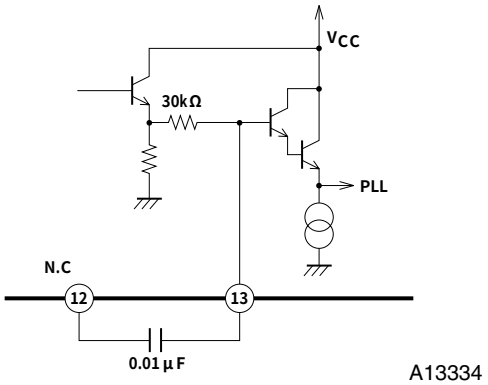
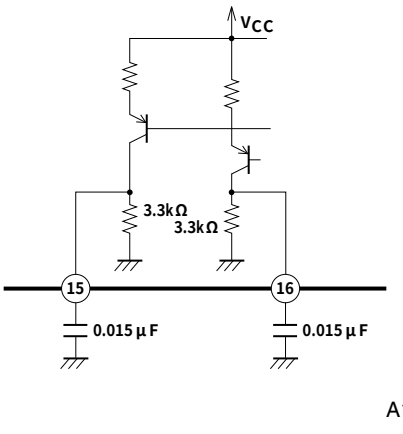
Pin No.	Function	Equivalent circuit	Description
11 12	Memory circuit pin Memory circuit pin		Memory circuit used when the noise canceller is in operation.
13	Pilot input		Pin 13 - PLL circuit signal input pin.
14	N.C, MPX, MRC, GND		GND for N.C/MPX/MRC circuit.
15 16	MPX output (LEFT) MPX output (RIGHT)		De-emphasis 50 µs; 0.015 µF 75 µs; 0.022 µF

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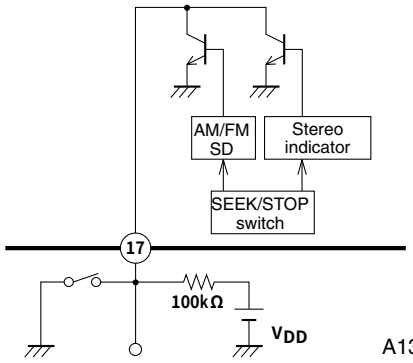
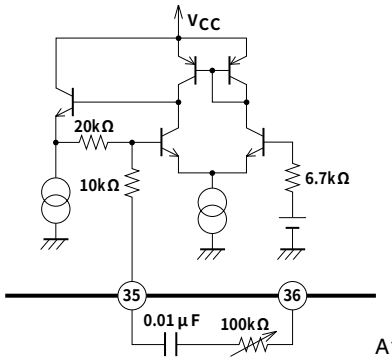
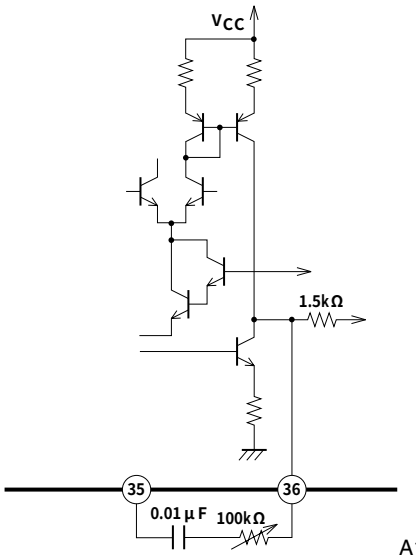
Pin No.	Function	Equivalent circuit	Description
17	SD pin Stereo indicator	 A13342	For FM: V17 switches among three modes according to the following voltages. 5 V: Operates in conjunction with the SD pin and the IF count buffer. 2.5 V: Operates as SD pin in forced SD mode. RDS AF9AR. 0 V: Reception mode stereo indicator For AM: (two modes: 0 and 5 V) 5 V: Operates as SEEK SD pin. 0 V: Reception mode, not used
35	Pilot canceller signal input	 A13336	The pilot signal level requires adjustment since it changes according to variations in the IF output level, etc.
36	Pilot canceller signal output	 A13337	Pin 36 pilot canceller signal output pin.

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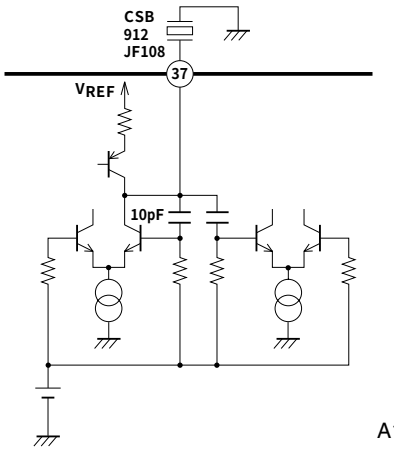
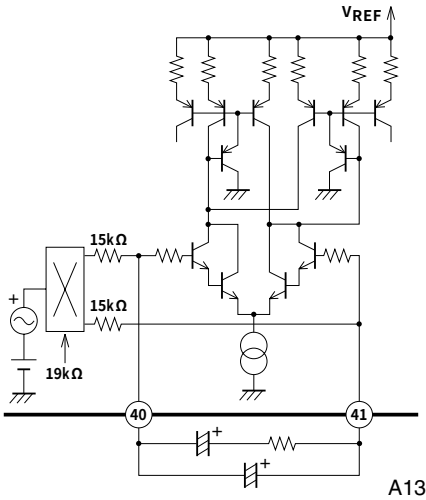
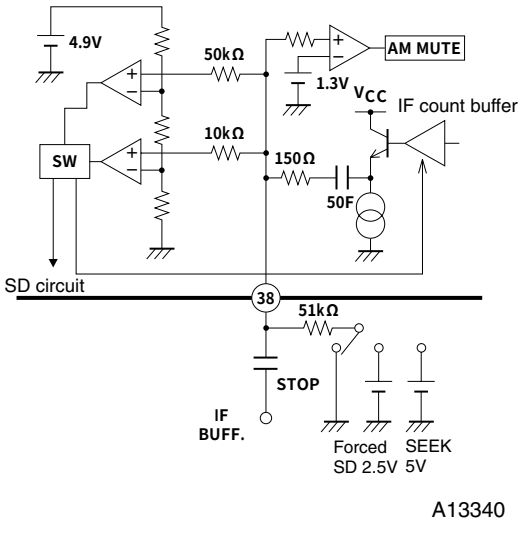
Pin No.	Function	Equivalent circuit	Description
37	VCO		Oscillation frequency: 912 kHz. Murata CSB912JF108
40 41	PHASE COMP. PHASE COMP.		
38	IF count buffer SEEK/STOP switch		Shared pin for the IF count buffer (AC output) and SEEK/STOP switch (DC input). V38 switches among three modes according to the following voltages. For FM: 5 V: SEEK mode 2.5 V: Forced SD mode, RDS mode 0 V: Reception mode For AM (two modes: 0 and 5V) 5 V: SEEK mode 0 V: Reception mode *When interference from an adjacent FM frequency is detected: 2.5 V: Use RDS mode.

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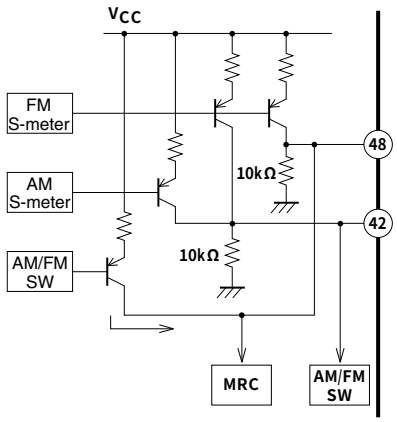
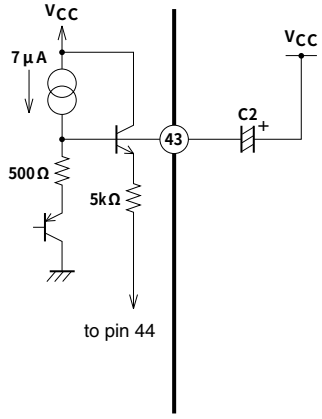
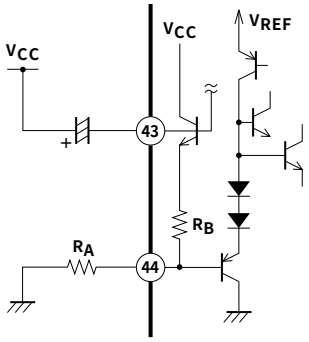
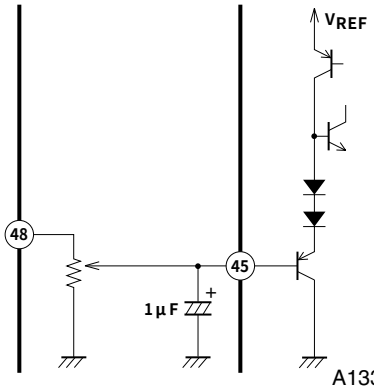
Pin No.	Function	Equivalent circuit	Description
42 48	AM/FM S-meter Dedicated FM S-meter	 A13341	Constant current drive-type S-meter output. When AM is set, pin 48 outputs a 1 mA current, which turns HCC OFF.
43	MRC control voltage time constant	 A13343	The MRC detection time constant is determined 1 kΩ and C2 when discharging and by a constant current of 7 μA and C2 when charging.
44	SNC control input pin	 A13344	Controls sub-output with an input of 0 to 1 V. SNC voltage is determined by the RA and RB component voltage. This sets the separation blend curve. RB = 5 kΩ on chip RA is external
45	HCC control input pin	 A13345	Controls high frequency output with an input of 0 to 1 V. Control through the MRC output is also possible. Use at least a 100 kΩ resistor when using pin 48 FM S-meter for control.

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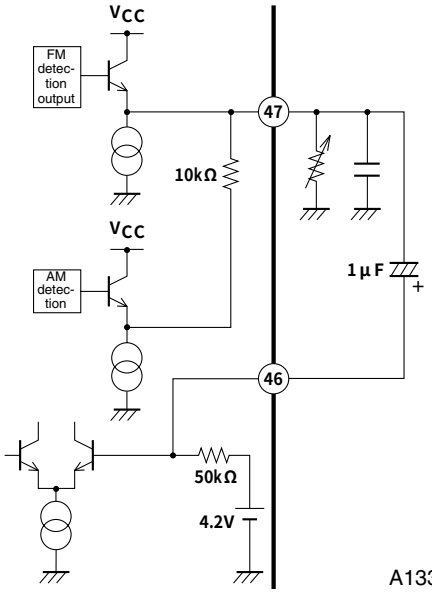
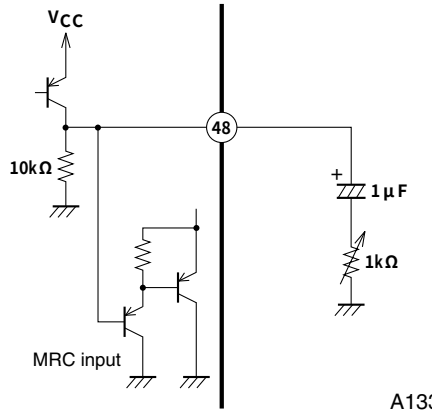
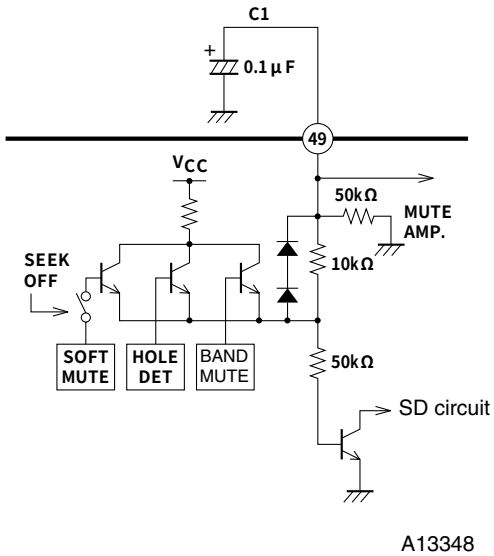
Pin No.	Function	Equivalent circuit	Description
46 47	Noise canceller input AM/FM detection output		Pin 46: N.C. input Input impedance 50 kΩ Pin 47: AM.FM detection output For FM: Low impedance For AM: 10 kΩ output To improve low-band separation, use a coupling capacitor of at least 10 μ.
48	IF S-meter output and MRC DC input pin		FM S-meter output block MRC AC input block Adjust an external 1-kΩ resistor to attenuate and control the MRC AC input.
49	Mute driver output		1) The mute time constant is determined by an external CR as follows: Attack time $T_A = 10\ k\Omega \times C1$ Release time $T_R = 50\ k\Omega \times C1$ 2) Noise convergence adjustment Fine adjustments can be made when there is no input to the ANT input by inserting a resistor between pin 49 and GND. 3) Mute off function Short pin 49 with GND using a 4-kΩ resistor.

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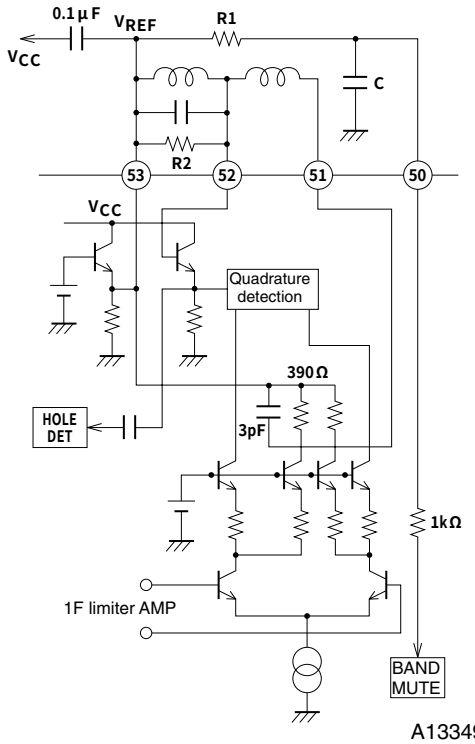
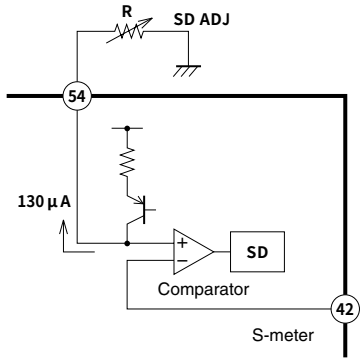
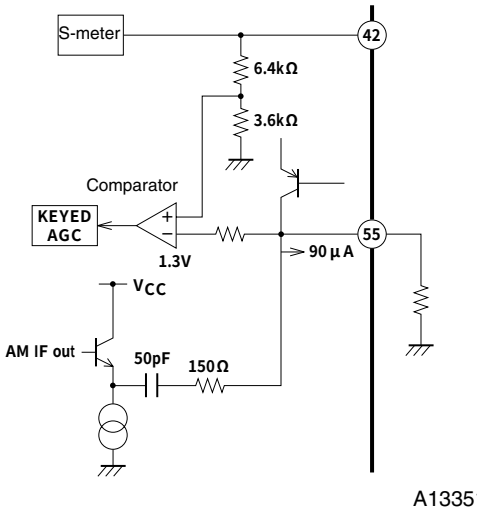
Pin No.	Function	Equivalent circuit	Description
50 51 52 53	AFC QD output QD input V_{REF}		• R1: Resistor that determines the band muting function. Increasing the value of R1 narrows the band Reducing the value of R1 widens the band. • Null voltage Voltage between pins 50 and 53 during tuning: V_{50-53} = 0 V Band muting turns on when $\|V_{50-53}\| \geq 0.7$ V. V_{53} = 4.9V
54	FM SD Adi		Current of 130 µA flows from pin 54 and comparison voltage is determined by external resistance.
55	Keyed AGC AM stereo buffer		The keyed AGC operates when the voltage divided by the 6.4-kΩ and 3.6-kΩ resistors on S-meter output pin 42 falls below the voltage determined by the resistor between pin 55 and GND. Shared pin for the AM stereo decoder IF buffer.

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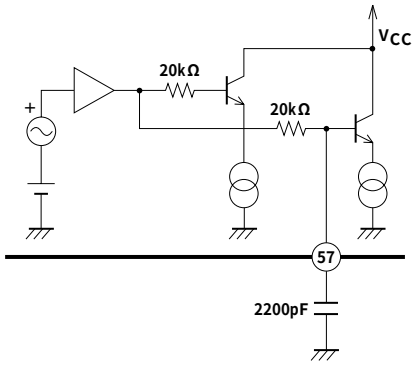
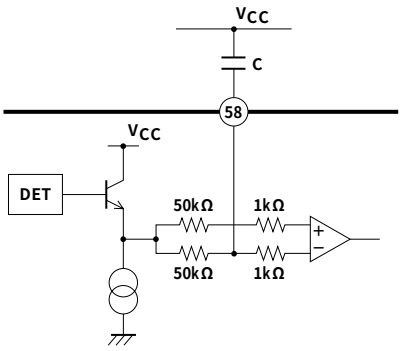
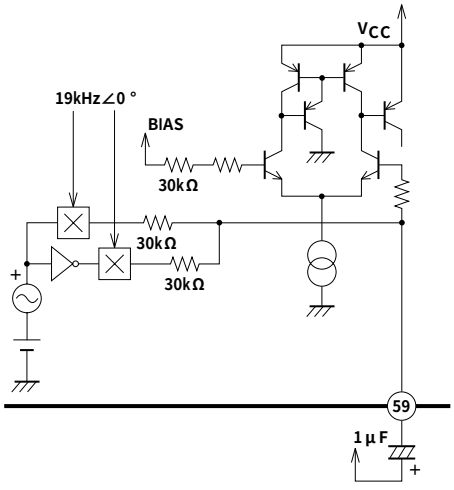
Pin No.	Function	Equivalent circuit	Description
57	HCC capacitor	 A13352	HCC frequency characteristics are determined by the capacitance of the external capacitor.
58	AM L.C. pin	 A13353	In AM mode, this changes the frequency characteristics of the unneeded audio band below 100 Hz in order to produce clear audio. Note: The capacitor for the LC must be connected to V_{CC} (pin 56) (because the detection circuit operates with V_{CC} as a reference). The cutoff frequency f_C is determined by the following formula: $f_C = 1/2\ \pi \times 50\ k\Omega \times C$
59	Pilot detector	 A13354	Inserting a 1-MΩ resistor between pin 59 and V_{CC} forces MONO.

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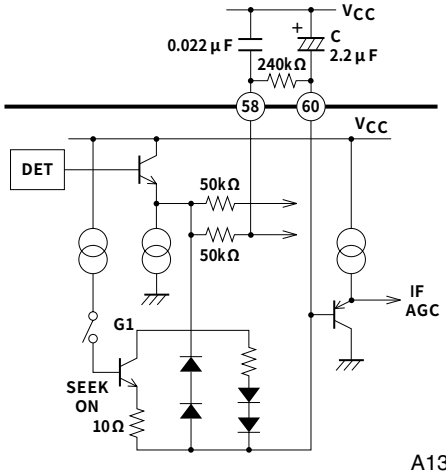
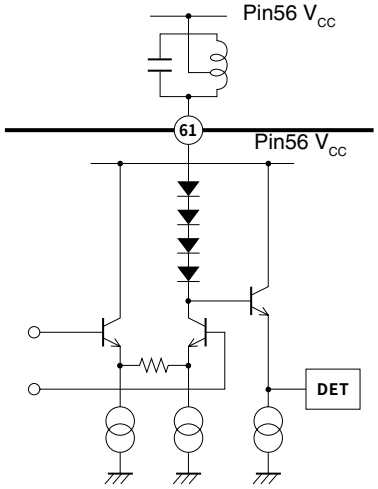
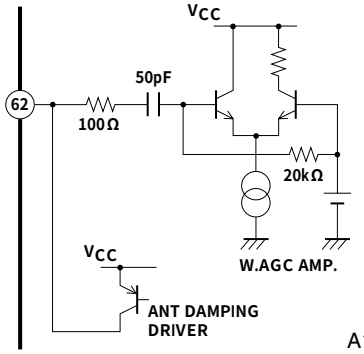
Pin No.	Function	Equivalent circuit	Description
60	IF AGC		Q1: Seek time constant switch $\tau = 2.2\ \mu F \times 300\ k$ ② SEEK $\tau = 2.2\ \mu F \times 10$ Connect external C to V_{CC} (because the IF amplifier operates with V_{CC} as a reference).
61	IF output		IF amplifier load
62	AM ANT damping drive output Wideband AGC input		I62 = 6 mA max ANT damping current

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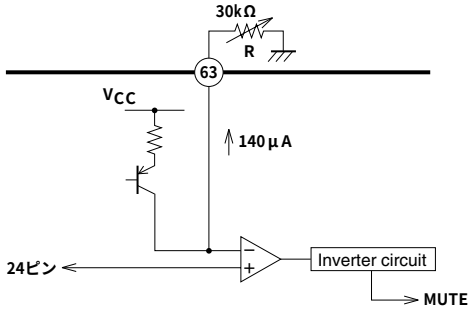
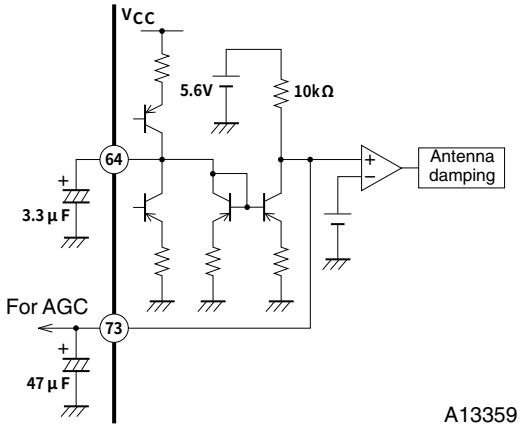
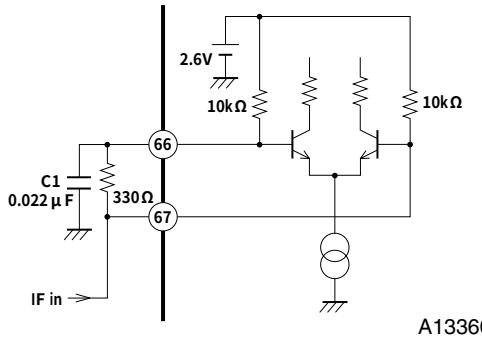
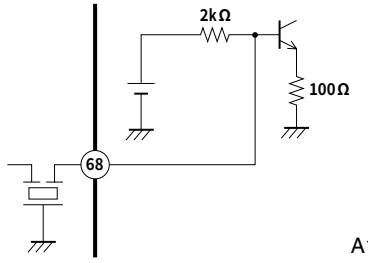
Pin No.	Function	Equivalent circuit	Description
63	FM mute on Adjust	 A13358	Vary the external resistor to adjust the mute on level.
64 73	RF AGC bypass RF AGC	 A13359	RF AGC rectification capacitor The distortion in low-frequency modulation is determined as follows. C64, C73 → Increase Distortion → Good Response → Slow C64, C73 → Decrease Distortion → Worsens Response → Fast
66 67	IF bypass FM IF input	 A13360	Be careful in regards to the GND point for the limiter amplifier input C. Ground C1 at a point that does not increase AMR.
68	IF input	 A13361	Input impedance 2 kΩ

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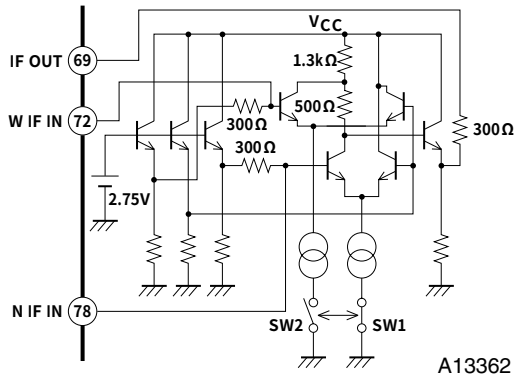
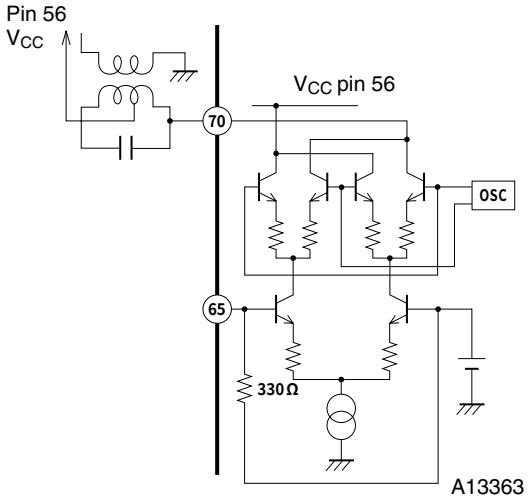
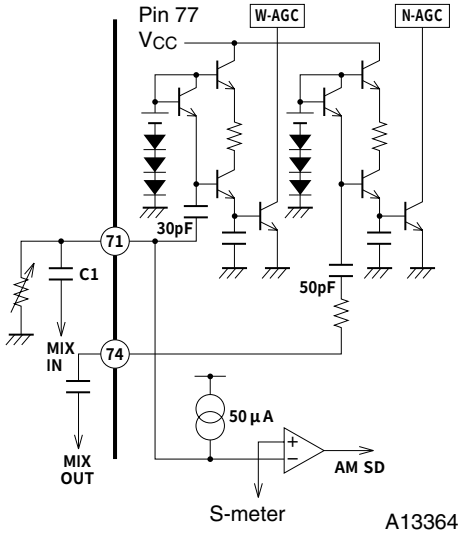
Pin No.	Function	Equivalent circuit	Description
69 72 78	IF amplifier output IF amplifier input wide input IF amplifier input narrow input		• 1ST.IF amplifier I/O pin • Inversion amplifier V78 = 2 V Narrow 1st IF input V72 = 2 V Wide 1st IF input Input impedance R_{IN} = 330 Ω V59 = 5.3 V Output impedance R_{OUT} = 330 Ω When SW1 open, SW2 short When SW1 short, SW2 open Switched by the CF band, switched by voltage on pin 10.
70 65	MIX output 130 μA MIX input		Wire the MIX coil that is connected to the pin 70 MIX output to pin 56 (V_{CC}). Pin 65 MIX input. Input impedance 330 Ω
71 74	W-AGC IN AM SD Adjust N-AGC IN mute attenuation adjusting pin		Pin 71, 74 DC cut capacitors are on chip. The AGC on level is determined by the capacitance of C1 and C2. Pin 71 is the SD sensitivity adjusting pin for AM. Output current I71 = 50 μA, and V71 varies according to the external resistance. SD is put into operation by comparing V71 with the S-meter voltage.

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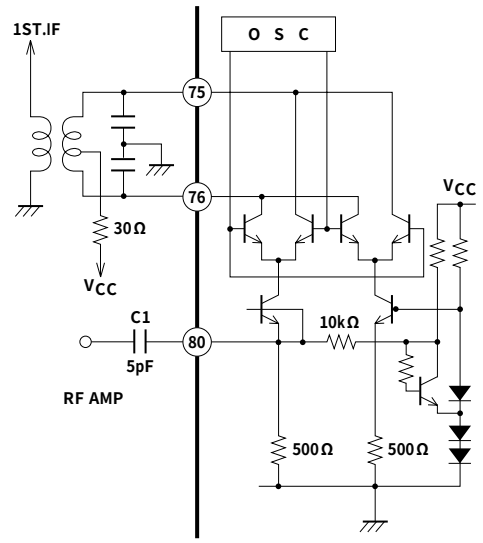
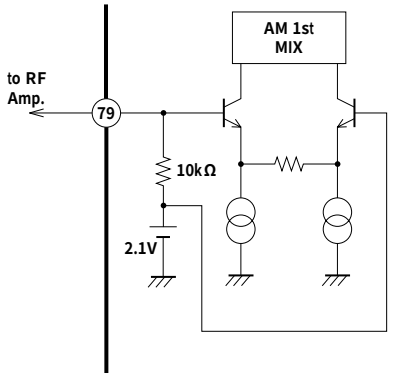
Pin No.	Function	Equivalent circuit	Description
75 76 80	MIX ouput MIX input	 A13365	Double-balance type mixer Pins 75 and 76, MIX output, 10.7 MHz output Pin 80, MIX input Emitter injection method and injection amount are determined by the values of C1 and C2. Note: The line for pin 80 must not approach pins 75 and 76.
79	1st MIX INPUT	 A13368	1st MIX input Input impedance: approximately 10 kΩ

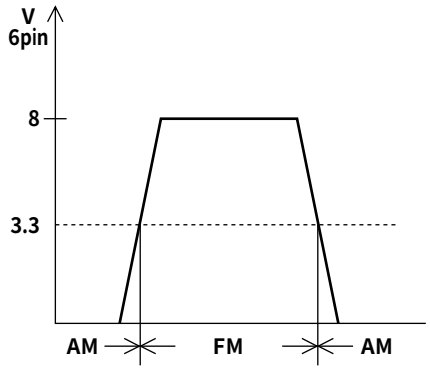
Methods for Using the LA17000M

(1) About V_{CC} and GND

Pin 56	V_{CC} for FM IF, AM, NC, MPX, and MRC
Pin 39	GND for FM IF and AM
Pin 14	GND for NC, MPX and MRC
Pin 77	V_{CC} for FM FE, AM 1st MIX, and 1st OSC
*Pin 6	V_{CC} for FM FE and AGC, and AM/FM switch
Pin 3	GND for FM FE, AM 1st MIX, and 1st OSC

(2) Notes on AM coil connection
V_{CC} for the 1st OSC coil that is connected to pin 7 should have the same electric potential as pin 77.
Connect pin 61 IFT to pin 70 MIX coil. V_{CC} should have the same electric potential as pin 56.

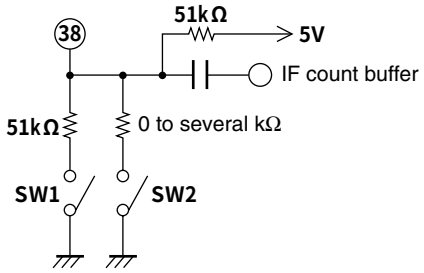
(3) AM/FM switch
Pin 6 serves as FM, FE, and RFAGC V_{CC}.



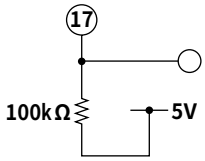
A13369

Pin 6 voltage	Mode
8	FM
OPEN	AM

(4) Relationship between pin 38 and pin 17
4-1. For FM
Pin 17 STEREO indicator and SD dual-purpose pin
Pin 38 ┌ DC input SEEK, STOP pin (control pin)
└ AC output IF count buffer pin



A13370

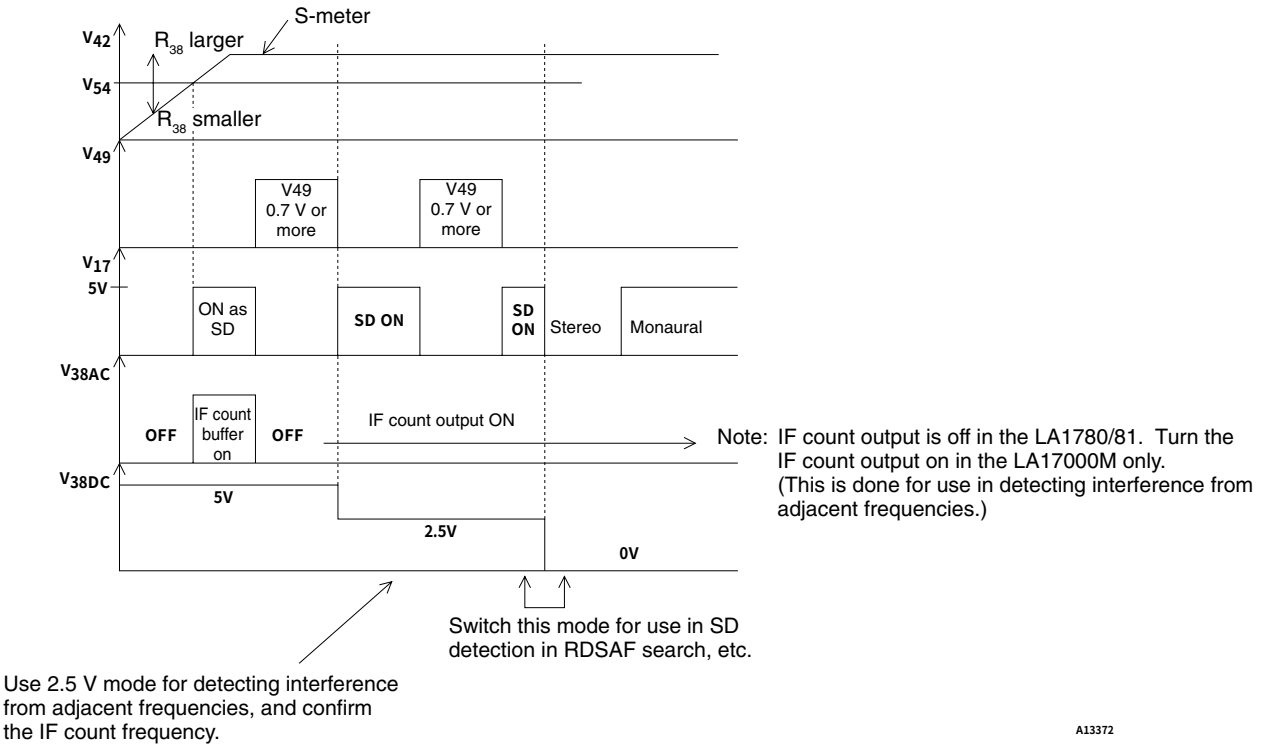


A13371

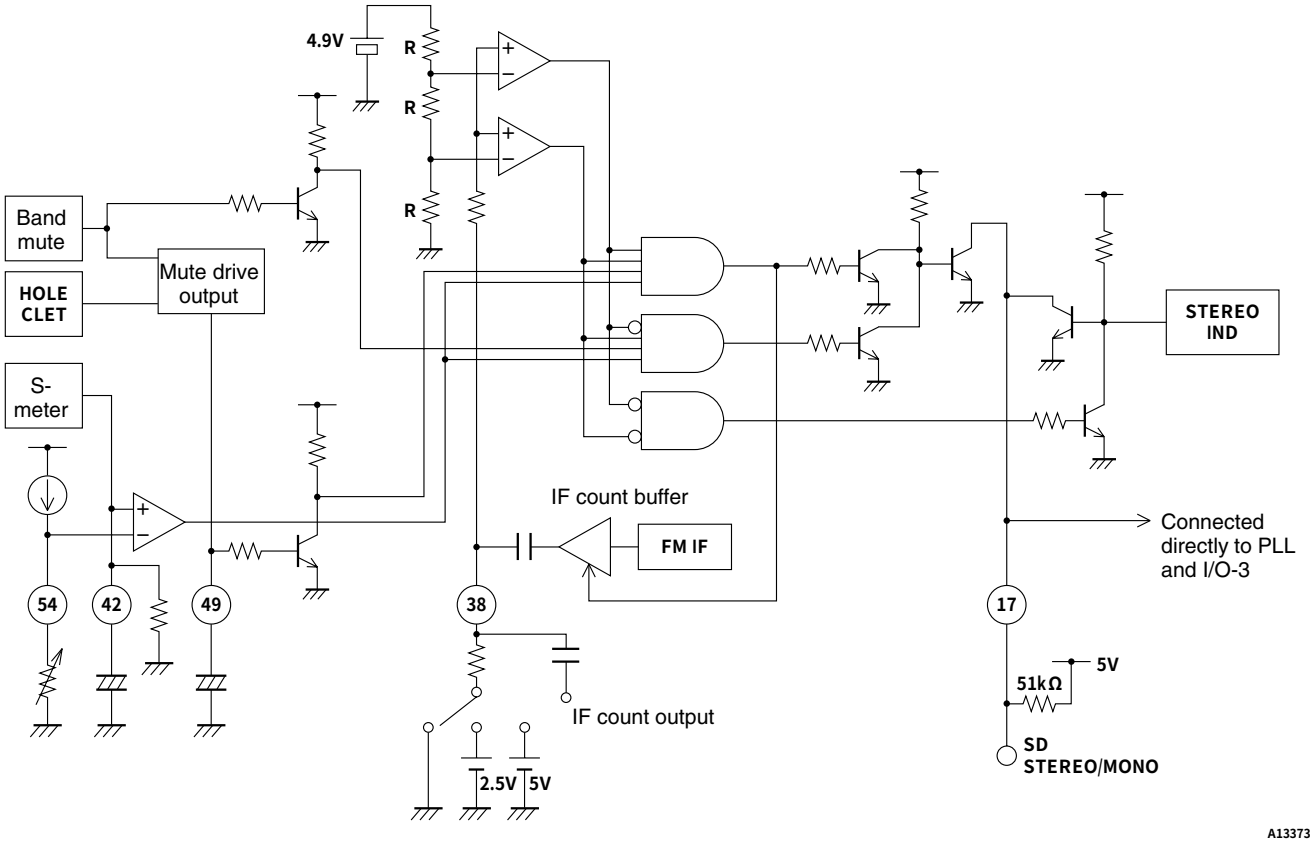
SW1	SW2	Pin 38 voltage	Pin 17	Pin 17
OPEN	OPEN	5 V	IF count buffer on	SD
ON	OPEN	2.5 V	IF count buffer on	High-speed SD
—	ON	0.7 V or less	OFF	Stereo indicator

Relationship Between Pin 38 Control Method and Output from Pins 38 and 17

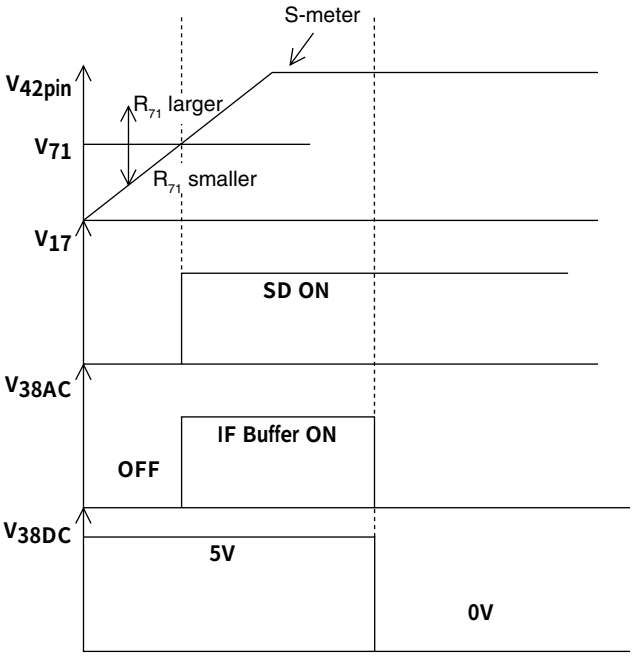
Relationship between FMSD, IF count buffer output, S-meter, and mute drive output



About FM SD

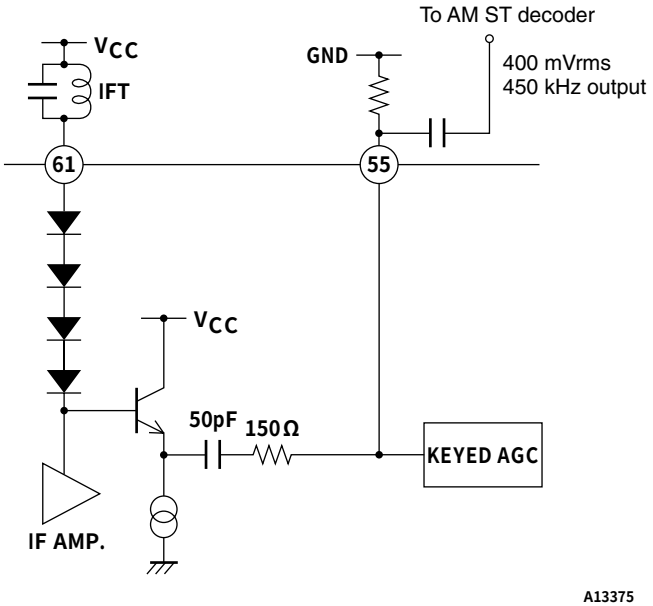


4-2. For AM



Pin 71 AM, SD, Adj Pin

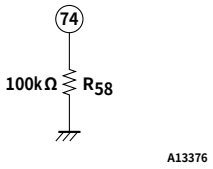
(5) AM STEREO support pin



- To attenuate the pin 55 AC level, add capacitance between GND and pin 55. For example, if pin 67 is added between GND and pin 55, the AM IF output decreases by about 6 dB.

(6) About MUTE ATT

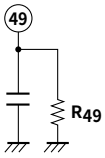
It is possible to switch to one of three levels (–20 dB, –30 dB, or –40 dB) by means of the resistor between pin 74 and GND. (This also has an effect on the total gain of the tuner.)



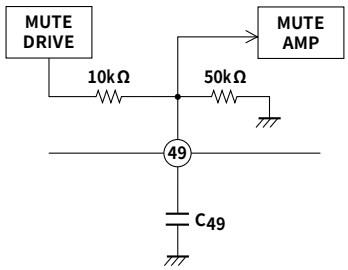
A13376

R	Mute ATT
OPEN	–20 dB
200 kΩ	–30 dB
30 kΩ	–40 dB

The attenuation can be reduced as shown in the table above by reducing R49.



A13377

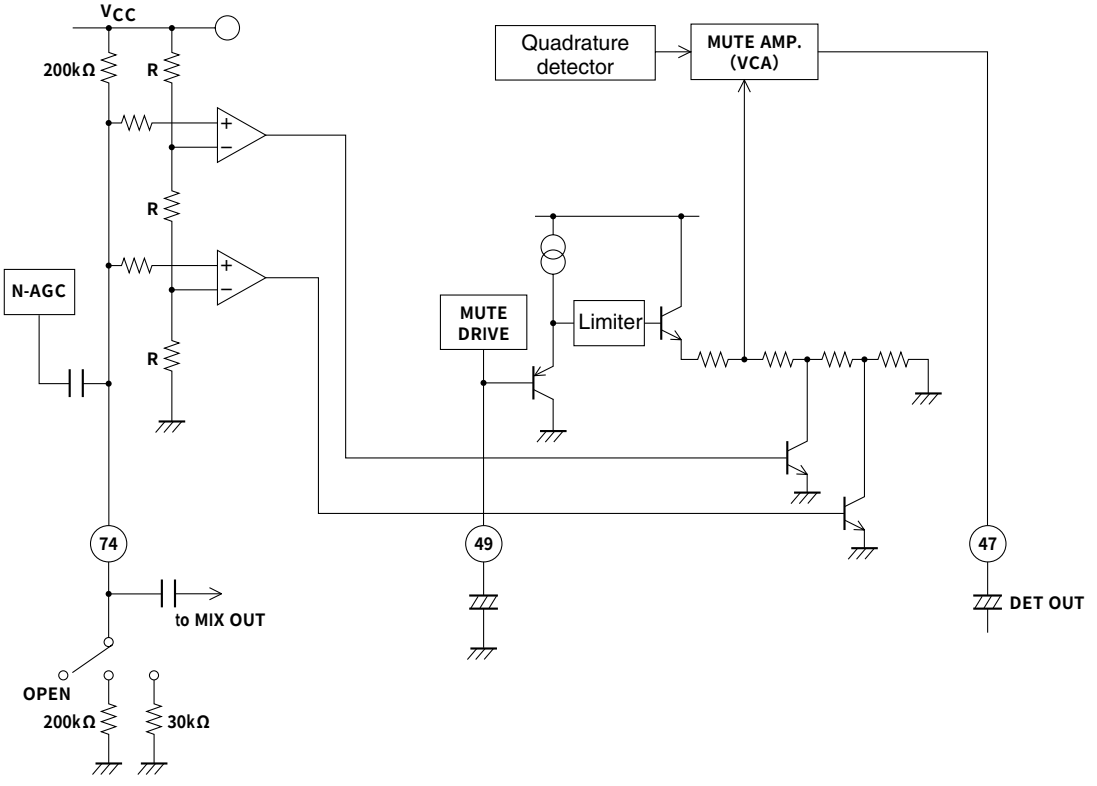


A13378

MUTE time constant

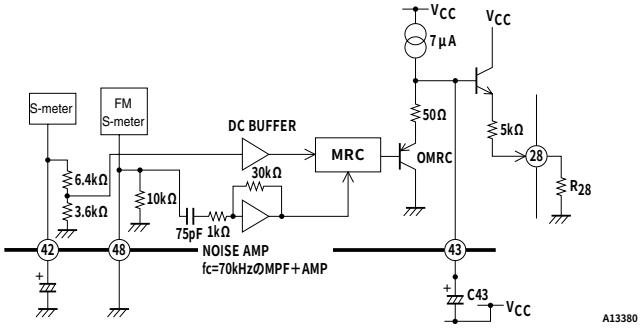
Attack $10\ k\Omega \times C49$

Release $50\ k\Omega \times C49$



A13379

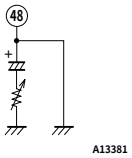
(7) MRC circuit



The stereo blend curve can be adjusted through the R28 external resistor.

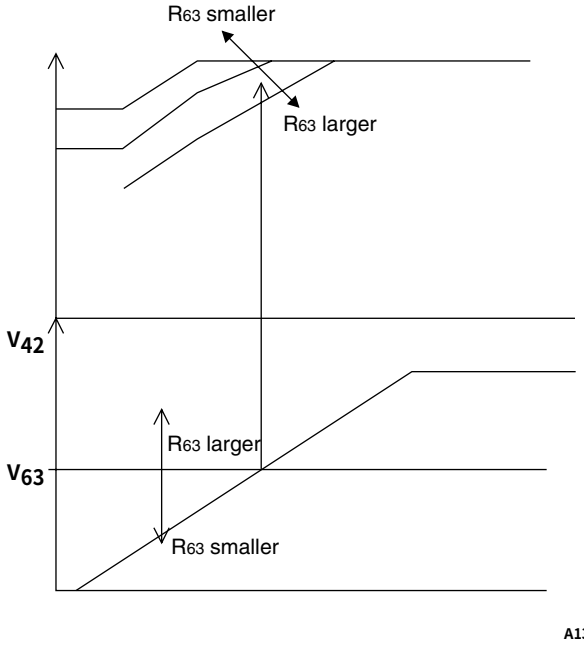
1) When there is no AC noise on pin 48
   $V42 = V43 - V_{BE}$
   ↑
   Q_{MRC}
   V43 is approximately 2.5 V when ANT input is 60 dBµ or higher.

2) Because the MRC noise amplifier gain is fixed, adjust MRC by reducing the AC input level.



3) The MRC attack and release are determined by C43 on pin 43.
   Attack 7 µA • C27
   Release 500 Ω • C27

(8) FM soft mute



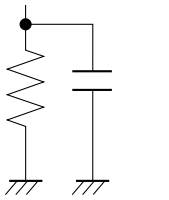
Compare the pin 63 MUTE ON adjusting voltage and the V42 S-meter voltage, and adjust the MUTE ON point.

(9) About the noise canceller

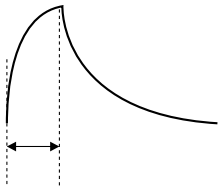
The noise canceller improves the characteristics by implementing the circuits that determine the gate time with a logic circuit.

Because a conventional noise canceller determines the time constant according to CR as shown in Fig. 5, the rise time is dependent on the CR, as shown in Fig. 6. This caused a delay in the rise, which resulted in a deterioration of noise filtering performance when the rise was delayed too much.

In the LA17000, the circuits that determine the gate time have been configured with logic, resulting in a faster rise and making more reliable noise filtering possible.

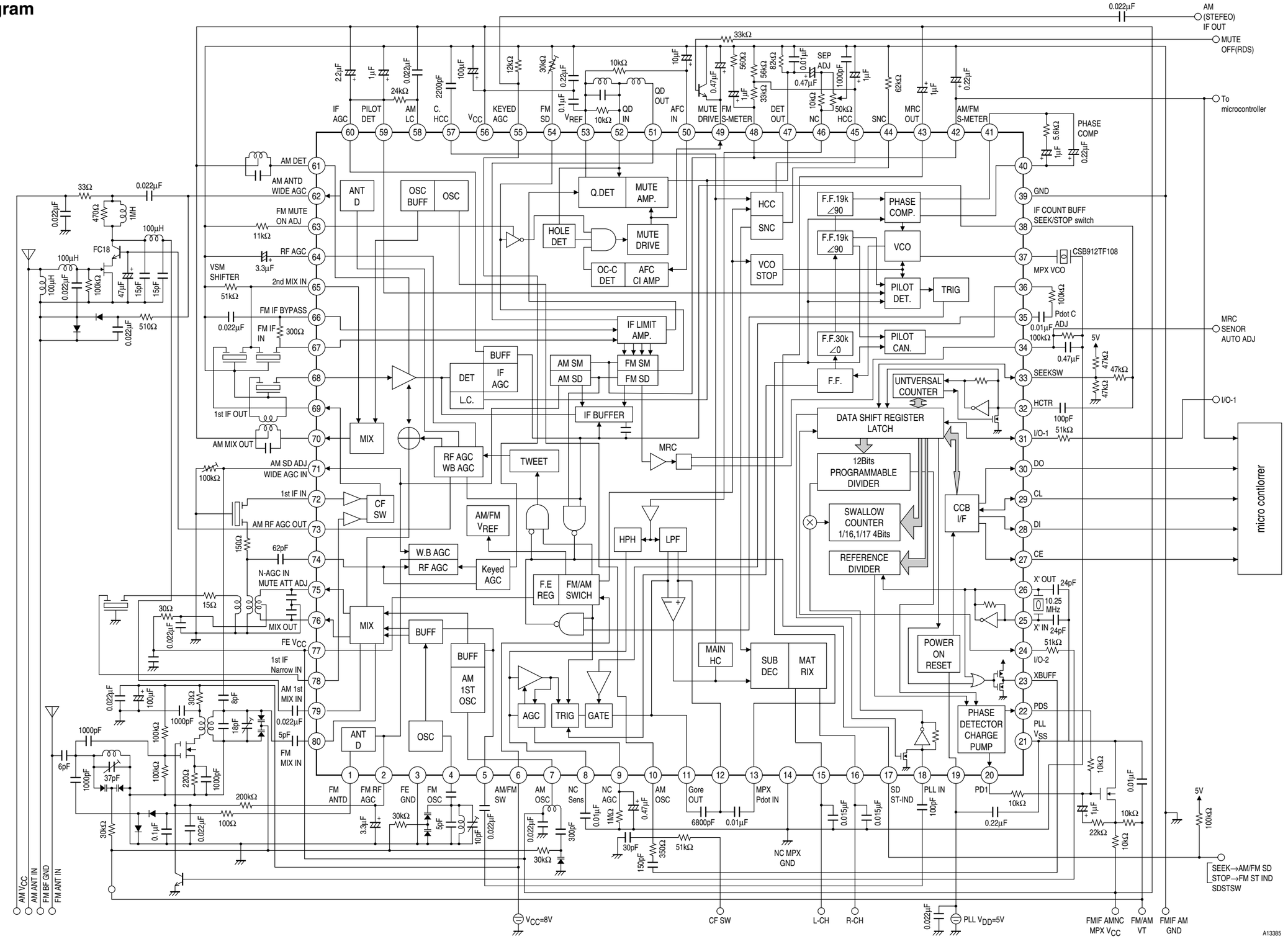


A13383



A13384

Block Diagram



Recommended External Components

Component name	Manufacturer	Component number	Component model number
AM loading coil	Toko Sumida Electronics Co., Ltd.	L1	7TL-269ANS-0720Z SA-1062
AM ANT-IN	Toko Sumida Electronics Co., Ltd.	L2	7PSU-385BNS-027Z SA-1048
AM RF LPF	Toko Sumida Electronics Co., Ltd.	L3	5VUS-A286LBIS-15327 SA-1051
AM choke coil	Toko Sumida Electronics Co., Ltd.	L4	8RB-187LY-222J RC875-222J
AM 2nd MIX coil	Toko Sumida Electronics Co., Ltd.	L7	5PG-5PGLC-5310N SA-264
AM IF coil	Toko Sumida Electronics Co., Ltd.	L8	7PSGTC-50002Y=S SA-1063/SA-1112
AM OSC1 coil	Toko Sumida Electronics Co., Ltd.	L9	7KSS-V666SNS-213BY SA-359
AM/FM MIX coil with selectivity switch	Toko	L10	7PSG-8261N-5202D=S
AM/FM MIX coil without selectivity switch	Sumida Electronics Co., Ltd. Toko	L10	SA-266 371DH-1108FYH
FM detection coil	Sumida Electronics Co., Ltd. Toko	L14	SA-208 DM600DEAS-8407GLF
FM OSC coil	Sumida Electronics Co., Ltd. Toko	L11	SA-125 (JP), SA-278 (US) T-666NF-251APZ (JP), T-666SNF-2471B (US)
FM RF coil	Sumida Electronics Co., Ltd. Toko	L12	SA-143 (JP), SA-250 (US) T-666NF-269X (JP), T-666SNF-246JA (US)
FM ANT coil	Sumida Electronics Co., Ltd. Toko	L13	SA-144 (JP), SA-231 (US) T-666NF-268Z (JP), T-666SNF-244X (US)
MPX ceramic oscillator	Murata Manufacturing Co., Ltd. Kyocera	VCO1	CSB912JF108 (912 kHz) KRB-912F108 (912kHz)
PLL X'tal oscillator	Nihon Dempa kogyo	VCO2	LN-P-0001 (10.25, 10.35 MHz)
FM ceramic filter	Murata Manufacturing Co., Ltd.	CF1	SFE 10.7MS3A50K-A
FM/AM narrow band ceramic filter	Murata Manufacturing Co., Ltd.	CF2	SFE 10.7 MTE
AM ceramic filter	Toko Murata Manufacturing Co., Ltd.	CF3	LFCM450H SFPS450H
AM pin diode	SANYO Electric Co., Ltd.	PIN1	1SV234/267
AMRF FET+TR	SANYO Electric Co., Ltd.	FET1	FC18
AM OSC1 varactor	SANYO Electric Co., Ltd.	VD2	SVC252/253
FM pin diode	SANYO Electric Co., Ltd.	PIN2	1SV234
FM RF amplifier FET	SANYO Electric Co., Ltd.	FET2	3SK263/264
FM RF/ANT/OSC varactor	SANYO Electric Co., Ltd.	VD3	SVC231/208

Crystal oscillator

Nihon Dempa Kogyo Co., Ltd.

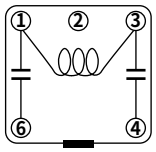
Frequency:	10.25 MHz	10.35 MHz
CL:	16pF	16pF
Model name:	LN-P-0001	LN-P-0001

Coil specifications

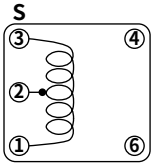
Sumida Electronics Co., Ltd.

[AM block]

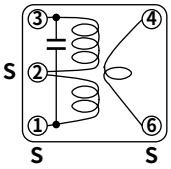
AM FILTER (SA-1051)



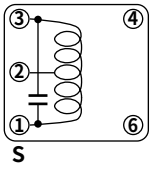
AM OSC (SA-359)



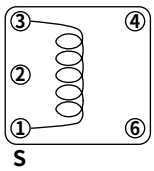
AM IF1 (SA-264)



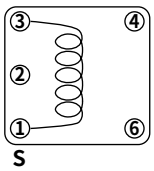
AM IF2 (SA-1063)



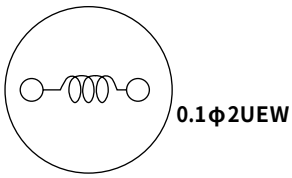
AM loading (SA-1062)



AM ANT IN (SA-1048)

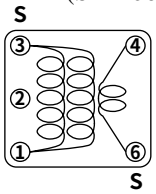


For AM RF amplifier (RC875-222J)

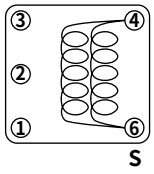


[FM block]

FM RF (SA-1060)

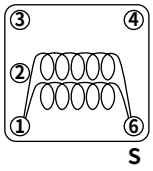


FM ANT (SA-1061)

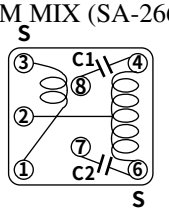


(without selectivity switch)

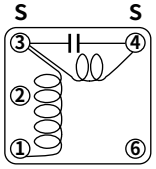
FM OSC (SA-1052)



FM MIX (SA-266)



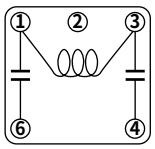
FM DET (SA-208)



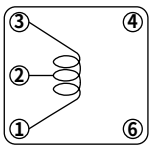
TOKO Co., Ltd.

[AM block]

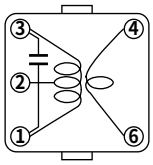
AM FILTER (A286LBIS-15327)



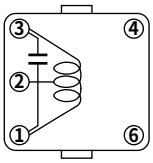
AM OSC (V666SNS-213BY)



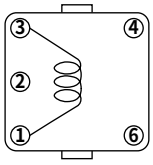
AM IF1 (7PSGTC-5001A=S)



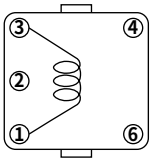
AM IF2 (7PSGTC-5002Y=S)



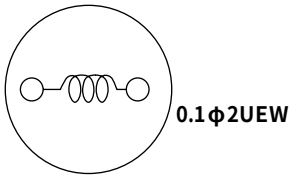
AM loading (269ANS-0720Z)



AM ANT IN (385BNS-027Z)

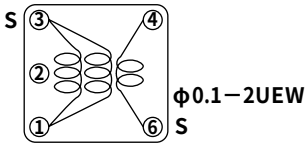


For AM RF amplifier (187LY-222)

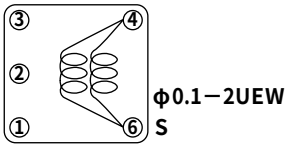


[FM block]

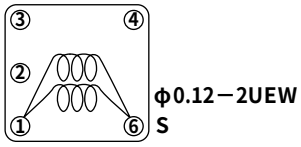
FM RF (V666SNS-208AQ)



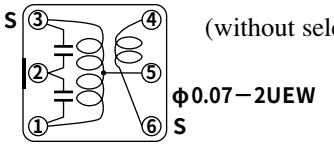
FM ANT (V666SNS-209BS)



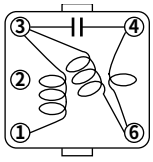
FM OSC (V666SNS-205APZ)



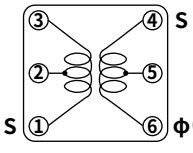
FM MIX (371DH-1108FYH)



FM DET (DM600DEAS-8407GLF)

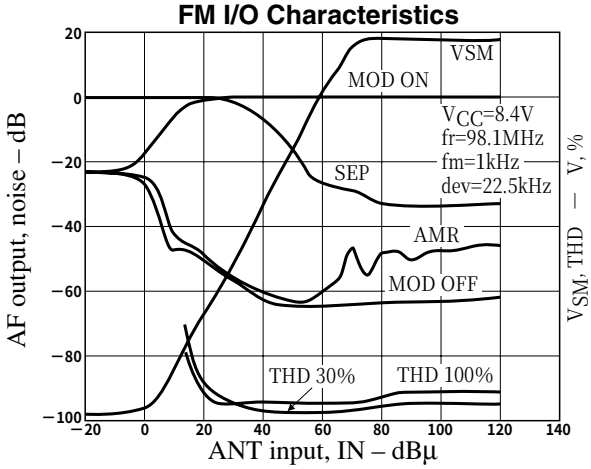


FM MIX (826IN-5202D=S)

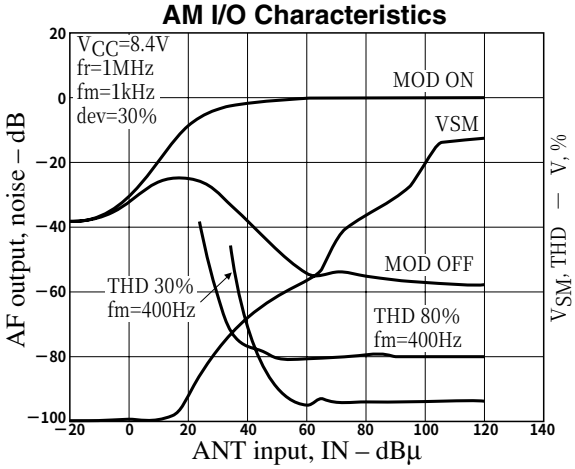


(with selectivity switch)
External 82P2 in parallel (1-G, 3-G)

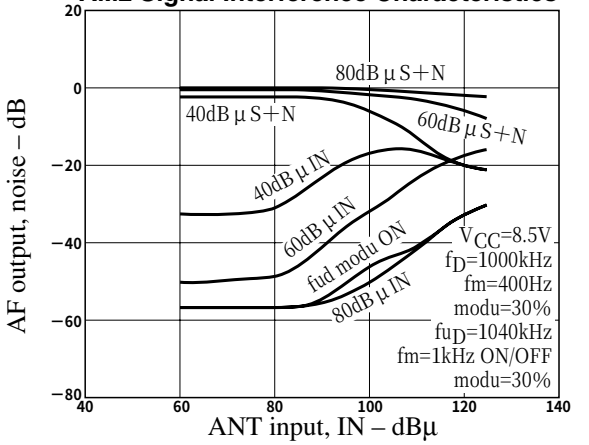
FM I/O Characteristics



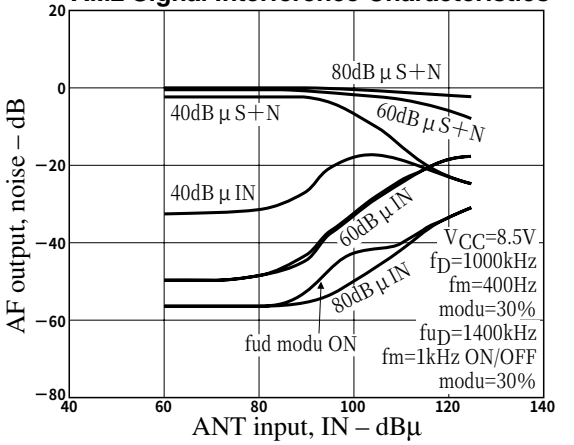
AM I/O Characteristics



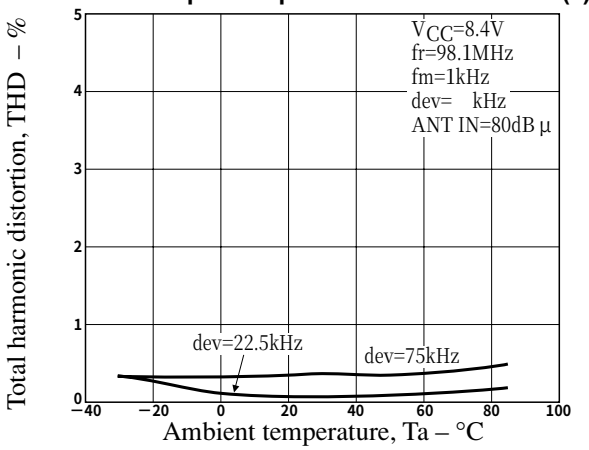
AM2 Signal Interference Characteristics



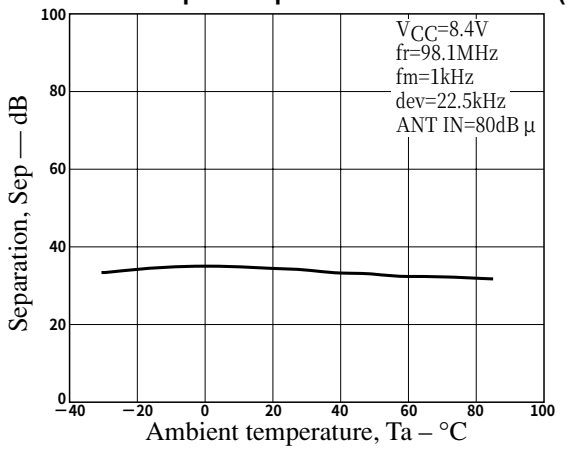
AM2 Signal Interference Characteristics



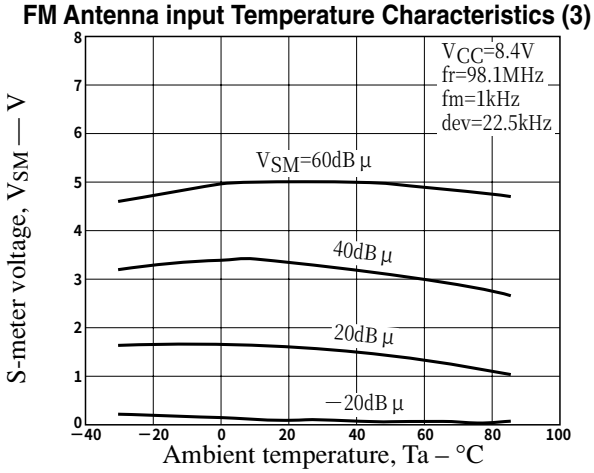
FM Antenna input Temperature Characteristics (1)



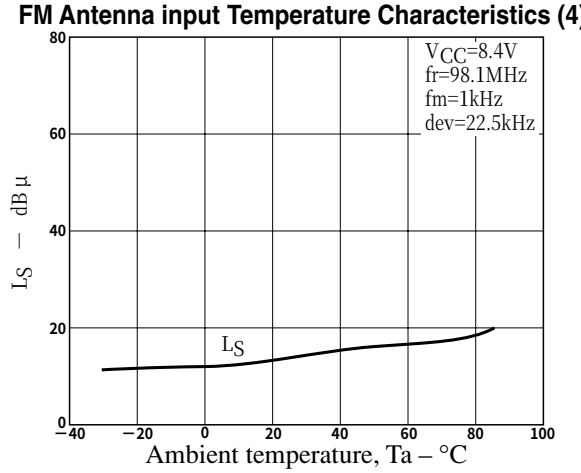
FM Antenna input Temperature Characteristics (2)



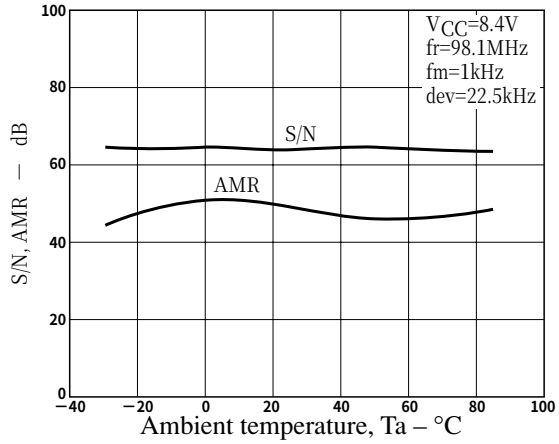
FM Antenna input Temperature Characteristics (3)



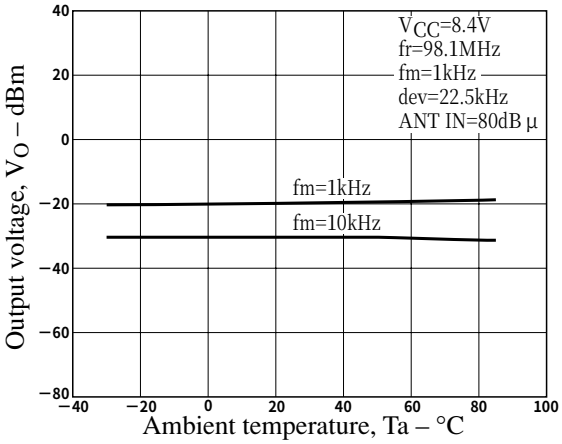
FM Antenna input Temperature Characteristics (4)



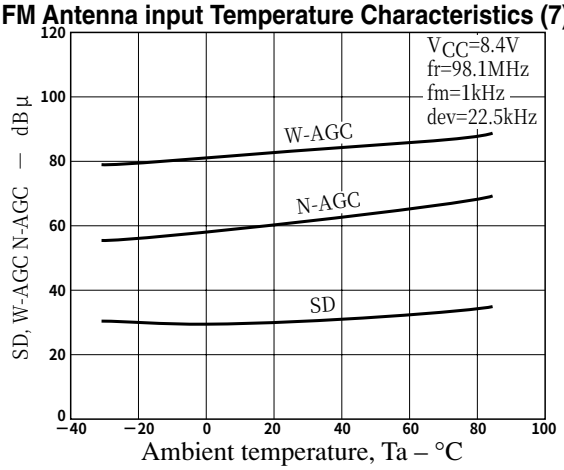
FM Antenna input Temperature Characteristics (5)



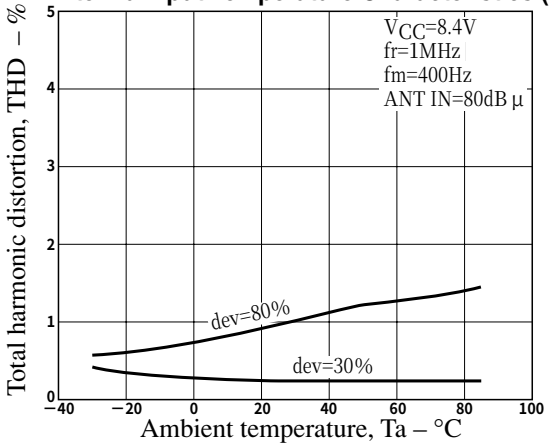
FM Antenna input Temperature Characteristics (6)



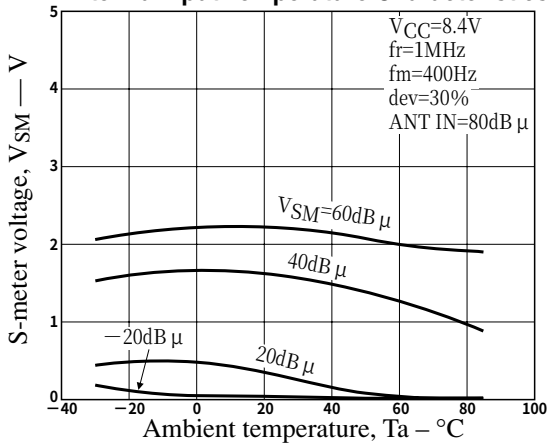
FM Antenna input Temperature Characteristics (7)



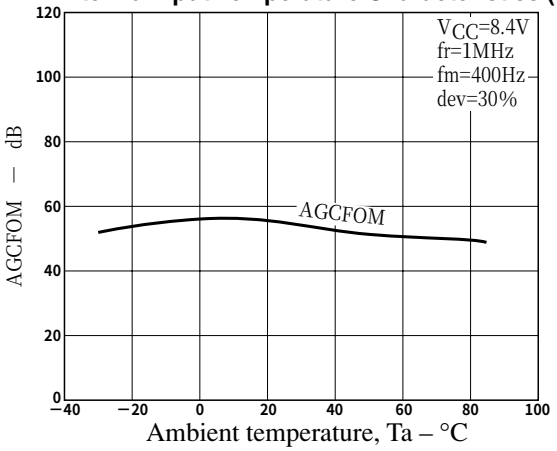
AM Antenna input Temperature Characteristics (1)



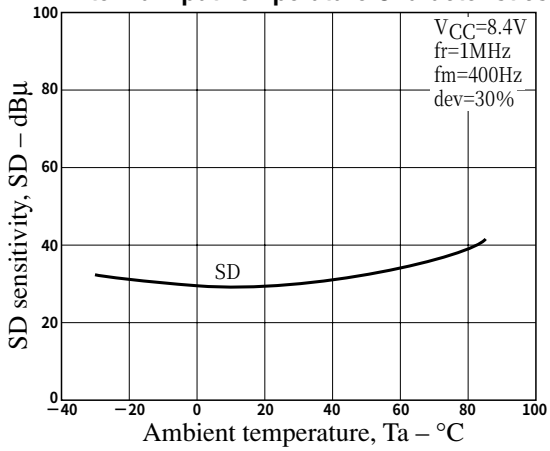
AM Antenna input Temperature Characteristics (2)



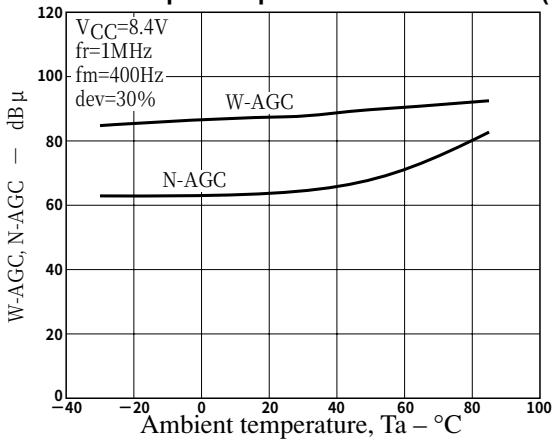
AM Antenna input Temperature Characteristics (3)



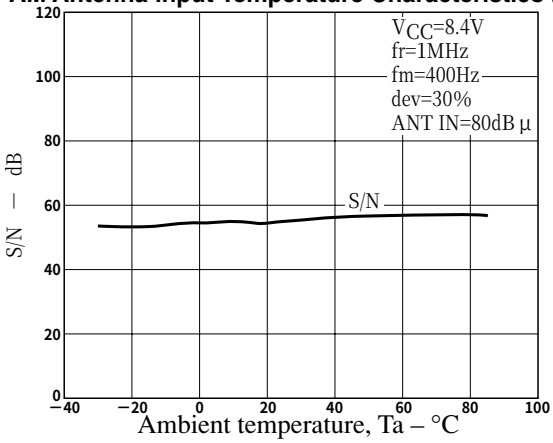
AM Antenna input Temperature Characteristics (4)



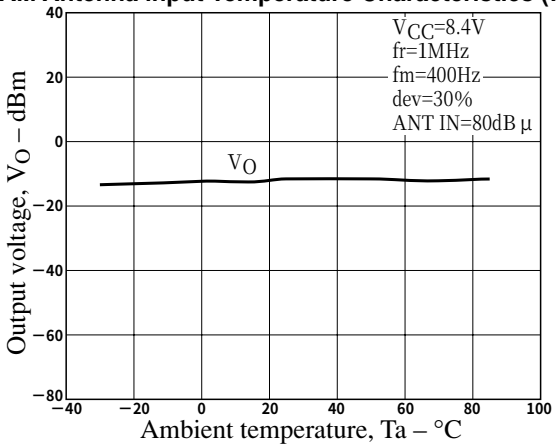
AM Antenna input Temperature Characteristics (5)



AM Antenna input Temperature Characteristics (6)



AM Antenna input Temperature Characteristics (7)



This catalog provides information as of June, 2001. Specifications and information herein are subject to change without notice.