Ordering number : EN5717

Monolithic Linear IC

LA6542M

4-Channel Bridge (BTL) Driver for CD-ROM

Overview

The LA6542M is a 4-channel bridge (BTL) driver developed for CD-ROM applications.

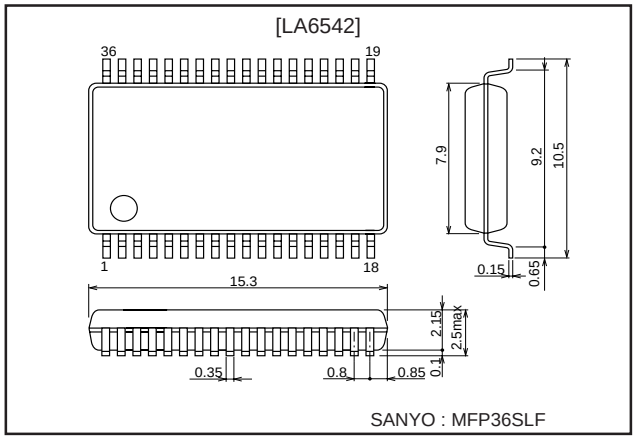
Functions

- 4-channel power amplifier with bridge circuit (BTL)
- $I_O$max: 1A
- Integrated muting circuit
  (MUTE: Output OFF at Low, output ON at High.
  MUTE1 is for channels 1 and 2, and MUTE2 for channels 3 and 4.)
- Slew rate 0.5 V/μs
- Integrated thermal shutdown circuit

Package Dimensions

unit: mm

3204-MFP36SLF



Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage 1	V_{CC}max		14	V
Maximum supply voltage 2	$V_S$max	V_S1, 2	14	V
Maximum input voltage	V_{IN}max	Input pins V_{IN}1 to 4	13	V
Mute pin voltage	V_{MUTE}max		13	V
Allowable power dissipation	Pd max	IC only	0.9	W
Operating temperature	Topr		–20 to +75	℃
Storage temperature	Tstg		–55 to +150	℃

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended operation voltage 1	V_{CC}		4 to 13	V
Recommended operation voltage 2-1	V_S1		4 to 13	V
Recommended operation voltage 2-2	V_S2		4 to 13	V

*$V_{CC} \geq V_S$1, 2

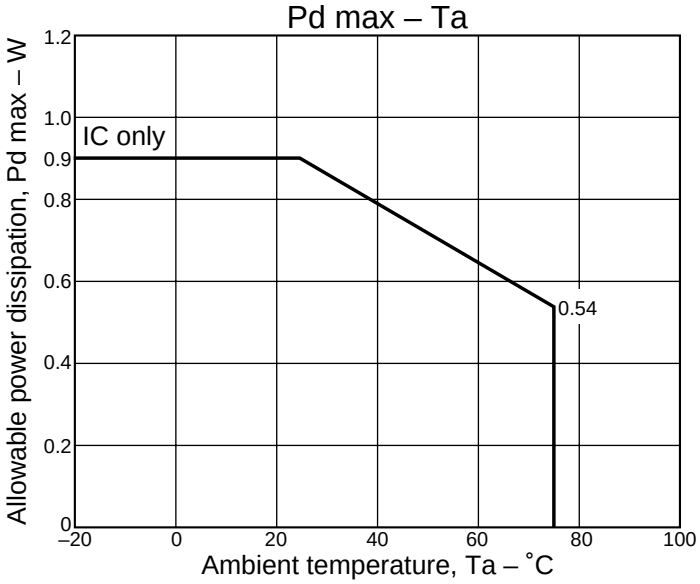
SANYO Electric Co., Ltd. Semiconductor Business Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Electrical Characteristics at V_{CC} = 12V, V_S = 5V, Ta = 25°C

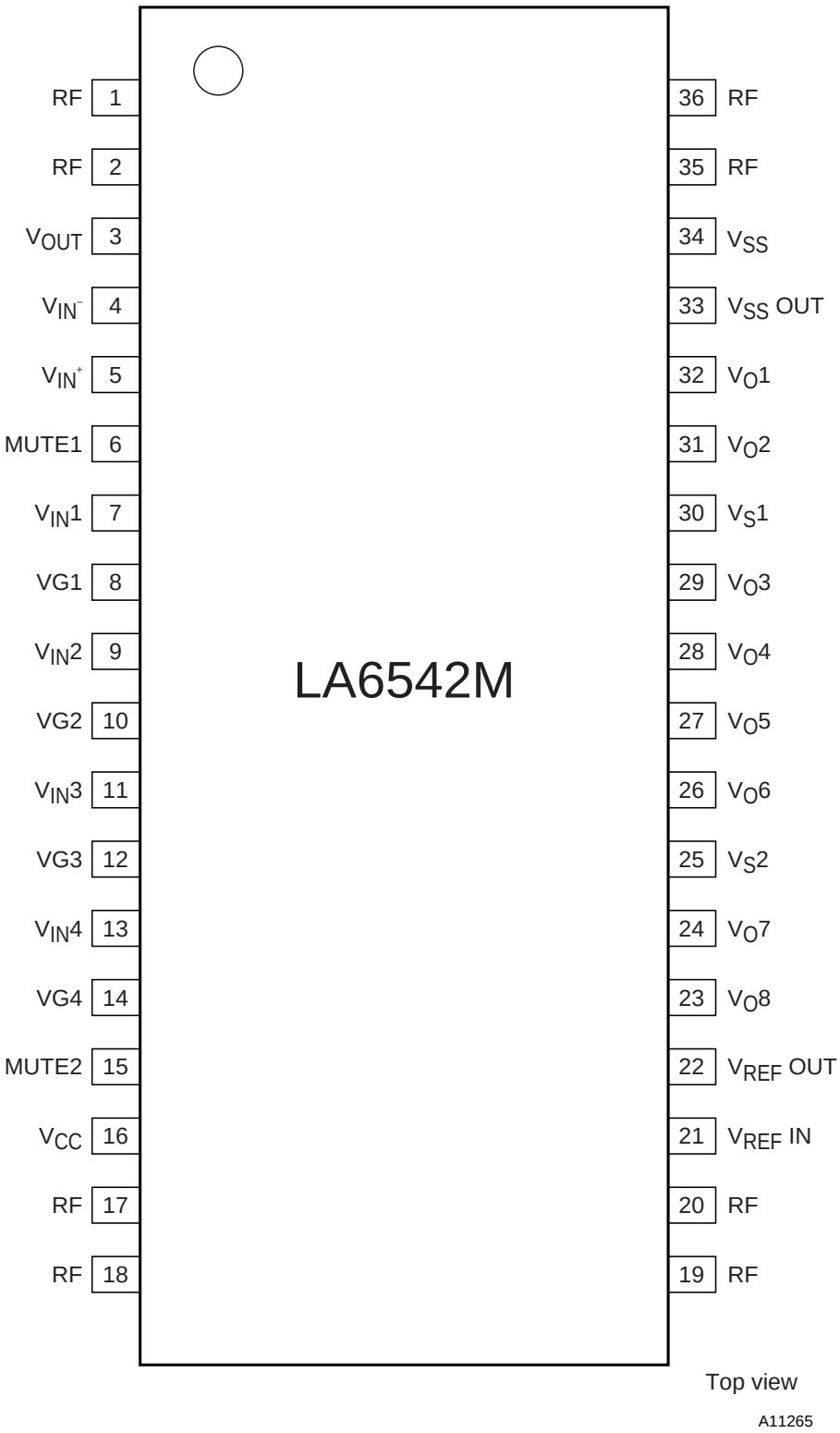
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
V_{CC} no-load current drain	$I_{CC}1$	All outputs ON (MUTE1, MUTE2: High)	5	10	20	mA
	$I_{CC}2$	All outputs OFF (MUTE1, MUTE2: Low)		5	10	mA
V_S1 no-load current drain	I_S1-1	CH1, 2 ON (MUTE1, MUTE2: High)		10	30	mA
	I_S1-2	CH1, 2 OFF (MUTE1, MUTE2: Low)			4	mA
V_S2 no-load current drain	I_S2-1	CH3, 4 ON (MUTE1, MUTE2: High)		10	30	mA
	I_S2-2	CH3, 4 OFF (MUTE1, MUTE2: Low)			4	mA
Output offset voltage	V_{OF}1 to 4	Potential difference between plus and minus outputs for CH1 to CH4	–50		50	mV
Input voltage range	V_{IN}	Input voltage range for V_{IN}1 to V_{IN}4	0.5		5	V
Output voltage (source)	Vsource	Plus and minus outputs at high level	4.4	4.7		V
		I_O = 700 mA				
(sink)	Vsink	Plus and minus outputs at low level		0.3	0.6	V
		I_O = 700 mA				
Closed circuit voltage gain	VG	Voltage gain between BTL amplifiers		6		dB
Slew rate	SR	(Note 1)		0.5		V/µs
Mute ON voltage	V_{MUTE}	MUTE1, MUTE2 voltage when output is ON (Note 2)		1.5	2	V
Mute ON current	I_{MUTE}	MUTE1, MUTE2 current when output is ON (Note 2)		6	10	µA

Note 1: Guaranteed design value

Note 2: MUTE works on all channels. At High, amplifier output is ON and at Low amplifier output is OFF (output impedance becomes HI).



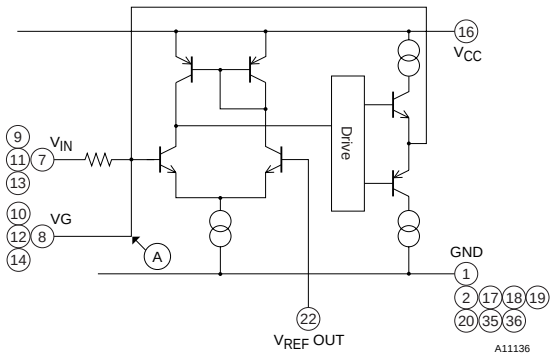
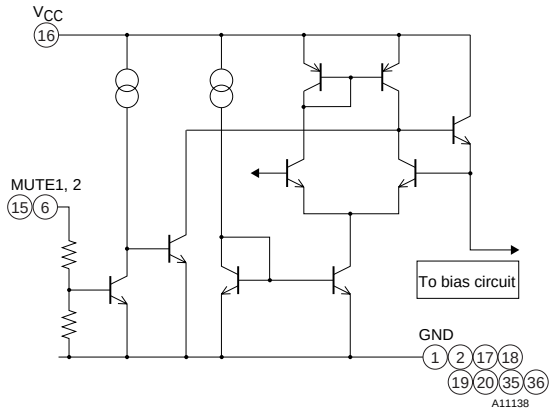
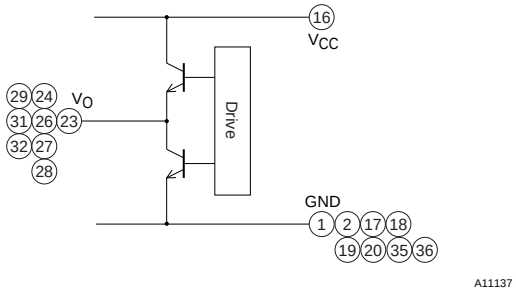
Pin Assignment



Top view

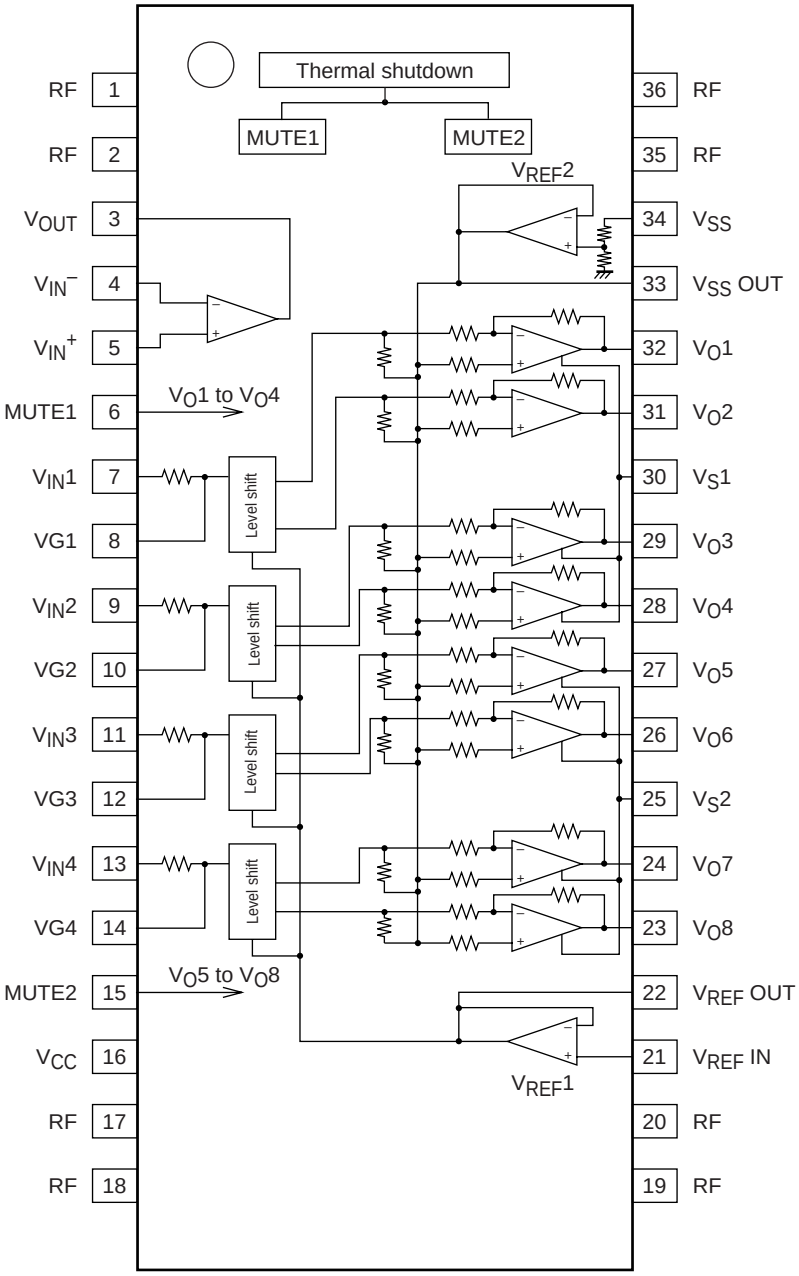
A11265

Pin Function

Pin number	Pin name	Equivalent circuit	Pin function
1, 2 17, 18 19, 20 35, 36	RF		Substrate (minimum potential)
7, 9 11, 13	$V_{IN}1$, $V_{IN}2$ $V_{IN}3$, $V_{IN}4$		Input pins for CH1 and CH2 Input pins for CH3 and CH4
8, 10 12, 14	VG1, VG2 VG3, VG4		Input pins for CH1 and CH2 (for gain adjustment) Input pins for CH3 and CH4 (for gain adjustment)
16	V_{CC}		Power supply
22	V_{REF}OUT		Level shift circuit reference voltage (V_{REF}1 buffer amplifier output*)
3	V_{OUT}		OP amp output
4	V_{IN}-		OP amp inverted input
5	V_{IN}+		OP amp non-inverted input
6 15	MUTE1 MUTE2		CH1, CH2 output ON/OFF CH3, CH4 output ON/OFF
21	V_{REF}IN		Level shift circuit reference voltage input (V_{REF} buffer amplifier input*)
23 24 26 27 28 29 31 32	V_O8 V_O7 V_O6 V_O5 V_O4 V_O3 V_O2 V_O1		CH4 inverted output (AMP8 output) CH4 non-inverted output (AMP7 output) CH3 inverted output (AMP6 output) CH3 non-inverted output (AMP5 output) CH2 inverted output (AMP4 output) CH2 non-inverted output (AMP3 output) CH1 inverted output (AMP2 output) CH1 non-inverted output (AMP1 output)
25	V_S2		CH3 (AMP5, AMP6), CH4 (AMP7, AMP8) output stage power supply
30	V_S1		CH1 (AMP1, AMP2), CH2 (AMP3, AMP4) output stage power supply
33	V_{SS}-OUT		Output stage reference voltage (V_{SS}1/2: typ) (V_{REF}2 buffer amplifier output*)
34	V_{SS}		Connect to VS1, VS2 (resistance split) to generate V_{SS}OUT

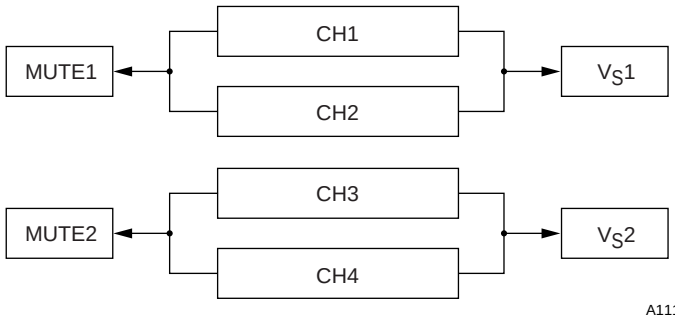
*See block diagram on next page.

Block Diagram



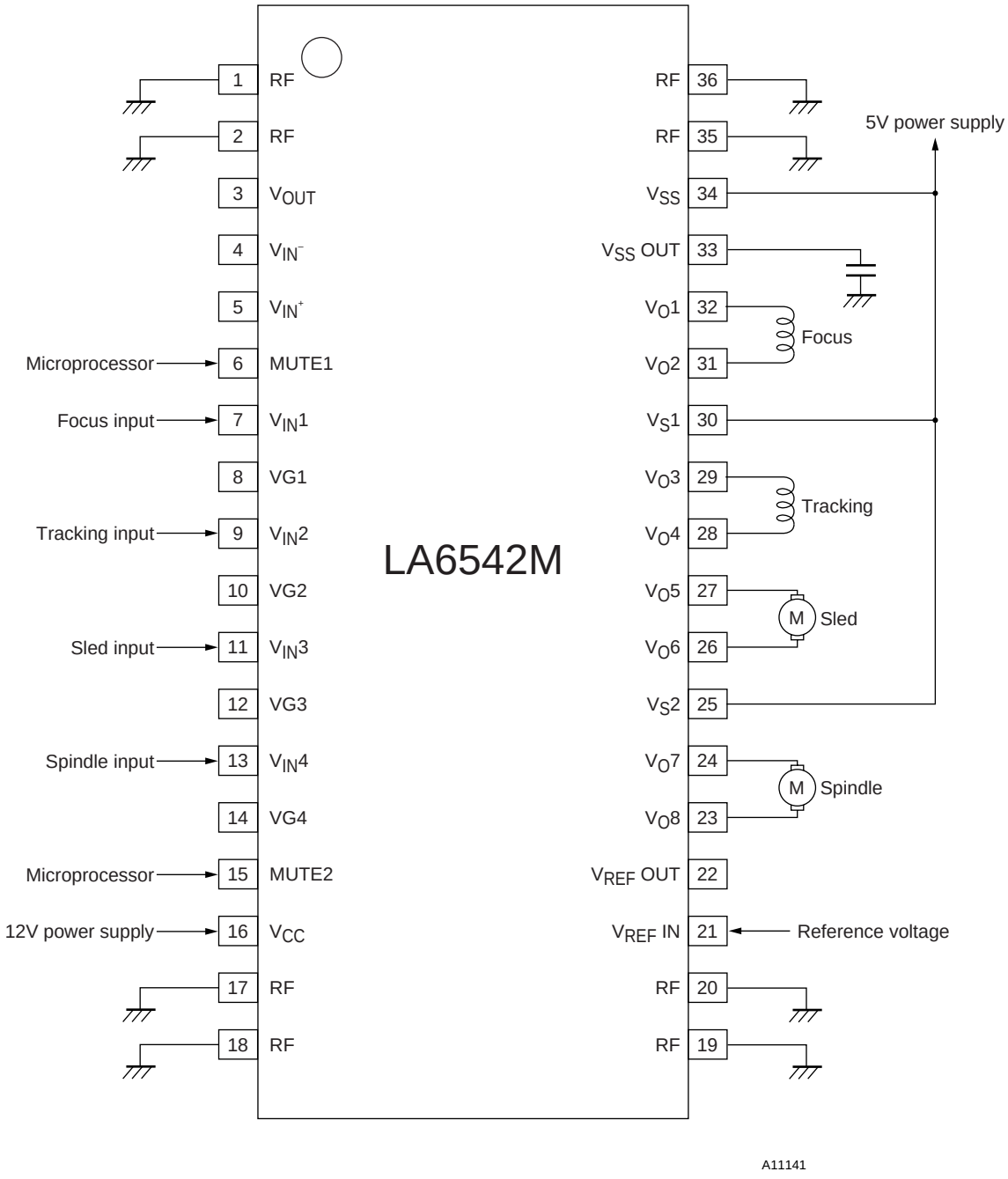
A11139

System Diagram (relationship between power supply and MUTE)



A11140

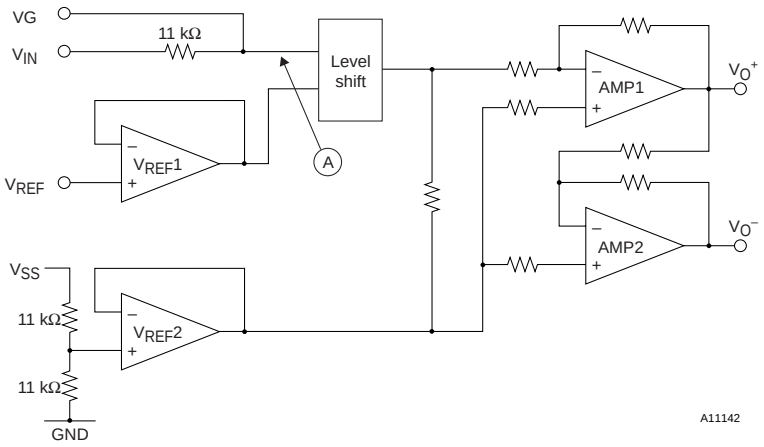
Sample Application Circuit



Gain Setting (input pins and adjustment pins)

A simplified diagram of V_{IN} and VG is shown below.

1) Consider an 11 kΩ (typ.) resistor inserted between V_{IN} and VG.
2) When not the pin VG but the pin V_{IN} is used alone, the BTL gain (between V_O^+ and V_O^-) is set to 6 dB (0 dB for AMP only). This also applies for the case when V_{IN} is not used and an 11 kΩ external resistor is connected to VG for input.
3) Gain is set by the input impedance as seen from point A.
   When VG only is used and the external resistor is R, the BTL gain (between V_O^+ and V_O^-) is
   20 log (11 kΩ/R) + 6 dB.
   When an 11 kΩ resistor is inserted between V_{IN} and VG, and input is via V_{IN}, the combined resistance Rz as seen from point A is Rz = 5.5 kΩ. Gain is
   20 log (11 kΩ /5.5 kΩ) + 6 dB = 12 dB.



Offset Voltage

This IC incorporates a level shifter circuit. The input references the V_{REF} to be applied, and references the voltage ($V_{SS} - V_{BE}$ (0.7))/2V to be output.