Monolithic Digital IC

LB1945H



PWM Current Control Type Stepping Motor Driver

Preliminary Features

- PWM current control (external excitation)
- Load current digital selection (1–2, W1–2, and 2 phase excitation drives possible)
- Built-in upper/lower diode
- Simultaneous ON prevention function (feedthrough current prevention)
- Built-in thermal shutdown circuit
- Built-in noise canceler

Package Dimensions

unit: mm

3233-HSOP28H



Specifications

Absolute Maximum Ratings at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum motor supply voltage	Vвв тах		30	V
Output peak current	I OPEAK	$tw \le 20 \ \mu s$	1.0	А
Output continuous current	I o max		0.8	А
Logic supply voltage	Vcc max		6.0	V
Logic input voltage range	VIN max		-0.3 to VCC	V
Emitter output voltage	VE max		1.0	V
Allowable power dissipation	Pd max	Ta = 25°C, with specified substrate*	1.9	W
Operating temperature	Topr		-20 to +90	°C
Storage temperature	Tstg		-55 to +150	°C

* Specified substrate: $114.3 \times 76.1 \times 1.6$ mm³, glass epoxy

Allowable Operating Ranges at Ta = $25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Motor supply voltage	Vвв		10 to 28	V
Logic supply voltage	Vcc		4.75 to 5.25	V
Reference voltage	Vref		1.5 to 5.0	V

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Parameter		Currente e l	Conditions	Ratings			
		Symbol Conditions	min	typ	max	Unit	
Output Block	Output stage supply current	I BB ON	I ₁ = 0.8V, I ₂ = 0.8V, ENABLE = 0.8V	0.5	1.0	2.0	mA
		BB OFF	ENABLE = 3.2V			0.2	mA
	Output saturation voltage 1	V osat 1	lo = +0.5A sink		0.3	0.5	V
	2	V osat 2	lo = +0.8A sink		0.5	0.7	V
	3	V osat 3	lo = –0.5A source		1.6	1.8	V
	4	V osat 4	lo = -0.8A source		1.8	2.0	V
	Output leakage current	l o1(leak)	Vo = V sink			50	μΑ
		l o2(leak)	Vo = 0V source	-50			μΑ
	Output sustain voltage	V sus	L = 3.9 mH lo = 1.0A *1	30			V
	Logic supply current	I CC ON	I ₁ = 0.8V, I ₂ = 0.8V, ENABLE = 0.8V	50.0	70.0	92.0	mA
		I CC OFF	ENABLE = 3.2V	7.0	10.0	13.0	mA
	Input voltage	Vін		3.2			V
		V IL				0.8	V
옹	Input current	Ιн	V IH = 3.2V	35	50	65	μΑ
Blo		I⊫	V IL = 0.8V	7	10	13	μΑ
gic	Set current control threshold	Vref/Vsen	$I_1 = 0.8V, I_2 = 0.8V$	9.5	10	10.5	
, Lo	value		$I_1 = 3.2V, I_2 = 0.8V$	13.5	15	16.5	
			$I_1 = 0.8V, I_2 = 3.2V$	25.5	30	34.5	
	Reference current	l ref	Vref = 5.0V, I ₁ = 0.8V, I ₂ = 0.8V	17.5	25	32.5	μΑ
	CR pin current	I CR	CR = 1.0V	-1.0			mA
	Thermal shutdown temperature	T TSD			170		°C
	Temperature hysteresis width	ΔT_{TSD}			40		°C

Electrical Characteristics at Ta = 25° C, VBB = 24V, Vcc = 5V, VREF = 5.0V

*1: Assured design target value, not measured

Truth Table

ENABLE	PHASE	OUTA	OUTA-
L	Н	Н	L
L	L	L	Н
Н	-	OFF	OFF

1	12	Output current
L	L	Vref / $(10 \times \text{Re}) = \text{IOUT}$
н	L	Vref / (15 × RE) = IOUT × 2/3
L	Н	Vref / $(30 \times R_E) = Iout \times 1/3$
н	Н	0

Note: Output is OFF when ENABLE = H or when I1 = I2 = H.

Block Diagram



Pin Assignment



Sample Application Circuit



The fin on the bottom of HSOP-28H package and the fins between pins 7 and 8 and 21 and 22 should be grounded.

Pin Description

Pin name	Pin number	Function
Vвв1	7	Output stage power supply voltage pin.
Vвв2	24	Cathode pin for the upper-side diodes.
E1	5	Insert resistor R _E between these pins and ground to control set current.
E2	23	
OUTA	2	Output pins.
OUTA-	1	
OUTB	27	
OUTB-	28	
GND	14	Ground pin.
S-GND	15	Sense ground pin.
D–GND	6	Lower-side internal diode ground (anode)
	22	
CR	21	Triangular wave chopping with CR constant setting.
		Triangular wave OFF time is noise cancel time.
Vref1	13	Output current setting pins.
Vref2	16	(Output current is set by inputting a 1.5V to 7.5V voltage.)
PHASE1	9	Output phase select input pin.
PHASE2	20	High input: $OUTA = H$, $OUTA^- = L$
		Low input: $OUTA = L$, $OUTA^- = H$
ENABLE1	10	Output ON/OFF setting input pins.
ENABLE2	19	High input: output OFF
		Low input: output ON
IA1, IA2	12, 11	Output current setting digital input pins.
Ib1, Ib2	17, 18	Current is set to 1/3, 2/3, 1 by High and Low combinations.
Vcc	8	Logic block power supply voltage pin.

Usage Notes

1. V_{REF} pin

Because the V_{REF} pin is used as reference voltage input pin for the current setting, care must be taken to prevent noise from affecting the input.

2. GND pin

Because this IC switches large currents, the ground pattern must be designed with care. The fin on the bottom of the package and the fins between pins 7 and 8 and 21 and 22 should be grounded. Low-impedance patterns should be used in blocks where large currents flow, and these blocks should be separated from low-level signal blocks. In particular, the ground of the sense resistor R_E at pin E should be located close to the IC ground. Pattern layout should be designed so that the capacitors between V_{CC} and ground and V_{BB} and ground are close to V_{CC} and V_{BB} .

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