Ordering number : EN5944

CMOS IC

LC5824, LC5823, LC5822

4-Bit Single-Chip Microcontrollers Featuring 4 KB to 8 KB of ROM, 1 Kbit of RAM, and an LCD Driver for Medium Speed Small-Scale Control Applications

Overview

The LC5822, LC5823, and LC5824 are CMOS microcontrollers that feature the low-voltage operation required for battery-power applications and that provide 4 KB, 6 KB, or 8 KB of ROM, 1 kilobit of RAM, and an LCD driver.

These microcontrollers support an instruction set based on that of the earlier LC5800, LC5812, and LC5814 for excellent efficiency in software development.

Applications

- LCD display in multi-function watches, timers, and other products
- Control and LCD display in timers
- Control and LCD display in miniature test equipment, health maintenance equipment, and other products
- These microcontrollers are optimal for products that include an LCD display, especially battery powered products.

Wide Allowable Operating Ranges

Power options supply	Cycle times	Supply voltage range	Notes
EXT-V	10 µs	V_{DD} = 2.3 to 3.6 V	When an 800-kHz ceramic oscillator is used
EXT-V	20 µs	V_{DD} = 2.3 to 3.6 V	When an 400-kHz ceramic oscillator is used
EXT-V	61 µs	V_{DD} = 2.3 to 3.6 V	When an 65-kHz crystal oscillator is used
EXT-V	122 µs	V_{DD} = 2.0 to 3.6 V	When an 32-kHz crystal oscillator is used
Li	122 µs	V_{DD} = 2.6 to 3.6 V*	When an 32-kHz crystal oscillator is used
Ag	122 µs	V_{DD} = 1.3 to 1.65 V	When an 32-kHz crystal oscillator is used

Note*: When the backup flag is set, the BAK pin is connected to V_{DD}.

Features

- These microcontrollers are high-end versions of the LC5800 and provide the following features.

Low Current Drain * In halt mode (typical)

- Ceramic oscillator 400 kHz (3.0 V) 200 µA
- Crystal oscillator 32 kHz (1.5 V, Ag specifications) 3.0 µA (LCD biases other than 1/3) 4.5 µA (LCD drive: 1/3 bias)
- Crystal oscillator 32 kHz (3.0 V, Li specifications) 2.0 µA (LCD biases other than 1/3) 6.0 µA (LCD drive: 1/3 bias)

Timer and Counter Functions

- One 8-bit programmable timer (May be used as an event counter)
- One 8-bit programmable reload timer
- Time base timer (for clocks)
- Watchdog timer
- 8-bit serial I/O (3-pin synchronous system)

Standby Functions

- Clock standby function (halt mode)
  Only the oscillator circuits, the divider circuit, and the LCD driver operate. All other internal operations are stopped. This provides a power-saving function in which current drain is minimized, and allows a clock function to be implemented easily with low power dissipation. Furthermore, low-speed and high-speed modes can be implemented by setting the operating modes of the two oscillator circuits.
- Full standby function (hold mode)
- Halt mode can be cleared by any of two external and two internal interrupts.

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Improved I/O Functions
- External interrupt pins
- Input pins that can clear halt mode: 10 pins (maximum)
- Input ports with input resistors that can be controlled from software: 8 pins (maximum)
- Pins with a function that prevents the input port floating state: 8 pins (maximum)
- LCD drive pins: 4 pins (common), 42 pins (segment outputs)
- General-purpose I/O ports: 16 pins (when all 4 P port pins are used)
- General-purpose inputs: 8 pins
- General-purpose outputs (1): 1 pin (the ALM pin)
- General-purpose outputs (2): 42 pins (when all 42 of the LCD segment outputs are switched over to function as general-purpose outputs)
- 8-bit serial output port: 1 set (3 pins: output, input, and clock)

Functional Overview
- Program ROM: 4096 × 16 bits LC5824
  3072 × 16 bits LC5823
  2048 × 16 bits LC5822
- Internal RAM: 256 × 4 bits
- All instructions execute in a single cycle.
- Extensive set of interrupt functions for clearing halt and hold mode
  — 8 halt mode clearing functions
  — 5 hold mode clearing functions
  — 6 interrupt functions
  — Subroutines can be nested up to 8 levels (Special-purpose registers that are shared with the interrupt function are built in.)
- Powerful hardware to increase system processing capacity
  — Segment port related hardware
    Built-in segment PLA circuit
    Built-in segment decoder
    Support for six different LCD drive specifications
    Outputs can be switched to CMOS levels
  — Built-in 8-bit synchronous serial I/O circuit
  — 8-bit read/write timer (plus a separate 8-bit prescaler; can be used as and event counter)
  — 8-bit reload timer (plus built-in 8-bit prescaler)
  — Built-in 8-bit prescaler (for use with timer 1, timer 2, and the serial counter)
  — All of RAM can be used a working area (RAM bank system)
  — Dedicated data pointer register for RAM access
  — 15-stage divider circuit for clocks (also used as the LCD voltage alternation frequency generator)
  — 8-bit table reference function (reads 8-bit ROM data)
  — Chattering prevention circuit (on two ports)
  — Alarm signal generation circuit
- LCD panel drive output pins with high flexibility (42 pins)

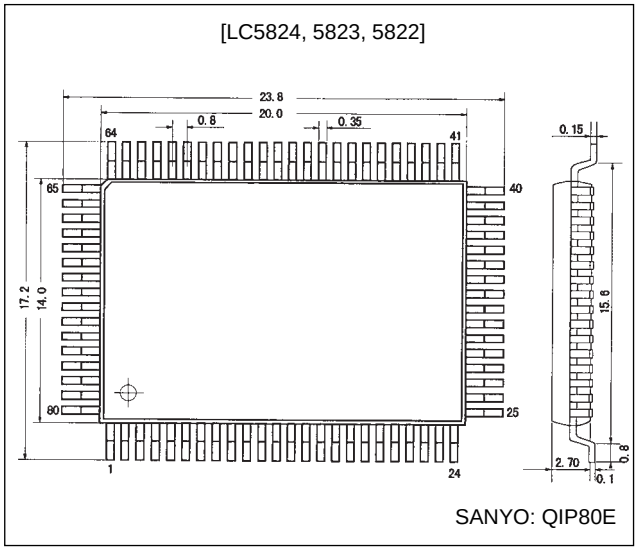
Drive system	Number of driven segments	Required number of common pins
bias · duty	168 segments	4 pins
bias · duty	126 segments	3 pins
bias · duty	168 segments	4 pins
bias · duty	126 segments	3 pins
bias · duty	84 segments	2 pins
Static drive	42 segments	1 pin

  — The LCD output pins can be switched to function as general-purpose outputs.
    CMOS/p-channel/n-channel type combinations: Up to 42 pins
  — An alternation frequency appropriate for the LCD panel used can be selected.
- An oscillator appropriate for your system's specifications can be selected.
  — A 32- or 65-kHz crystal oscillator can be selected (Used when a clock function is required or for low current drain operation.)
  — A ceramic oscillator with a frequency from 400 kHz to 2 MHz can be selected (when high-speed operation is required.)
    Available delivery formats: QIP-80 and chip

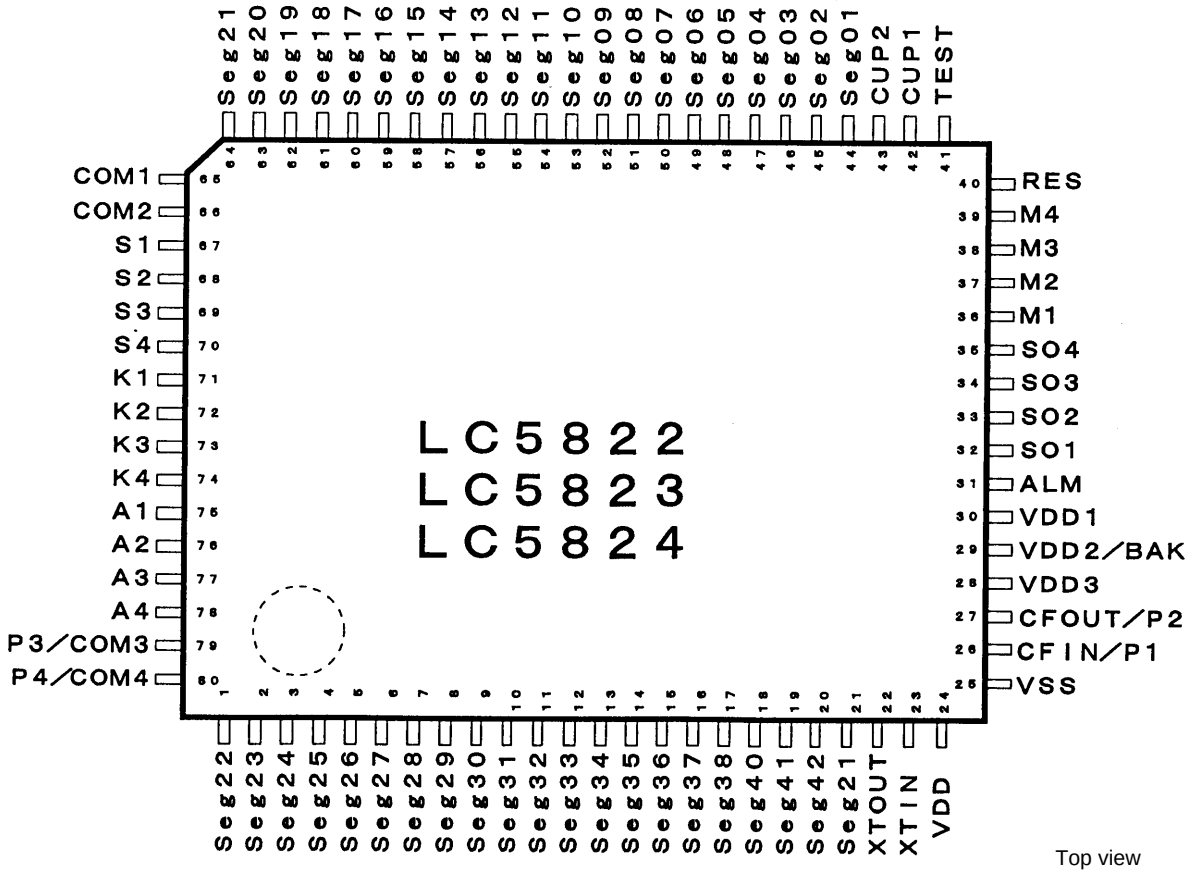
Package Dimensions

unit: mm

3174-QFP80E



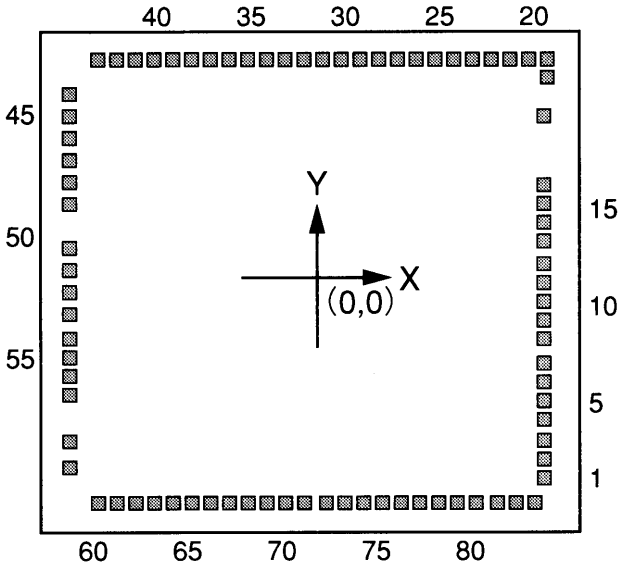
Pin Assignment



Top view

Pad Arrangement

Chip size: 4.92 mm × 5.15 mm
Pad size: 120 µm × 120 µm
Chip thickness 480 µm (chip specifications)



Pad Coordinates

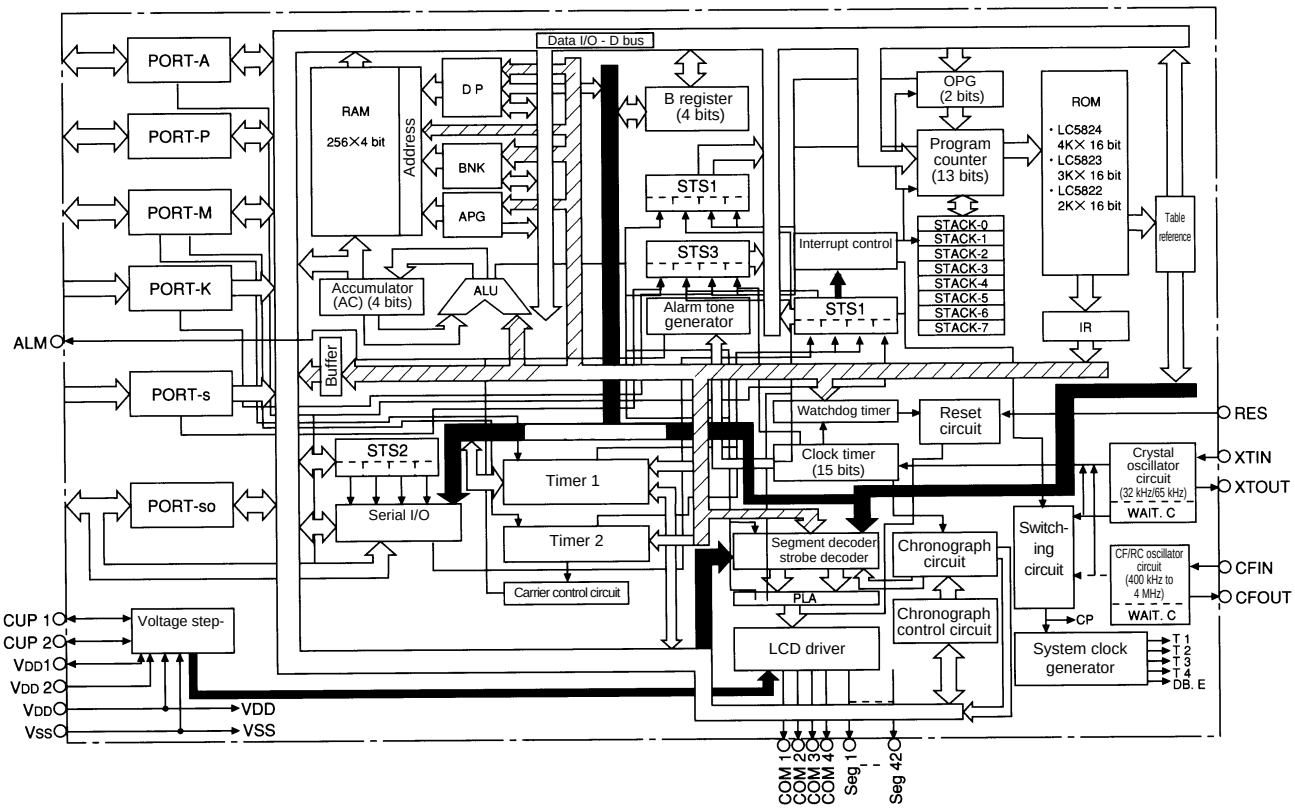
PAD No.	Pin	Coordinates	
		X µm	Y µm
60	Seg 22	–2030	–2178
61	Seg 23	–1850	–2178
62	Seg 24	–1670	–2178
63	Seg 25	–1490	–2178
64	Seg 26	–1310	–2178
65	Seg 27	–1130	–2178
66	Seg 28	–950	–2178
67	Seg 29	–770	–2178
68	Seg 30	–590	–2178
69	Seg 31	–410	–2178
70	Seg 32	–230	–2178
71	Seg 33	–50	–2178
72	Seg 34	122	–2178
73	Seg 35	302	–2178
74	Seg 36	482	–2178
75	Seg 37	662	–2178
76	Seg 38	842	–2178
77	Seg 39	1022	–2178
78	Seg 40	1202	–2178
79	Seg 41	1382	–2178
80	Seg 42	1562	–2178
81	XC	1774	–2178
82	XTOUT	1954	–2178
83	XTIN	2134	–2178
1	V_{DD}	2257	–1959
2	V_{SS}	2257	–1779
3	CFIN/P1	2257	–1599
4	CFOUT/P2	2257	–1402

PAD No.	Pin	Coordinates	
		X µm	Y µm
5	$V_{DD}3$	2257	–1212
6	$V_{DD}2$/BAK	2257	–1032
7	$V_{DD}1$	2257	–852
8	ALM	2257	–601
9	SO1	2257	–419
10	SO2 I/O port	2257	–236
11	SO3 I/O port	2257	56
12	SO4 I/O port	2257	132
13	M1	2257	364
14	M2 I/O port	2257	544
15	M3 I/O port	2257	724
16	M4 I/O port	2257	904
17	RES I/O port	2257	1636
18	Test	2330	1998
19	Test	2330	2178
20	TST	2150	2178
21	CUP1	1970	2178
22	CUP2	1790	2178
23	Seg 1	1606	2178
24	Seg 2	1426	2178
25	Seg 3	1246	2178
26	Seg 4	1066	2178
27	Seg 5	886	2178
28	Seg 6	706	2178
29	Seg 7	526	2178
30	Seg 8	346	2178
31	Seg 9	166	2178
32	Seg 10	–14	2178

PAD No.	Pin	Coordinates	
		X µm	Y µm
33	Seg 11	–194	2178
34	Seg 12	–374	2178
35	Seg 13	–546	2178
36	Seg 14	–726	2178
37	Seg 15	–906	2178
38	Seg 16	–1086	2178
39	Seg 17	–1266	2178
40	Seg 18	–1446	2178
41	Seg 19	–1626	2178
42	Seg 20	–1806	2178
43	Seg 21	–1986	2178
44	COM1	–2270	1871
45	COM2	–2270	1628
46	S1	–2270	1367
47	S2 Input port	–2270	1140
48	S3 Input port	–2270	960
49	S4 Input port	–2270	734
50	K1	–2270	328
51	K2 Input port	–2270	88
52	K3 Input port	–2270	–140
53	K4 Input port	–2270	–380
54	A1	–2270	–593
55	A2 I/O ports	–2270	–773
56	A3 I/O ports	–2270	–953
57	A4 I/O ports	–2270	–1133
58	COM3/P3	–2270	–1602
59	COM4/P4	–2270	–1846

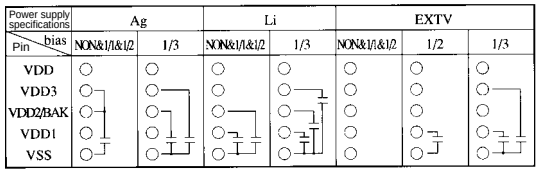
Note:
- The pin numbers are the QIP-80E mass-production package pin numbers.
- The test pin (TST) must be connected to V_{SS}.
- Pads number 42 and 43 in the chip version must be left open.
- Do not use solder dip techniques to mount the QIP-80E package version.
- In the chip version, the substrate must be either connected to V_{SS} or left open.

System Block Diagram



RAM: Data memory
ROM: Program memory
DP: Data pointer register
BNK: Bank register
APG: RAM page flag
AC: Accumulator
ALU: Arithmetic and logic unit
B: B register
OPG: ROM page flag
PC: Program counter
IR: Instruction register
STS1: Status register 1
STS2: Status register 2
STS3: Status register 3
STS4: Status register 4
PLA: Programmed logic array used for segment data and strobe functions
WAIT.C: Wait time counter

Pin Functions

Pin No.	Pin	I/O	Function	Options	Status at reset
24 25	V_{DD} V_{SS}	— —	Power supply		
30 29 28	$V_{DD}1$ $V_{DD}2$/BAK $V_{DD}3$	— — —	LCD drive power supply 	• Ag specifications • Li specifications • EXT-V specifications	
42 43	CUP1 CUP2	— —	Connections of the LCD power supply step-up (step-down) capacitors		
26 27	CFIN CFOUT	Input Output	System clock oscillator connections • Ceramic element connections (CF specifications) • RC component connections (RC specifications) *: This oscillator circuit is stopped when a STOP or SLOW instruction is executed.	• CF specifications • RC specifications • Unused	
23 22	XTIN XTOUT	Input Output	Used for reference counting (clock specifications, LCD alternation frequency) and as the system clock. • 32-kHz crystal oscillator • 65-kHz crystal oscillator *: This oscillator circuit is stopped when a STOP instruction is executed.	• 32-kHz specifications • 65-kHz specifications • 38-kHz specifications • Unused	
—	XC	—	Used for the phase compensation capacitor connected between this pin and XTOUT and XTIN. This pin is only used in the chip product.		
67 68 69 70	S1 S2 S3 S4	Input	Input-only port • Input pins used to acquire input data to RAM • 1.95-ms and 7.8-ms chattering exclusion circuits included. • Pull-down resistors are built in. Note: the 1.95 ms and 7.8 ms values are for a ø0 of 32.768 kHz.	• Presence or absence of low-level hold transistors	• Pull-down resistors enabled Note: After a reset is cleared, these pins go to the floating state.
71 72 73 74	K1 K2 K3 K4	Input	Input-only port • Input pins used to acquire input data to RAM • 1.95-ms and 7.8-ms chattering exclusion circuits included. • Pull-down resistors are built in. Note: the 1.95 ms and 7.8 ms values are for a ø0 of 32.768 kHz.	• Presence or absence of low-level hold transistors	• Pull-down resistors enabled Note: After a reset is cleared, these pins go to the floating state.
36 37 38 39	M1 M2 M3 M4	I/O	I/O port • Input pins used to acquire input data to RAM. • Output pins used to output RAM data. • M4 is also used as the TM1 external clock input in TM1 mode 3. • M3 is also used for HEF8 halt mode clear control. *: The minimum period for clock signal inputs is twice the cycle time • Pull-down resistors are built in.	• Presence or absence of low-level hold transistors • Output type: CMOS or p-channel	• Pull-down resistors enabled Note: After a reset is cleared, these pins go to the floating state. • Input mode • The output latch data is set to 1.
26 27 79 80	P1 P2 P3 P4	I/O	I/O port • Input pins used to acquire input data to RAM. • Output pins used to output RAM data. • Pull-down resistors are built in.	The same as those for M1 to M4. However, only for valid ports.	The same as those for M1 to M4. However, only for valid ports.
76 77 78 79	A1 A2 A3 A4	I/O	I/O port • Input pins used to acquire input data to RAM. • Output pins used to output RAM data. • Pull-down resistors are built in. • A1 is also used as the external interrupt request control input signal (INT).	The same as those for M1 to M4.	The same as those for M1 to M4.

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<table>
<tr><th>Pin No.</th><th>Pin</th><th>I/O</th><th>Function</th><th>Options</th><th>Status at reset</th></tr>
<tr><td>32
33
34
35</td><td>SO1
SO2
SO3
SO4</td><td>I/O</td><td>I/O port
• Input pins used to acquire input data to RAM.
• Output pins used to output RAM data.
• Pull-down resistors are built in.
SO1 to SO3 are also used as the serial interface pins.
• The serial interface function can be selected under program control.
• Pin functions:
SO1: Serial input
SO2: Serial output
SO3: Serial clock
The serial clock can be taken from either internal or external sources, and can be set up to detect either rising or falling edges under program control.</td><td>Identical to M1 through M4</td><td>Identical to M1 through M4</td></tr>
<tr><td>31</td><td>ALM</td><td>Output</td><td>Output-only pin
• A signal modulated by ø0, ø3, or ø4 can be output under program control.</td><td></td><td>Low-level output</td></tr>
<tr><td>40</td><td>RES</td><td>Input</td><td>IC internal reset input
• The program counter is set to point to location 00H.
• The reset input level can be set to be either high or low.
• Either a pull-up or a pull-down resistor is built in.
Note: Applications must apply the reset signal level for at least 500 µs to effect a reset.</td><td>• Selection of a pull-up or pull-down resistor
• Selection of active-low or active-high reset logic</td><td></td></tr>
<tr><td>44

64

1

21</td><td>Seg 22

Seg 21

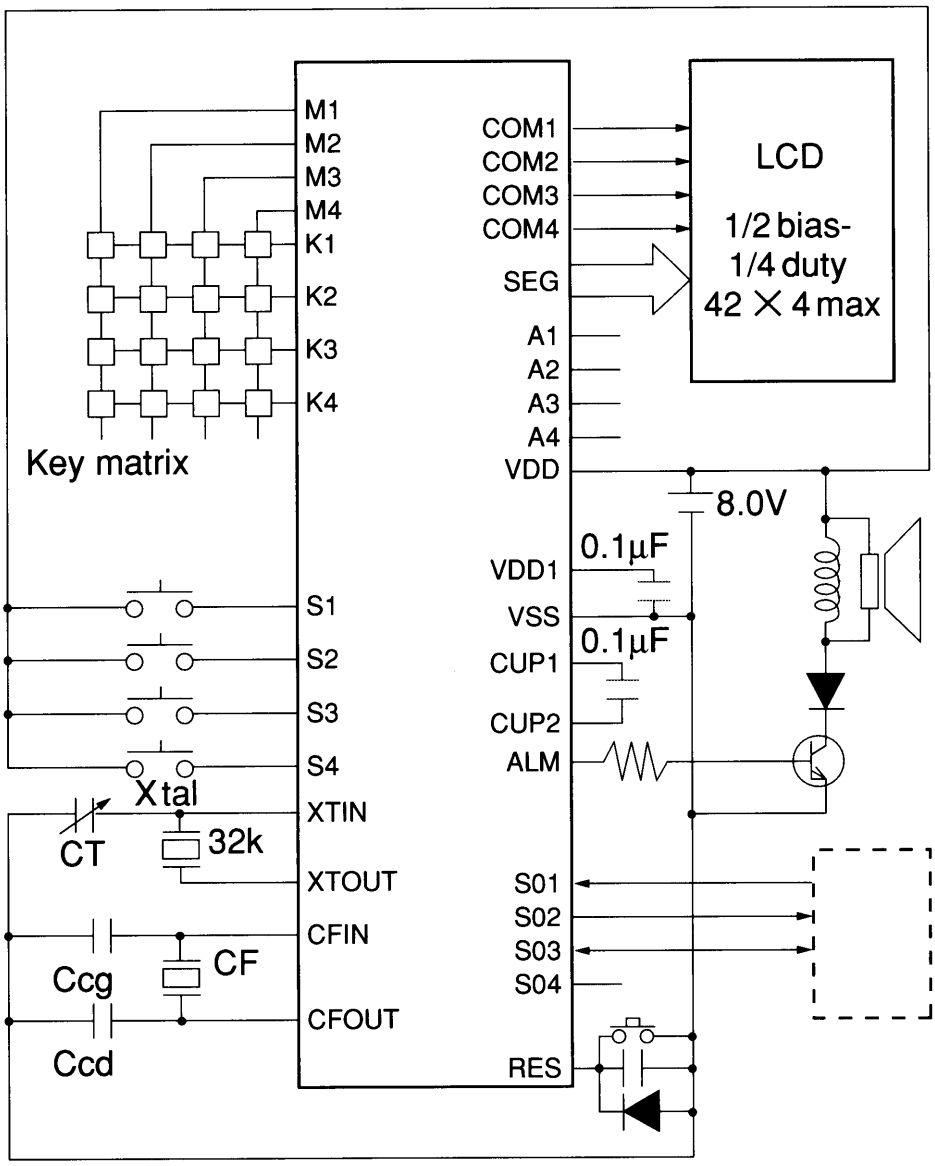
Seg 22

Seg 42</td><td>Output</td><td>LCD panel drive outputs/general-purpose outputs
• LCD panel drive
(1) Static
(2) 1/2 bias 1/2 duty
(3) 1/2 bias 1/3 duty
(4) 1/2 bias 1/4 duty
(5) 1/3 bias 1/3 duty
(6) 1/3 bias 1/4 duty
One of items (1) through (5) is selected as a mask option.

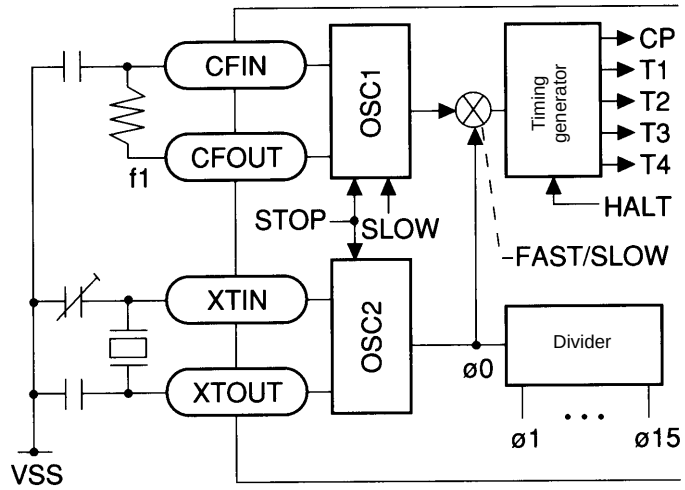
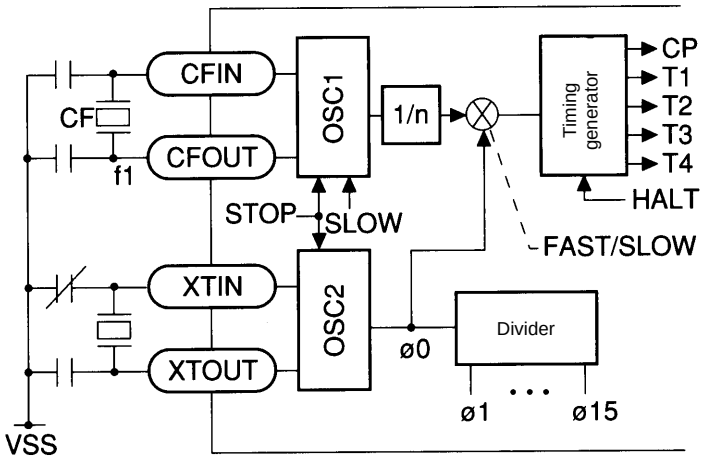
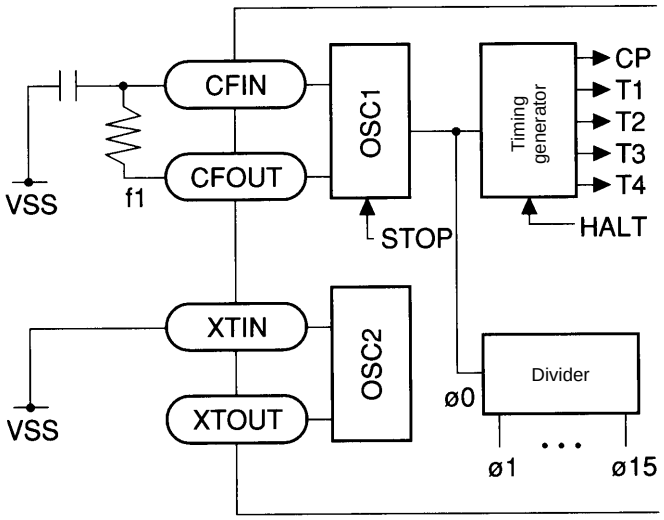
• General-purpose output ports
(1) CMOS output
(2) p-channel open-drain output
(3) n-channel open-drain output
One of items (1) through (3) is selected as a mask option.

• The adoption of the segment PLA in these microcontrollers means that there is no need for programs to control the LCD/general-purpose output states of these pins.
• Output latch control is supported in the oscillator stopped standby states and during a reset.
• Any combination of LCD and general-purpose output functions may be used.</td><td>• Switching between LCD drive output and general-purpose output
• Switching between the LCD drive type options
—Static
—1/2 bias 1/2 duty
—1/2 bias 1/3 duty
—1/2 bias 1/4 duty
—1/3 bias 1/3 duty
—1/3 bias 1/4 duty
• General-purpose output type switching
—CMOS
—p-channel open-drain
—n-channel open-drain
• Standby mode output latch control</td><td>• When used for LCD drive:
—All lit
—All off
*Determined by the master options
• When used as general-purpose outputs:
—High level
—Low level
*Determined by the master options
Note: When a combination of LCD drive and general-purpose outputs is selected, these pins will be either:
All lit/high-level output, or
All off/low-level output.
• During the reset period, the LCD drive functions as static drive.</td></tr>
<tr><td>65
66
79
80</td><td>COM1
COM2
COM3
COM4</td><td>Output</td><td>Common drive outputs for the LCD panel
The table below lists which pins are used in each of the drive types.
However, note that the listed alternation frequencies are the typical specifications when ø0 is 32.768 kHz.
<table><tr><th></th><th>Static</th><th>1/2 duty</th><th>1/3 duty</th><th>1/4/duty</th></tr><tr><td>COM1</td><td>○</td><td>○</td><td>○</td><td>○</td></tr><tr><td>COM2</td><td>×</td><td>○</td><td>○</td><td>○</td></tr><tr><td>COM3</td><td>×</td><td>×</td><td>○</td><td>○</td></tr><tr><td>COM4</td><td>×</td><td>×</td><td>×</td><td>○</td></tr><tr><td>Alternation frequency</td><td>32 Hz</td><td>32 Hz</td><td>42.7 Hz</td><td>64 Hz</td></tr></table>Note: Note that the “×” symbol indicates that the corresponding common pin cannot be used in that drive type.</td><td></td><td>*In products with the CF specifications, the alternation frequency signal stops briefly.</td></tr>
<tr><td>41</td><td>TST</td><td>Input</td><td>Test input
• In the QIP-80 version, this pin must be connected to V_{SS}.
• In the chip version, this pin must be left open or connected to V_{SS}.</td><td></td><td></td></tr>
<tr><td>—
—</td><td>TEST
TEST</td><td>—
—</td><td>Test pins.
(These are not used in the device user interface.)</td><td></td><td></td></tr>
</table>

Sample Application Circuit
LCD : 1/2 bias — 1/4 duty



Oscillator Circuit Options

Option	Circuit type	Notes
RC & Xtal		• The cycle time is 4 times the f1 period. • The divider circuit outputs (ø1 through ø15) are used as the clock time base, the LCD drive waveform generation clock, and for S/K port chattering prevention. • OSC1 is stopped by the execution of a SLOW instruction.
CF & Xtal • 400 kHz (CF) • 4 MHz (CF)		• The cycle time is 4 times n times the f1 period. (n:1) • The divider circuit outputs (ø1 through ø15) are used as the clock time base, the LCD drive waveform generation clock, and for S/K port chattering prevention. • OSC1 is stopped by the execution of a SLOW instruction.
RC		• The cycle time is 4 times the f1 period. • The divider circuit outputs (ø1 through ø15) are used as the clock time base, the LCD drive waveform generation clock, and for S/K port chattering prevention.

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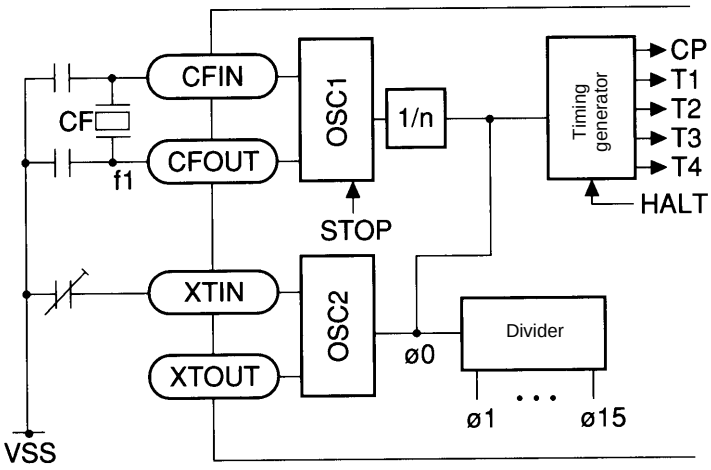
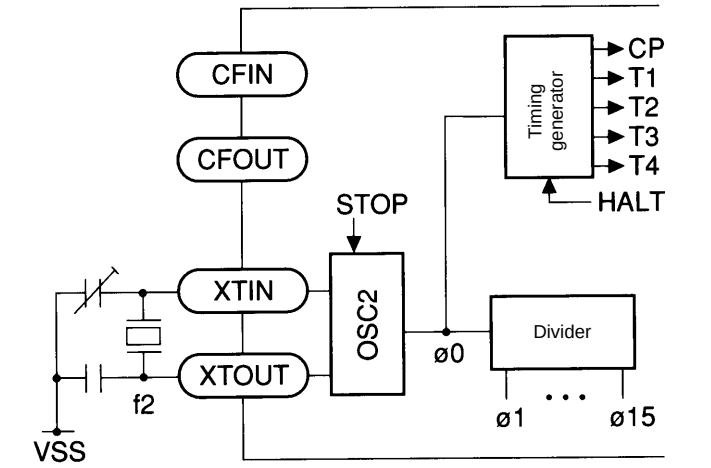
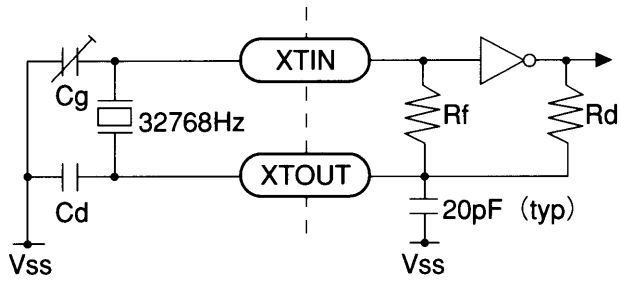
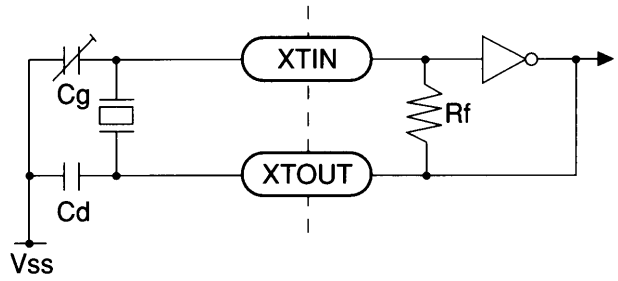
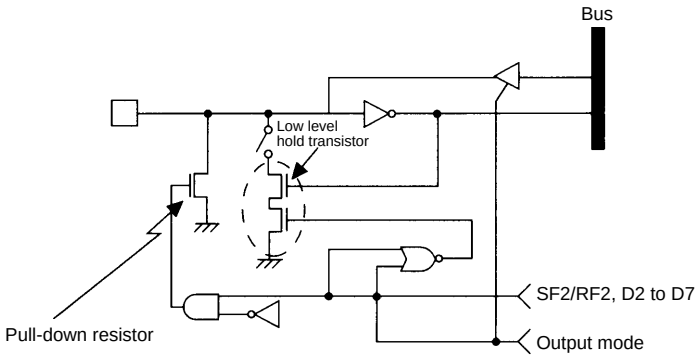
Option	Circuit type	Notes
CF • 400 kHz • 4 MHz		• The cycle time is 4 times n times the f1 period. (n:1) • The divider circuit outputs (ø1 through ø15) are used as the clock time base, the LCD drive frequency generation clock, and for S/K port chattering prevention.
Xtal • 32 kHz • 55 kHz		• The cycle time is 4 times the f2 period. • The divider circuit outputs (ø1 through ø15) are used as the clock time base, the LCD drive waveform generation clock, and for S/K port chattering prevention. Note that the CFIN and CFOUT pins are switched over to function as the P1 and P2 pins.

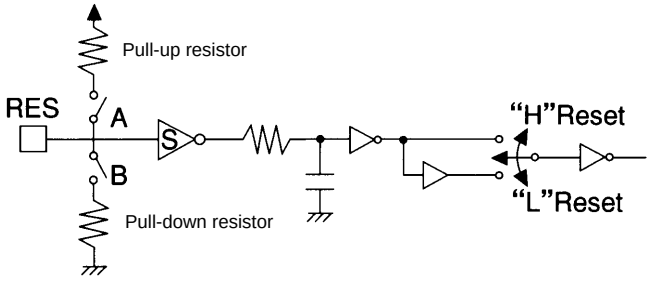
Crystal Oscillator Circuit Options

Option	Circuit type	Notes
Used at 32 kHz		The resistor RD is built into the IC when this circuit is used at 32 kHz.
Used at 38 kHz Used at 65 kHz		• The cycle time is 4 times n times the f1 period. (n:2) • The divider circuit outputs (ø1 through ø15) are used as the clock time base, the LCD drive frequency generation clock, and for S/K port chattering prevention. • OSC1 is stopped by the execution of a SLOW instruction.

Input Port Options

Option	Circuit type	Notes
Low level hold transistor selection		When use of the hold transistor is selected, it is used to minimize the current drain that flows in the pull-down resistor when a push-button switch is used with S1 or a slide switch is used with S2. • When the input open specifications are selected, before reading the input, the pull-down transistor is turned on. Then the input state is read and the pull-down transistor is turned off. If the input was in the floating state, the low level hold transistor operates to hold the level. If use of the hold transistor is not selected: • The circuit is used with the pull-down transistor turned on. • Select unused if the external control signal line connected to this input will never be in the floating state.

RES Pin

Option	Circuit type	Notes
Pull-up resistor, pull-down resistor, resistors left open, and level selections		Internal resistor and polarity selections • Reset on low, pull-up resistor included • Reset on high, pull-down resistor included • Reset on low, no resistors connected • Reset on high, no resistors connected

Mask Option List

Voltage specifications
- Ag specifications
- Li specifications
- EXT-V specifications

LCD driver
- Static
- 1/2 bias — 1/2 duty
  - 1/2 bias — 1/3 duty
  - 1/2 bias — 1/4 duty
  - 1/3 bias — 1/3 duty
  - 1/3 bias — 1/4 duty
  - Unused

Segment port states during a reset
  LCD driver pins
  - All lit
  - All off

  CMOS p/n-channel pins
  - High level
  - Low level

Oscillator specifications
- CF only (ceramic oscillator element)
- RC only (using a resistor and a capacitor)
- Crystal only
- CF + crystal
- RC + crystal

CF
- 400 kHz
- 800 kHz
- 1 MHz
- 2 MHz
- 4 MHz

RC
- 400 kHz
- 800 kHz
- 1 MHz

Crystal
- 32 kHz
- 65 kHz
- 38 kHz

LCD alternation frequency
- SLOW
- TYP
- FAST

External reset circuit
- RES pin
- RES pin + S1 to S4 pressed at the same time

Internal reset circuit (power on reset)
- Selected
- Disabled

RES pin
- Reset on low, pull-up resistor included
- Reset on high, pull-down resistor included
- Reset on low, no resistors connected
- Reset on high, no resistors connected

Alarm output initial level
- Low level
- High level

Chronometer and strobe selection
- 00H
- 10H
- 00H & 10H
- Unused

Port S low level hold transistors
- Low level hold transistors present
- Low level hold transistors disabled

Port K low level hold transistors
- Low level hold transistors present
- Low level hold transistors disabled

Port M low level hold transistors
- Low level hold transistors present
- Low level hold transistors disabled

Port P low level hold transistors
- Low level hold transistors present
- Low level hold transistors disabled

Port SO low level hold transistors
- Low level hold transistors present
- Low level hold transistors disabled

Port A low level hold transistors
- Low level hold transistors present
- Low level hold transistors disabled

M1 to M4 outputs
- CMOS
- p-channel
- n-channel

P1 to P4 outputs
- CMOS
- p-channel
- n-channel

A1 to A4 outputs
- CMOS
- p-channel
- n-channel

These electrical characteristics are provisional and the values are subject to change.

Ag Specifications

Absolute Maximum Ratings at Ta = 25°C ±2°C, V_{SS} = 0 V

Parameter	Symbol	Conditions and applicable pins	Ratings			Unit
			min	typ	max	
Maximum supply voltage	V_{DD}		–0.3		+4.0	V
	$V_{DD}1$		–0.3		+4.0	V
	$V_{DD}2$		–0.3		+5.5	V
	$V_{DD}3$	For 1/3-bias LCD drive techniques	–0.3		+4.0	V
	$V_{DD}3$	For LCD drive techniques other than 1/3 bias	–0.3		+4.0	V
Maximum input voltage	$V_{IN}1$	S1 to S4, K1 to K4, M1 to M4, A1 to A4, SO1 to SO4, RES,TST	–0.3		V_{DD} + 0.3	V
Maximum output voltage	$V_{OUT}1$	M1 to M4, A1 to A4, SO1 to SO4, ALM, CUP2 (With M1 to M4, A1 to A4, and SO1 to SO4 in input mode)	–0.3		+0.3	V
	$V_{OUT}2$	SEGOUT, COM1 to COM4, CUP1	–0.3		$V_{DD}3$ + 0.3	V
Operating temperature	Topg		–20		+65	°C
Storage temperature	Tstg		–30		+125	°C

Allowable Operating Ranges at Ta = 25°C ±2°C, V_{SS} = 0 V

Parameter	Symbol	Conditions and applicable pins	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD} $V_{DD}1$	VBAK = $V_{DD}1$	1.3		1.65	V
	$V_{DD}2$		2.4		3.3	V
	$V_{DD}3$	For 1/3-bias LCD drive techniques	3.7		4.95	V
	$V_{DD}3$	For LCD drive techniques other than 1/3 bias	2.4		3.3	
High-level input voltage	V_{IH}	S1 to S4, K1 to K4, M1 to M4, A1 to A4, SO1 to SO4, (With M1 to M4, A1 to A4, and SO1 to SO4 in input mode) RES	V_{DD} – 0.2		V_{DD}	V
Low-level input voltage	V_{IL}	S1 to S4, K1 to K4, M1 to M4, A1 to A4, SO1 to SO4, (With M1 to M4, A1 to A4, and SO1 to SO4 in input mode) RES	0		0.2	V
Operating frequency	fopg	Ta = –20 to +65°C	32		33	kHz

Electrical Characteristics at Ta = 25°C ±2°C, V_{SS} = 0 V, V_{DD} = $V_{DD}1$

Parameter	Symbol	Conditions and applicable pins	Ratings			Unit
			min	typ	max	
Input resistance	$R_{IN}1A$	V_{DD} = 1.5 V, Low level hold transistor V_{IN} = 0.35 V_{DD} *1 Figure 1	50		500	kΩ
	$R_{IN}1B$	V_{DD} = 1.5 V, Programmable pull-down resistor V_{IN} = 0.7 V_{DD} *1 Figure 1	50		1000	kΩ
	$R_{IN}2A$	V_{DD} = 1.5 V, Low level hold transistor V_{IN} = 0.35 V_{DD}, Input mode *2, Figure 1	50		500	kΩ
	$R_{IN}2B$	V_{DD} = 1.5 V, Programmable pull-down resistor V_{IN} = 0.7 V_{DD}, Input mode *2, Figure 1	50		1000	kΩ
	$R_{IN}3$	V_{DD} = 1.5 V, The RES pin pull-up/pull-down resistor V_{IN} = 0.7 V_{DD}/0.3 V_{DD}	10		300	kΩ
High-level output voltage	$V_{OH}1$	V_{DD} = 1.3 V, I_{OH} = –250 µA, ALM	V_{DD} – 0.65			V
Low-level output voltage	$V_{OL}1$	V_{DD} = 1.3 V, I_{OL} = 250 µA, ALM			0.65	V
High-level output voltage	$V_{OH}2$	V_{DD} = 1.5 V, M1 to 4, A1 to 4, SO1 to 4 I_{OH} = –20 µA, (With M1 to M4, A1 to A4, and SO1 to SO4 in output mode)	V_{DD} – 0.2			V
Low-level output voltage	$V_{OL}2$	V_{DD} = 1.5 V, M1 to 4, A1 to 4, SO1 to 4 I_{OL} = 20 µA, (With M1 to M4, A1 to A4, and SO1 to SO4 in output mode)			0.2	V

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Parameter	Symbol	Conditions and applicable pins	Ratings			Unit
			min	typ	max	
Segment driver output impedance						
[When Set Up as CMOS Output Ports]						
High-level output voltage	$V_{OH}3$	V_{DD} = 1.5 V, I_{OH} = –3 µA, Segment 1 to 42	V_{DD} – 1.0			V
Low-level output voltage	$V_{OL}3$	V_{DD} = 1.5 V, I_{OL} = 3 µA, Segment 1 to 42			1.0	V
[When Set Up as P-Channel Open-Drain Output Ports]						
High-level output voltage	$V_{OH}3$	V_{DD} = 1.5 V, I_{OH} = –3 µA, Segment 1 to 42		0.3	1.0	V
Output off leakage current	I_{OFF}	V_{DD} = 1.5 V, V_{OL} = V_{SS}, Segment 1 to 42			1.0	µA
[Static Drive]						
High-level output voltage	$V_{OH}3$	V_{DD} = 1.5 V, I_{OH} = –0.4 µA, SEGOUT	$V_{DD}2$ – 0.2			V
Low-level output voltage	$V_{OL}3$	V_{DD} = 1.5 V, I_{OL} = 0.4 µA, SEGOUT			0.2	V
High-level output voltage	$V_{OH}4$	V_{DD} = 1.5 V, I_{OH} = –4 µA, COM1	$V_{DD}2$ – 0.2			V
Low-level output voltage	$V_{OL}4$	V_{DD} = 1.5 V, I_{OL} = 4 µA, COM1			0.2	V
[Duplex Drive (1/2 bias - 1/2 duty)]						
High-level output voltage	$V_{OH}3$	V_{DD} = 1.5 V, I_{OH} = –0.4 µA, SEGOUT	$V_{DD}2$ – 0.2			V
Low-level output voltage	$V_{OL}3$	V_{DD} = 1.5 V, I_{OL} = 0.4 µA, SEGOUT			0.2	V
High-level output voltage	$V_{OH}4$	V_{DD} = 1.5 V, I_{OH} = –4 µA, COM1 to COM2	$V_{DD}2$ – 0.2			V
Middle-level output voltage	V_{OM}	V_{DD} = 1.5 V, I_{OH} = –4 µA, I_{OL} = 4 µA, COM1 to COM2	$V_{DD}1$ – 0.2		$V_{DD}1$ + 0.2	V
Low-level output voltage	$V_{OL}4$	V_{DD} = 1.5 V, I_{OL} = 4 µA, COM1 to COM2			0.2	V
[1/2 Bias - 1/3 Duty and 1/2 Bias - 1/4 Duty Drive]						
High-level output voltage	$V_{OH}3$	V_{DD} = 1.5 V, I_{OH} = –0.4 µA, SEGOUT	$V_{DD}2$ – 0.2			V
Low-level output voltage	$V_{OL}3$	V_{DD} = 1.5 V, I_{OL} = 0.4 µA, SEGOUT			0.2	V
High-level output voltage	$V_{OH}4$	V_{DD} = 1.5 V, I_{OH} = –4 µA, COM1 to COM3 (1/3 duty) COM1 to COM4 (1/4 duty)	$V_{DD}2$ – 0.2			V
Middle-level output voltage	V_{OM}	V_{DD} = 1.5 V, I_{OH} = –4 µA, I_{OL} = 4 µA, COM1 to COM3 (1/3 duty), COM1 to COM4 (1/4 duty)	$V_{DD}1$ – 0.2		$V_{DD}1$ + 0.2	V
Low-level output voltage	$V_{OL}4$	V_{DD} = 1.5 V, I_{OL} = 4 µA, COM1 to 2 COM1 to COM3 (1/3 duty), COM1 to COM4 (1/4 duty)			0.2	V
[1/3 Bias - 1/3 Duty and 1/3 Bias - 1/4 Duty Drive]						
High-level output voltage	$V_{OH}3$	V_{DD} = 1.5 V, I_{OH} = –0.4 µA, SEGOUT	$V_{DD}3$ – 0.2			V
M1-level output voltage	$V_{OM}1$–3	V_{DD} = 1.5 V, I_{OH} = –0.4 µA, I_{OL} = 0.4 µA, SEGOUT	$V_{DD}2$ – 0.2		$V_{DD}2$ + 0.2	V
M2-level output voltage	$V_{OM}2$–3	V_{DD} = 1.5 V, I_{OH} = –0.4 µA, I_{OL} = 0.4 µA, SEGOUT	$V_{DD}1$ – 0.2		$V_{DD}1$ + 0.2	V
Low-level output voltage	$V_{OL}3$	V_{DD} = 1.5 V, I_{OL} = 0.4 µA, SEGOUT			0.2	V
High-level output voltage	$V_{OH}4$	V_{DD} = 1.5 V, I_{OH} = –4 µA, COM1 to COM3 (1/3 duty) COM1 to COM4 (1/4 duty)	$V_{DD}3$ – 0.2			V
M1-level output voltage	$V_{OM}1$–4	V_{DD} = 1.5 V, I_{OH} = –4 µA, I_{OL} = 4 µA, COM1 to COM3 (1/3 duty), COM1 to COM4 (1/4 duty)	$V_{DD}2$ – 0.2		$V_{DD}2$ + 0.2	V
M2-level output voltage	$V_{OM}2$–4	V_{DD} = 1.5 V, I_{OH} = –4 µA, I_{OL} = 4 µA, COM1 to COM3 (1/3 duty), COM1 to COM4 (1/4 duty)	$V_{DD}1$ – 0.2		$V_{DD}1$ + 0.2	V
Low-level output voltage	$V_{OL}4$	V_{DD} = 1.5 V, I_{OL} = 4 µA, COM1 to COM3 (1/3 duty), COM1 to COM4 (1/4 duty)			0.2	V

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Parameter	Symbol	Conditions and applicable pins	Ratings			Unit
			min	typ	max	
[Output Voltage]						
LCD drive method: 1/3 bias						
(doubler)	$V_{DD}2$	V_{DD} = 1.35 V, fopg = 32.768 kHz, C1 to C3 = 0.1 µF Figure 2	2.5			V
(tripler)	$V_{DD}3$	V_{DD} = 1.35 V, fopg = 32.768 kHz, C1 to C3 = 0.1 µF Figure 2	3.75			V
LCD drive method: 1/2 bias						
(doubler)	$V_{DD}2$	V_{DD} = 1.35 V, fopg = 32.768 kHz, C1 to C2 = 0.1 µF Figure 3	2.5			V
[Current Drain (with the backup flag cleared)]						
LCD drive method: 1/3 bias	$\lvert I_{DD} \rvert$	V_{DD} = 1.5 V, In halt mode, C1 to C3 = 0.1 µF, CI = 25 kΩ, Figure 2, Co = Cg = 20 pF, 32.768 kHz Xtal		3.5		µA
LCD drive methods other than 1/3 bias	$\lvert I_{DD} \rvert$	V_{DD} = 1.5 V, In halt mode, C1 = C2 = 0.1 µF, CI = 25 kΩ, Figure 3, Co = Cg = 20 pF, 32.768 kHz Xtal		2.0		µA
Oscillator start voltage	| Vstt |	Co = Cg = 20 pF, CI = 25 kΩ, Figure 3, 32.768 kHz Xtal			1.35	V
Oscillator hold voltage	$\lvert V_{HOLD} \rvert$	$V_{BAK} = V_{DD}1$, CI = 25 kΩ, Figures 2 and 3 Co = Cg = 20 pF, 32.768 kHz Xtal	1.3		1.65	V
Oscillator start time	Tstt	V_{DD} = 1.35 V, CI = 25 kΩ, Figure 4, Co = Cg = 20 pF, 32.768 kHz Xtal			10	sec
Oscillator correction capacitance	10P	XC	8	10	12	pF
	20P	XTOUT	16	20	24	pF

Li Specifications

Absolute Maximum Ratings at Ta = 25°C ±2°C, V_{SS} = 0 V

Parameter	Symbol	Conditions and applicable pins	Ratings			Unit
			min	typ	max	
Maximum supply voltage	V_{DD}		–0.3		+4.0	V
	$V_{DD}1$	V_{BAK} = $V_{DD}1$ or $V_{DD}2$	–0.3		+4.0	V
	$V_{DD}2$		–0.3		+4.0	V
	$V_{DD}3$	(LCD drive method: 1/3 bias)	–0.3		+5.5	V
	$V_{DD}3$	(LCD drive methods other than 1/3 bias)	–0.3		+4.0	V
Maximum input voltage	$V_{IN}1$	S1 to S4, K1 to K4, M1 to M4, A1 to A4, SO1 to SO4, (With M1 to M4, A1 to A4, and SO1 to SO4 in input mode) RES, TST	–0.3		V_{DD} + 0.3	V
Maximum output voltage (LCD drive method: 1/3 bias)	$V_{OUT}1$	M1 to M4, A1 to A4, SO1 to SO4, (With M1 to M4, A1 to A4, and SO1 to SO4 in output mode) ALM, CUP2	–0.3		V_{DD} + 0.3	V
	$V_{OUT}2$	SEGOUT, COM1 to COM4, CUP1	–0.3		$V_{DD}3$ + 0.3	V
(LCD drive methods other than 1/3 bias)	$V_{OUT}2$	M1 to M4, A1 to A4, SO1 to SO4, (With M1 to M4, A1 to A4, and SO1 to SO4 in output mode) ALM, SEGOUT, COM1 to COM4, CUP1, CUP2	–0.3		V_{DD} + 0.3	V
Operating temperature	Topg		–20		+65	°C
Storage temperature	Tstg		–30		+125	°C

Allowable Operating Ranges at Ta = 25°C ±2°C, V_{SS} = 0 V

Parameter	Symbol	Conditions and applicable pins	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD} / $V_{DD}2$	V_{BAK} = V_{DD} /2 (With the backup flag cleared)	2.0		3.6	V
	V_{DD} / $V_{DD}2$	V_{BAK} = V_{DD} (With the backup flag uncleared)	1.3		3.6	V
	$V_{DD}3$	(LCD drive method: 1/3-bias)	3.9		5.0	V
	$V_{DD}3$	(LCD drive methods other than 1/3 bias)		$V_{DD}3 = V_{DD}2$		V
High-level input voltage	V_{IH}	S1 to S4, K1 to K4, M1 to M4, A1 to A4, SO1 to SO4, (With M1 to M4, A1 to A4, and SO1 to SO4 in input mode) RES	V_{DD} – 0.4		V_{DD}	V
Low-level input voltage	V_{IL}	S1 to S4, K1 to K4, M1 to M4, A1 to A4, SO1 to SO4, (With M1 to M4, A1 to A4, and SO1 to SO4 in input mode) RES	0		0.4	V
Operating frequency	fopg	Ta = –20 to +65°C	32		33	kHz

Electrical Characteristics at Ta = 25°C ±2°C, V_{SS} = 0 V, V_{DD} = $V_{DD}2$

Parameter	Symbol	Conditions and applicable pins	Ratings			Unit
			min	typ	max	
Input resistance	$R_{IN}1A$	V_{DD} = 3.0 V, V_{IN} = 0.35 V_{DD} Low level hold transistor *1, Figure 5	50		500	kΩ
	$R_{IN}1B$	V_{DD} = 3.0 V, V_{IN} = 0.7V_{DD} Programmable pull-down resistor *1, Figure 5	50		1000	kΩ
	$R_{IN}2A$	V_{DD} = 3.0 V, input mode, Low level hold transistor *1, V_{IN} = 0.35 V_{DD}, Figure 5	50		500	kΩ
	$R_{IN}2B$	V_{DD} = 3.0 V, Programmable pull-down resistor, *2, V_{IN} = 0.7 V_{DD}, input mode, Figure 5	50		1000	kΩ
	$R_{IN}3$	V_{DD} = 3.0 V, RES pin pull-up/pull-down resistor V_{IN} = 0.7 V_{DD}/0.3 V_{DD}	10		300	kΩ

Electrical Characteristics at Ta = 25°C ±2°C, V_{SS} = 0 V, V_{DD} = V_{DD}2

Parameter	Symbol	Conditions and applicable pins	Ratings			Unit
			min	typ	max	
High-level output voltage	$V_{OH}1$	V_{DD} = 2.5 V, I_{OH} = –250 µA, ALM	V_{DD} – 0.65			V
Low-level output voltage	$V_{OL}1$	V_{DD} = 2.5 V, I_{OL} = 250 µA, ALM			0.65	V
High-level output voltage	$V_{OH}2$	V_{DD} = 3.0 V, I_{OH} = –40 µA, M1 to M4, A1 to A4, SO1 to SO4, (With M1 to M4, A1 to A4, and SO1 to SO4 in output mode)	V_{DD} – 0.4			V
Low-level output voltage	$V_{OL}2$	V_{DD} = 3.0 V, I_{OL} = 40 µA, M1 to M4, A1 to A4, SO1 to SO4, (With M1 to M4, A1 to A4, and SO1 to SO4 in output mode)			0.4	V
Segment driver output impedance						
[When Set Up as CMOS Output Ports]						
High-level output voltage	$V_{OH}3$	V_{DD} = 3.0 V, I_{OH} = –5 µA, Segment 1 to 42	V_{DD} – 1			V
Low-level output voltage	$V_{OL}3$	V_{DD} = 3.0 V, I_{OL} = 5 µA, Segment 1 to 42			1	V
[When Set Up as P-Channel Open-Drain Output Ports]						
High-level output voltage	$V_{OH}3$	V_{DD} = 2.5 V, I_{OH} = –10 µA, Segment 1 to 42		0.3	1	V
Output off leakage current	I_{OFF}	V_{DD} = 3.0 V, V_{OL} = V_{SS}			1	µA
[Static Drive]						
High-level output voltage	$V_{OH}3$	V_{DD} = 3.0 V, I_{OH} = –0.4 µA, SEGOUT	V_{DD} – 0.2			V
Low-level output voltage	$V_{OL}3$	V_{DD} = 3.0 V, I_{OL} = 0.4 µA, SEGOUT			0.2	V
High-level output voltage	$V_{OH}4$	V_{DD} = 3.0 V, I_{OH} = –4 µA, COM1	V_{DD} – 0.2			V
Low-level output voltage	$V_{OL}4$	V_{DD} = 3.0 V, I_{OL} = 4 µA, COM1			0.2	V
[Duplex Drive (1/2 bias - 1/2 duty)]						
High-level output voltage	$V_{OH}3$	V_{DD} = 3.0 V, I_{OH} = –0.4 µA, SEGOUT	V_{DD} – 0.2			V
Low-level output voltage	$V_{OL}3$	V_{DD} = 3.0 V, I_{OL} = 0.4 µA, SEGOUT			0.2	V
High-level output voltage	$V_{OH}4$	V_{DD} = 3.0 V, I_{OH} = –4 µA, COM1 to COM2	V_{DD} – 0.2			V
Middle-level output voltage	V_{OM}	V_{DD} = 3.0 V, I_{OH} = –4 µA, I_{OL} = 4 µA, COM1 to COM2	$V_{DD}1$ – 0.2		$V_{DD}1$ + 0.2	V
Low-level output voltage	$V_{OL}4$	V_{DD} = 3.0 V, I_{OL} = 4 µA, COM1 to COM2			0.2	V
[1/2 Bias - 1/3 Duty and 1/2 Bias - 1/4 Duty Drive]						
High-level output voltage	$V_{OH}3$	V_{DD} = 3.0 V, I_{OH} = –0.4 µA, SEGOUT	V_{DD} – 0.2			V
Low-level output voltage	$V_{OL}3$	V_{DD} = 3.0 V, I_{OL} = 0.4 µA, SEGOUT			0.2	V
High-level output voltage	$V_{OH}4$	V_{DD} = 3.0 V, I_{OH} = –4 µA, COM1 to COM3 (1/3 duty) COM1 to COM4 (1/4 duty)	V_{DD} – 0.2			V
Middle-level output voltage	V_{OM}	V_{DD} = 3.0 V, I_{OH} = –4 µA, I_{OL} = 4 µA, COM1 to COM3 (1/3 duty) COM1 to COM4 (1/4 duty)	$V_{DD}1$ – 0.2		$V_{DD}1$ + 0.2	V
Low-level output voltage	$V_{OL}4$	V_{DD} = 3.0 V, I_{OL} = 4 µA, COM1 to COM3 (1/3 duty) COM1 to COM4 (1/4 duty)			0.2	V

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Parameter	Symbol	Conditions and applicable pins	Ratings			Unit
			min	typ	max	
[1/3 Bias - 1/3 Duty and 1/3 Bias - 1/4 Duty Drive]						
High-level output voltage	$V_{OH}3$	V_{DD} = 3.0 V, I_{OH} = –0.4 µA, SEGOUT	$V_{DD}3$ – 0.2			V
M1-level output voltage	$V_{OM}1$–3	V_{DD} = 3.0 V, I_{OH} = –0.4 µA, I_{OL} = 0.4 µA, SEGOUT	$V_{DD}2$ – 0.2		$V_{DD}2$ + 0.2	V
M2-level output voltage	$V_{OM}2$–3	V_{DD} = 3.0 V, I_{OH} = –0.4 µA, I_{OL} = 0.4 µA, SEGOUT	$V_{DD}1$ – 0.2		$V_{DD}1$ + 0.2	V
Low-level output voltage	$V_{OL}3$	V_{DD} = 3.0 V, I_{OL} = 0.4 µA, SEGOUT			0.2	V
High-level output voltage	$V_{OH}4$	V_{DD} = 3.0 V, I_{OH} = –4 µA, COM1 to COM3 (in 1/3 duty mode) COM1 to COM4 (in 1/4 duty mode)	$V_{DD}3$ – 0.2			V
M1-level output voltage	$V_{OH}1$–4	V_{DD} = 3.0 V, I_{OH} = –4 µA, I_{OL} = 4 µA, COM1 to COM3 (in 1/3 duty mode) COM1 to COM4 (in 1/4 duty mode)	$V_{DD}2$ – 0.2		$V_{DD}2$ + 0.2	V
M2-level output voltage	$V_{OM}2$–4	V_{DD} = 3.0 V, I_{OH} = –4 µA, I_{OL} = 4 µA, COM1 to COM3 (in 1/3 duty mode) COM1 to COM4 (in 1/4 duty mode)	$V_{DD}1$ – 0.2		$V_{DD}1$ + 0.2	V
Low-level output voltage	$V_{OL}4$	V_{DD} = 3.0 V, I_{OL} = 4 µA, COM1 to COM3 (in 1/3 duty mode) COM1 to COM4 (in 1/4 duty mode)			0.2	V
[Output Voltage]						
LCD drive method: 1/3 bias						
(halver)	$V_{DD}1$	V_{DD} = 3.0 V, fopg = 32.768 kHz, C1 to C4 = 0.1 µF, Figure 6	1.35			V
(tripler)	$V_{DD}3$	V_{DD} = 3.0 V, fopg = 32.768 kHz, C1 to C4 = 0.1 µF, Figure 6	4.1			V
LCD drive method: 1/2 bias						
(halver)	$V_{DD}1$	V_{DD} = 3.0 V, fopg = 32.768 kHz, C1 = C2 = 0.1 µF, Figure 7	1.35			V
[Current Drain (With the backup flag cleared)]						
LCD drive method: 1/3 bias	$\lvert I_{DD} \rvert$	V_{DD} = 3.0 V, Halt mode C1 to C4 = 0.1 µF, C1 = 25 kΩ, Figure 6 Co = Cg = 20 pF, 32.768 kHz Xtal		2.0		µA
LCD drive methods other than 1/3 bias	$\lvert I_{DD} \rvert$	V_{DD} = 3.0 V, Halt mode C1 = C2 = 0.1 µF, CI = 25 kΩ, Figure 7 Co = Cg = 20 pF, 32.768 kHz Xtal		1.0		µA
Oscillator start capacitor	| Vstt |	$V_{DD}1$ = V_{DD}, CI = 25 kΩ, Figure 4 Co = Cg = 20 pF, 32.768 kHz Xtal			1.35	V
Oscillator hold voltage (with the backup flag cleared)	V_{HOLD}	V_{BAK} = $V_{DD}1$ = V_{DD}/2, CI = 25 kΩ, Figures 6 and 7 Co = Cg = 20 pF, 32.768 kHz Xtal	2.6			V
Oscillator start time	Tstt	$V_{DD}1$ = V_{DD} = 1.35 V, CI = 25 kΩ, Figure 4 Co = Cg = 20 pF, 32.768 kHz Xtal			10	sec
Oscillator correction capacitance	10P	XC	8	10	12	pF
	20P	XTOUT	16	20	24	pF

EXT-V Specifications

Absolute Maximum Ratings at Ta = 25°C ±2°C, V_{SS} = 0 V

Parameter	Symbol	Conditions and applicable pins	Ratings			Unit
			min	typ	max	
Maximum supply voltage	V_{DD}		–0.3		+4.0	V
	$V_{DD}1$		–0.3		+4.0	V
	$V_{DD}2$		–0.3		+4.0	V
	$V_{DD}3$	(LCD drive method: 1/3 bias)	–0.3		+5.5	V
	$V_{DD}3$	(LCD drive methods other than 1/3 bias)	–0.3		+4.0	V
Maximum input voltage	$V_{IN}2$	S1 to S4, K1 to K4, M1 to M4, A1 to A4, SO1 to SO4, (With M1 to M4, A1 to A4, and SO1 to SO4 in input mode) RES, TST	–0.3		V_{DD} + 0.3	V
Maximum output voltage (LCD drive method: 1/3 bias)	$V_{OUT}2$	M1 to M4, A1 to A4, SO1 to SO4, (With M1 to M4, A1 to A4, and SO1 to SO4 in output mode) ALM, CUP2	–0.3		V_{DD} + 0.3	V
	$V_{OUT}3$	SEGOUT, COM1 to COM4, CUP1	–0.3		$V_{DD}3$ + 0.3	V
(LCD drive methods other than 1/3 bias)	$V_{OUT}2$	M1 to M4, A1 to A4, SO1 to SO4, (With M1 to M4, A1 to A4, and SO1 to SO4 in output mode) ALM, SEGOUT, COM1 to COM4, CUP1	–0.3		V_{DD} + 0.3	V
Operating temperature	Topg		–20		+65	°C
Storage temperature	Tstg		–30		+125	°C

Allowable Operating Ranges at Ta = 25°C ±2°C, V_{SS} = 0 V

Parameter	Symbol	Conditions and applicable pins	Ratings			Unit
			min	typ	max	
Supply voltage	$V_{DD}1$		1.3		3.6	V
	V_{DD} $V_{DD}2$		2.0		3.6	V
	$V_{DD}3$	(LCD drive method: 1/3-bias)	3.9		5.0	V
	$V_{DD}3$	(LCD drive methods other than 1/3 bias)	$V_{DD}3 = V_{DD}2$			V
High-level input voltage	V_{IH}	S1 to S4, K1 to K4, M1 to M4, A1 to A4, SO1 to SO4, (With M1 to M4, A1 to A4, and SO1 to SO4 in input mode) RES	V_{DD} – 0.4		V_{DD}	V
Low-level input voltage	V_{IL}	S1 to S4, K1 to K4, M1 to M4, A1 to A4, SO1 to SO4, (With M1 to M4, A1 to A4, and SO1 to SO4 in input mode) RES	0		0.4	V
Operating frequency	fopg	Ta = –20 + 65°C	32		33	kHz

Electrical Characteristics at Ta = 25°C ±2°C, V_{SS} = 0 V, V_{DD} = $V_{DD}2$

Parameter	Symbol	Conditions and applicable pins	Ratings			Unit
			min	typ	max	
Input resistance	$R_{IN}1A$	V_{DD} = 3.0 V, V_{IN} = 0.35 V_{DD}, Low level hold transistor *1, Figure 5	50		500	kΩ
	$R_{IN}1B$	V_{DD} = 3.0 V, V_{IN} = 0.7 V_{DD}, Programmable pull-down resistor *1, Figure 5	50		1000	kΩ
	$R_{IN}2A$	V_{DD} = 3.0 V, V_{IN} = 0.35 V_{DD}, Input mode, Low level hold transistor *1, Figure 5	50		500	kΩ
	$R_{IN}2B$	V_{DD} = 3.0 V, V_{IN} = 0.7 V_{DD}, input mode, Programmable pull-down resistor *2, Figure 5	50		1000	kΩ
	$R_{IN}3$	V_{DD} = 3.0 V, V_{IN} = 0.7 V_{DD}/0.3 V_{DD} RES pin pull-up/pull-down resistor	10		300	kΩ

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Parameter	Symbol	Conditions and applicable pins	Ratings			Unit
			min	typ	max	
High-level output voltage	$V_{OH}1$	V_{DD} = 2.5 V, I_{OH} = –250 µA, ALM	V_{DD} – 0.65			V
Low-level output voltage	$V_{OL}1$	V_{DD} = 2.5 V, I_{OL} = 250 µA, ALM			0.65	V
High-level output voltage	$V_{OH}2$	V_{DD} = 3.0 V, I_{OH} = –40 µA, M1 to M4, A1 to A4, SO1 to SO4 (With M1 to M4, A1 to A4, and SO1 to SO4 in output mode)	V_{DD} – 0.4			V
Low-level output voltage	$V_{OL}2$	V_{DD} = 3.0 V, I_{OL} = 40 µA, M1 to M4, A1 to A4, SO1 to SO4 (With M1 to M4, A1 to A4, and SO1 to SO4 in output mode)			0.4	V
Segment driver output impedance						
[When Set Up as CMOS Output Ports]						
High-level output voltage	$V_{OH}3$	V_{DD} = 2.4 V, I_{OH} = –10 µA, Segment 1 to 42	V_{DD} – 1			V
Low-level output voltage	$V_{OL}3$	V_{DD} = 2.4 V, I_{OL} = 40 µA			1	V
High-level output voltage	$V_{OH}4$	V_{DD} = 2.4 V, I_{OH} = –5 µA, Segment 1 to 42	V_{DD} – 1			V
Low-level output voltage	$V_{OL}4$	V_{DD} = 2.4 V, I_{OL} = 20 µA			1	V
[When Set Up as P-Channel Open-Drain Output Ports]						
High-level output voltage	$V_{OH}3$	V_{DD} = 2.4 V, I_{OH} = –10 µA, Segment 1 to 42	V_{DD} – 0.2	0.3	1	V
Output off leakage current	I_{OFF}	V_{DD} = 2.6 V, V_{OL} = V_{SS}			1	µA
[Static Drive]						
High-level output voltage	$V_{OH}5$	V_{DD} = 3.0 V, I_{OH} = –0.4 µA, SEGOUT	V_{DD} – 0.2			V
Low-level output voltage	$V_{OL}5$	V_{DD} = 3.0 V, I_{OL} = 0.4 µA, SEGOUT			0.2	V
High-level output voltage	$V_{OH}6$	V_{DD} = 3.0 V, I_{OH} = –4 µA, COM1	V_{DD} – 0.2			V
Low-level output voltage	$V_{OL}6$	V_{DD} = 3.0 V, I_{OL} = 4 µA, COM1			0.2	V
[Duplex Drive (1/2 bias - 1/2 duty)]						
High-level output voltage	$V_{OH}5$	V_{DD} = 3.0 V, I_{OH} = –0.4 µA, SEGOUT	$V_{DD}2$ – 0.2			V
Low-level output voltage	$V_{OL}5$	V_{DD} = 3.0 V, I_{OL} = 0.4 µA, SEGOUT			0.2	V
High-level output voltage	$V_{OH}6$	V_{DD} = 3.0 V, I_{OH} = –4 µA, COM1 to COM2	$V_{DD}1$ – 0.2			V
Middle-level output voltage	V_{OM}	V_{DD} = 3.0 V I_{OH} = –4 µA, I_{OL} = 4 µA, COM1 to COM2			$V_{DD}1$ + 0.2	V
Low-level output voltage	$V_{OL}6$	V_{DD} = 3.0 V, I_{OL} = 4 µA, COM1 to COM2			0.2	V
[1/2 Bias - 1/3 Duty and 1/2 Bias - 1/4 Duty Drive]						
High-level output voltage	$V_{OH}5$	V_{DD} = 3.0 V, I_{OH} = –0.4 µA, SEGOUT	V_{DD} – 0.2			V
Low-level output voltage	$V_{OL}5$	V_{DD} = 3.0 V, I_{OL} = 0.4 µA, SEGOUT			0.2	V
High-level output voltage	$V_{OH}6$	V_{DD} = 3.0 V, I_{OH} = –4 µA, COM1 to COM3 (1/3 duty) COM1 to COM4 (1/4 duty)	$V_{DD}2$ – 0.2			V
Middle-level output voltage	V_{OM}	V_{DD} = 3.0 V I_{OH} = –4 µA, I_{OL} = 4 µA, COM1 to COM3 (1/3 duty) COM1 to COM4 (1/4 duty)	$V_{DD}1$ – 0.2		$V_{DD}1$ + 0.2	V
Low-level output voltage	$V_{OL}6$	V_{DD} = 3.0 V, I_{OL} = 4 µA, COM1 to COM3 (1/3 duty) COM1 to COM4 (1/4 duty)			0.2	V

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Parameter	Symbol	Conditions and applicable pins	Ratings			Unit
			min	typ	max	
[1/3 Bias - 1/3 Duty and 1/3 Bias - 1/4 Duty Drive]						
High-level output voltage	$V_{OH}5$	V_{DD} = 3.0 V, I_{OH} = –0.4 µA, SEGOUT	$V_{DD}3$ + 0.2			V
Middle-level output voltage	$V_{OM}1$–5	V_{DD} = 3.0 V, I_{OH} = –0.4 µA, I_{OL} = 0.4 µA, SEGOUT	$V_{DD}2$ – 0.2		$V_{DD}2$ + 0.2	V
	$V_{OM}2$–5	V_{DD} = 3.0 V, I_{OH} = –0.4 µA, I_{OL} = 0.4 µA, SEGOUT	$V_{DD}1$ – 0.2		$V_{DD}1$ + 0.2	V
Low-level output voltage	$V_{OL}5$	V_{DD} = 3.0 V, I_{OL} = 0.4 µA, SEGOUT			0.2	V
High-level output voltage	$V_{OH}6$	V_{DD} = 3.0 V, I_{OH} = –0.4 µA, COM1 to COM3 (in 1/3 duty mode) COM1 to COM4 (in 1/4 duty mode)	$V_{DD}3$ + 0.2			V
Middle-level output voltage	$V_{OM}1$–6	V_{DD} = 3.0 V, I_{OH} = –0.4 µA, I_{OL} = 0.4 µA, COM1 to COM3 (in 1/3 duty mode) COM1 to COM4 (in 1/4 duty mode)	$V_{DD}2$ – 0.2		$V_{DD}2$ + 0.2	V
	$V_{OM}2$–6	V_{DD} = 3.0 V, I_{OH} = –0.4 µA, I_{OL} = 0.4 µA, COM1 to COM3 (in 1/3 duty mode) COM1 to COM4 (in 1/4 duty mode)	$V_{DD}1$ – 0.2		$V_{DD}1$ + 0.2	V
Low-level output voltage	$V_{OL}6$	V_{DD} = 3.0 V, I_{OL} = 0.4 µA			0.2	V
[Output Voltage]						
LCD drive method: 1/3 bias						
(halver)	$V_{DD}1$	V_{DD} = 3.0 V, fopg = 32.768 kHz, C1 to C4 = 0.1 µF, Figure 6	1.35			V
(tripler)	$V_{DD}3$	V_{DD} = 3.0 V, fopg = 32.768 kHz, C1 to C4 = 0.1 µF, Figure 6	4.1			V
LCD drive method: 1/2 bias						
(halver)	$V_{DD}1$	V_{DD} = 3.0 V, fopg 32.768 kHz, C1 = C2 = 0.1 µF, Figure 7	1.35			V
[Current Drain (With the backup flag cleared)]						
LCD drive method: 1/3 bias	$\lvert I_{DD} \rvert$	V_{DD} = 3.0 V, Halt mode, C1 to C4 = 0.1 µF, CI = 25 kΩ Co = Cg = 20 pF, 32.768 kHz Xtal, Figure 6		5.0		µA
LCD drive methods other than 1/3 bias	$\lvert I_{DD} \rvert$	V_{DD} = 3.0 V, Halt mode, C1 to C2 = 0.1 µF, CI = 25 kΩ, Figure 7, Co = Cg = 20 pF, 32.768 kHz, Xtal		5.0		µA
Oscillator start voltage	Vstt	V_{DD} = $V_{DD}2$, CI = 25 kΩ, Figure 4, Co = Cg = 20 pF, 32.768 kHz Xtal			2.2	V
Oscillator hold voltage (with the backup flag cleared)	V_{HOLD}	V_{DD} = $V_{DD}2$, CI = 25 kΩ, , Figures 5, 6, 7, and 8, Co = Cg = 20 pF, 32.768 kHz Xtal	2.0			V
Oscillator start time	Tstt	V_{DD} = $V_{DD}2$ = 2.2 V, CI = 25 kΩ, Figure 4 Co = Cg = 20 pF, 32.768 kHz Xtal			10	sec
Oscillator correction capacitance	10P	XC	8	10	12	pF
	20P	XTOUT	16	20	24	pF

Note : 1. S1 to 4, K1 to 4
2. M1 to 4, A1 to 4, SO1 to 4

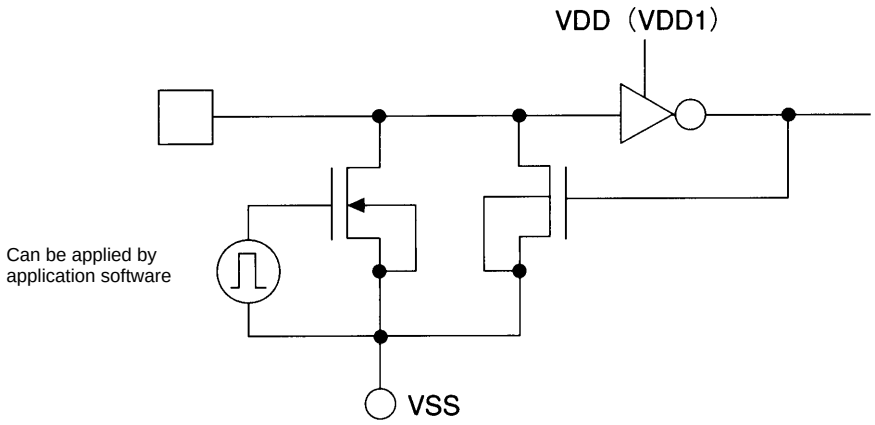

Figure 1 S1 to S4, K1 to K4, M1 to M4, A1 to A4, and SO1 to SO4

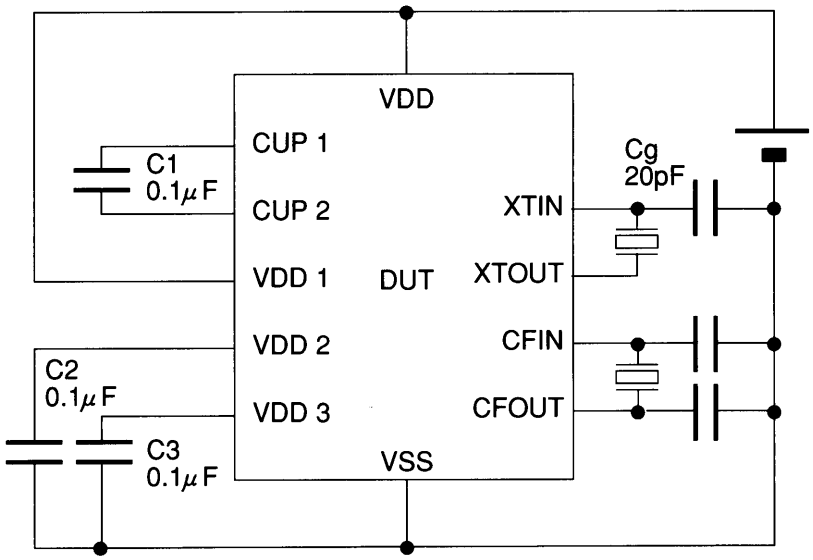

Figure 2 Output Voltage, Current Drain, and Oscillator Hold Voltage Test Circuit

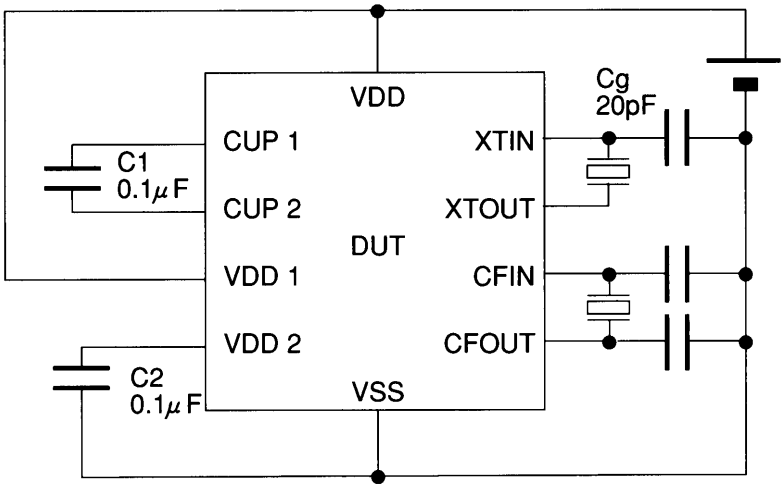

Figure 3 Output Voltage, Current Drain, and Oscillator Hold Voltage Test Circuit

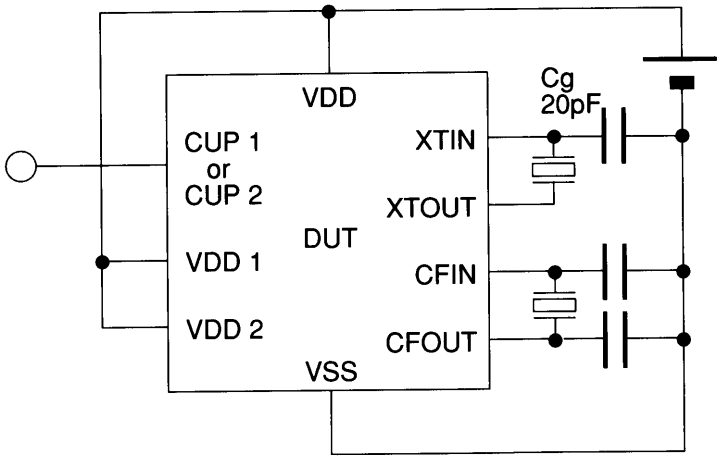

Figure 4 Oscillator Start Voltage, Oscillator Start Time, and Frequency Stability Test Circuit

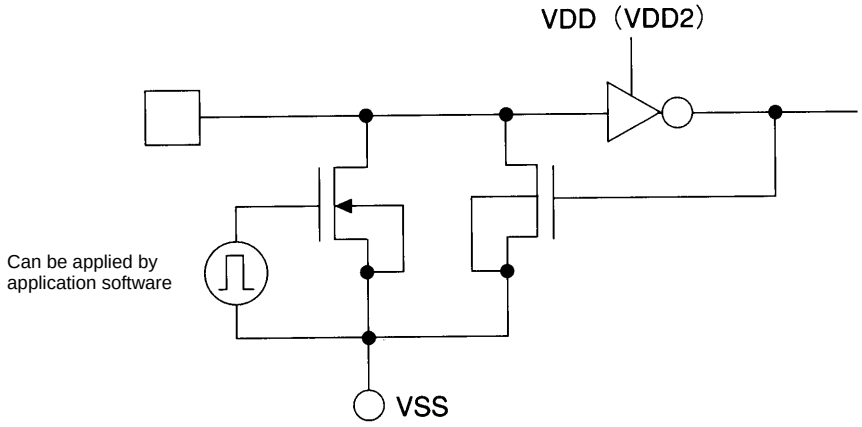

Figure 5 S1 to S4, K1 to K4, M1 to M4, A1 to A4, and SO1 to SO4

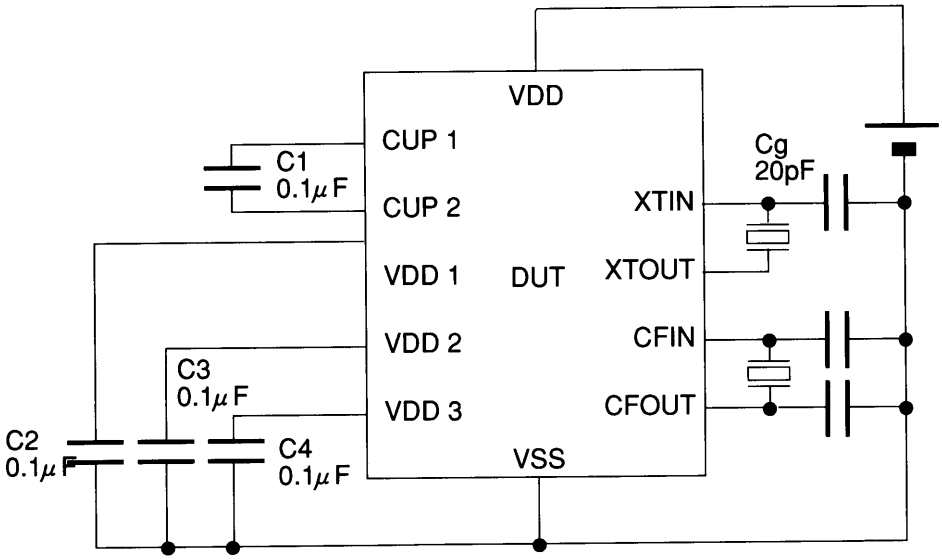

Figure 6 Output Voltage, Current Drain, and Oscillator Hold Voltage Test Circuit

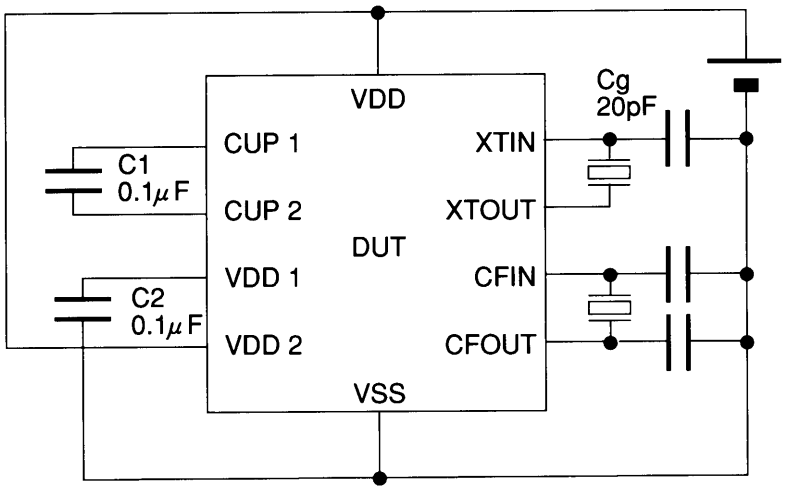

Figure 7 Output Voltage, Current Drain, and Oscillator Hold Voltage Test Circuit

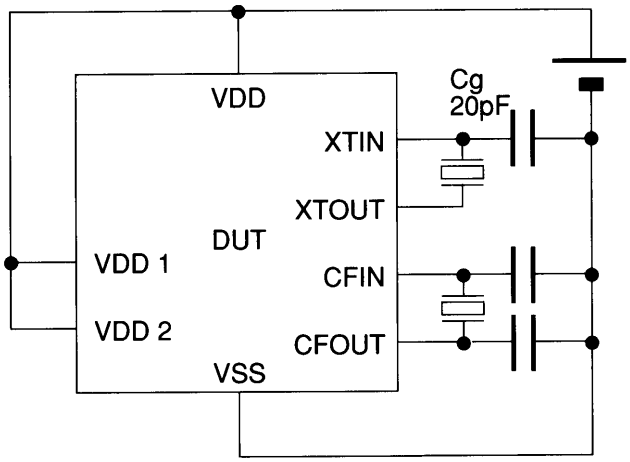

Figure 8 Output Voltage, Current Drain, and Oscillator Hold Voltage Test Circuit