



LC75374E

Electronic Volume and Tone Control for Car Stereos



Overview

The LC75374E is an electronic volume and tone control circuit that provides volume, balance, fader, bass and treble, super bass, input switching, and input and output level controls and requires a minimal number of external components to implement these functions.

Functions

- Volume: 0dB to -79dB (in 1-dB steps) and $-\infty$ dB for a total of 81 positions.
A balance function can be implemented by controlling the left and right channels independently.
- Fader: Allows either the rear or the front channel outputs to be attenuated over 16 positions.
(0 to -20dB in 2dB steps, -20 to -25dB in a 5dB step, -25 to -45dB in 10dB steps, -60dB, and $-\infty$ dB for a total of 16 positions.)
- Bass and treble: NF-type tone control circuits are formed using external CR circuits. The bass and treble can be controlled from 0dB to +11.9dB (in 1.7dB steps) for a total of 15 positions.
- Input gain: The input signal can be amplified by 0dB to +18.75dB (in 1.25dB steps).
- Output gain: The fader output can be set to one of three settings: 0dB, +6.5dB, or +8.5dB.
- Input switching: Both the left and right channels can be selected from one of four inputs.
- Super bass: This circuit provides peaking characteristics (T type characteristics) and 11 position settings.

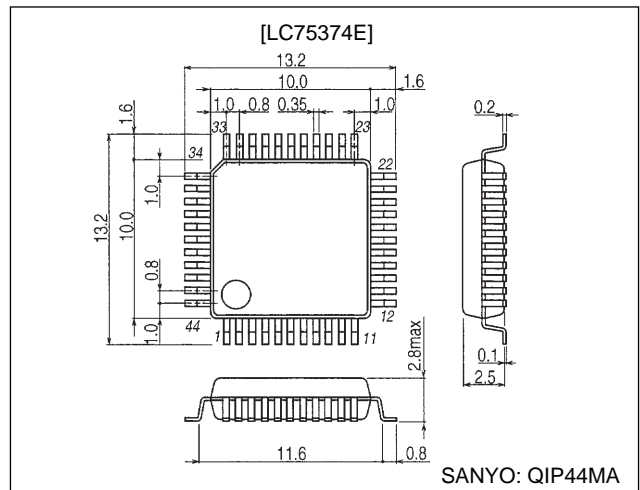
Features

- On-chip buffer amplifiers minimizes the number of external components.
- Built-in reference voltage generator for the analog ground.
- All controls can be set using the serial data input circuit (CCB).

Package Dimensions

unit: mm

3148-QIP44MA



- CCB is a trademark of SANYO ELECTRIC CO., LTD.
- CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.

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LC75374E

Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{ V}$

| Parameter | Symbol | Conditions | Ratings | Unit |
|-----------------------------|---------------------|---|----------------------------------|------------------|
| Maximum supply voltage | $V_{DD\text{ max}}$ | V_{DD} | 11 | V |
| Maximum input voltage | $V_{IN\text{ max}}$ | CL, DI, CE | $V_{SS} - 0.3$ to $V_{DD} + 0.3$ | V |
| Allowable power dissipation | $Pd\text{ max}$ | When $T_a \leq 85^\circ\text{C}$ and mounted on a printed circuit board | 720 | mW |
| Operating temperature | T_{opr} | | -40 to +85 | $^\circ\text{C}$ |
| Storage temperature | T_{stg} | | -50 to +125 | $^\circ\text{C}$ |

Allowable Operating Ranges at $T_a = -40$ to $+85^\circ\text{C}$, $V_{SS} = 0\text{ V}$

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|--------------------------|--------------------|--|----------|-----|----------|---------------|
| | | | min | typ | max | |
| Supply voltage | V_{DD} | V_{DD} | 7.5 | | 9.7 | V |
| High-level input voltage | V_{IH} | CL, DI, CE | 4.0 | | V_{DD} | V |
| Low-level input voltage | V_{IL} | CL, DI, CE | V_{SS} | | 1.0 | V |
| Input voltage amplitude | V_{IN} | CL, DI, CE, LVRIN, RVRIN, L1 to L4, R1 to R4, LFIN, RFIN, LSIN, RSIN | V_{SS} | | V_{DD} | Vp-p |
| Input pulse width | $t\phi W$ | CL | 1 | | | μs |
| Setup time | t_{setup} | CL, DI, CE | 1 | | | μs |
| Hold time | t_{hold} | CL, DI, CE | 1 | | | μs |
| Operating frequency | fopg | CL | | | 500 | kHz |

Electrical Characteristics at $T_a = 25^\circ\text{C}$, $V_{DD} = 8\text{ V}$, $V_{SS} = 0\text{ V}$

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---------------------------------|----------------------|--|---------|------------|----------|------------|
| | | | min | typ | max | |
| [Input Block] | | | | | | |
| Maximum input gain | $G_{in\text{ max}}$ | | | +18.75 | | dB |
| Step resolution | G_{step} | | | +1.25 | | dB |
| Output load resistance | R_L | | 10 | | | k Ω |
| Output impedance | R_O | LSEL0, RSEL0 : $R_L = 10\text{ k}\Omega$, $f = 1\text{ kHz}$, $V_{IN} = 1\text{ Vrms}$ | | 46 | | Ω |
| [Output Block] | | | | | | |
| Maximum output gain | $G_{out\text{ max}}$ | | | +8.5 | | dB |
| Output load resistance | R_L | | 10 | | | k Ω |
| Output impedance | R_O | LFOUT, LROUT, RFOUT, RROUT : $R_L = 10\text{ k}\Omega$, $f = 1\text{ kHz}$, $V_{IN} = 1\text{ Vrms}$ | | 35 | | Ω |
| [Volume Control Block] | | | | | | |
| Step resolution | AT_{step} | | | 1 | | dB |
| Step error | AT_{err} | STEP = 0 dB to -20 dB | -1 | 0 | +1 | dB |
| | | STEP = -20 dB to -50 dB | -3 | 0 | +3 | dB |
| Output load resistance | R_L | | 10 | | | k Ω |
| Output impedance | R_O | LTOUT, RTOUT : $R_L = 10\text{ k}\Omega$, $f = 1\text{ kHz}$, $V_{IN} = 1\text{ Vrms}$ | | 46 | | Ω |
| [Fader Volume Control Block] | | | | | | |
| Step resolution | AT_{step} | STEP = 0 dB to -20 dB | | 2 | | dB |
| | | STEP = -20 dB to -25 dB | | 5 | | dB |
| | | STEP = -25 dB to -45 dB | | 10 | | dB |
| Step error | AT_{err} | STEP = 0 dB to -45 dB | -2 | 0 | +2 | dB |
| | | STEP = -45 dB to -60 dB | -3 | 0 | +3 | dB |
| Output load resistance | R_L | | 10 | | | k Ω |
| Output impedance | R_O | LFOUT, LROUT, RFOUT, RROUT : $R_L = 10\text{ k}\Omega$, $f = 1\text{ kHz}$, $V_{IN} = 1\text{ Vrms}$ | | 46 | | Ω |
| [Bass and Treble Control Block] | | | | | | |
| Bass control range | G_{bass} | Max. Boost/Cut | ± 8 | ± 11.9 | ± 13 | dB |
| Treble control range | G_{tre} | Max. Boost/Cut | ± 8 | ± 11.9 | ± 13 | dB |
| Output load resistance | R_L | | 10 | | | k Ω |
| Output impedance | R_O | LTOUT, RTOUT : $R_L = 10\text{ k}\Omega$, $f = 1\text{ kHz}$, $V_{IN} = 1\text{ Vrms}$ | | 46 | | Ω |

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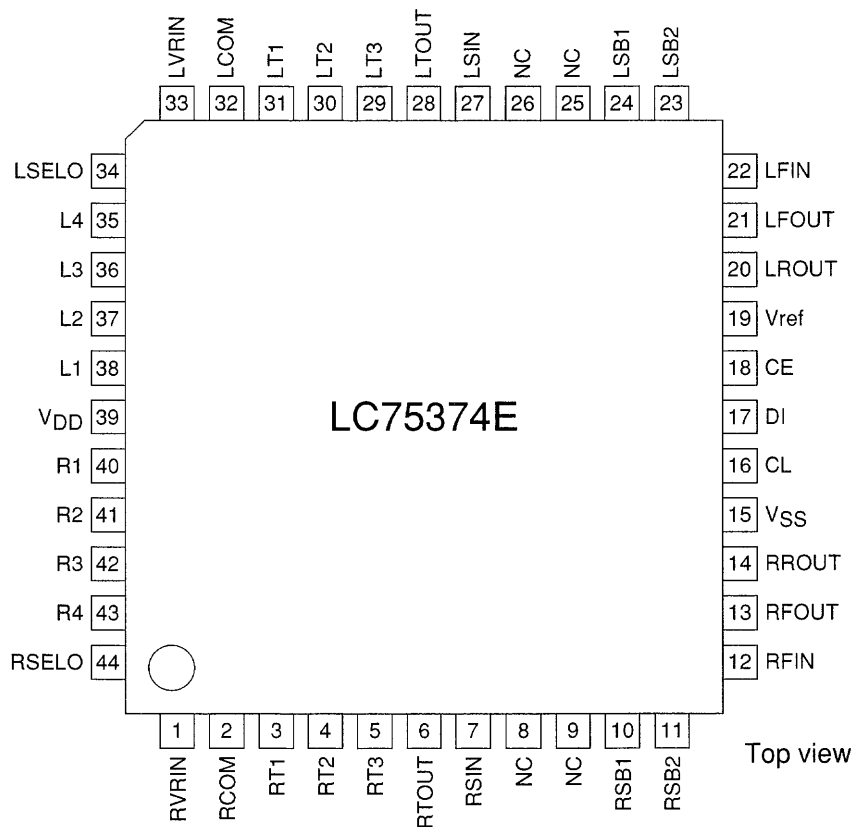
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Electrical Characteristics at $T_a = 25^\circ\text{C}$, $V_{DD} = 8\text{ V}$, $V_{SS} = 0\text{ V}$

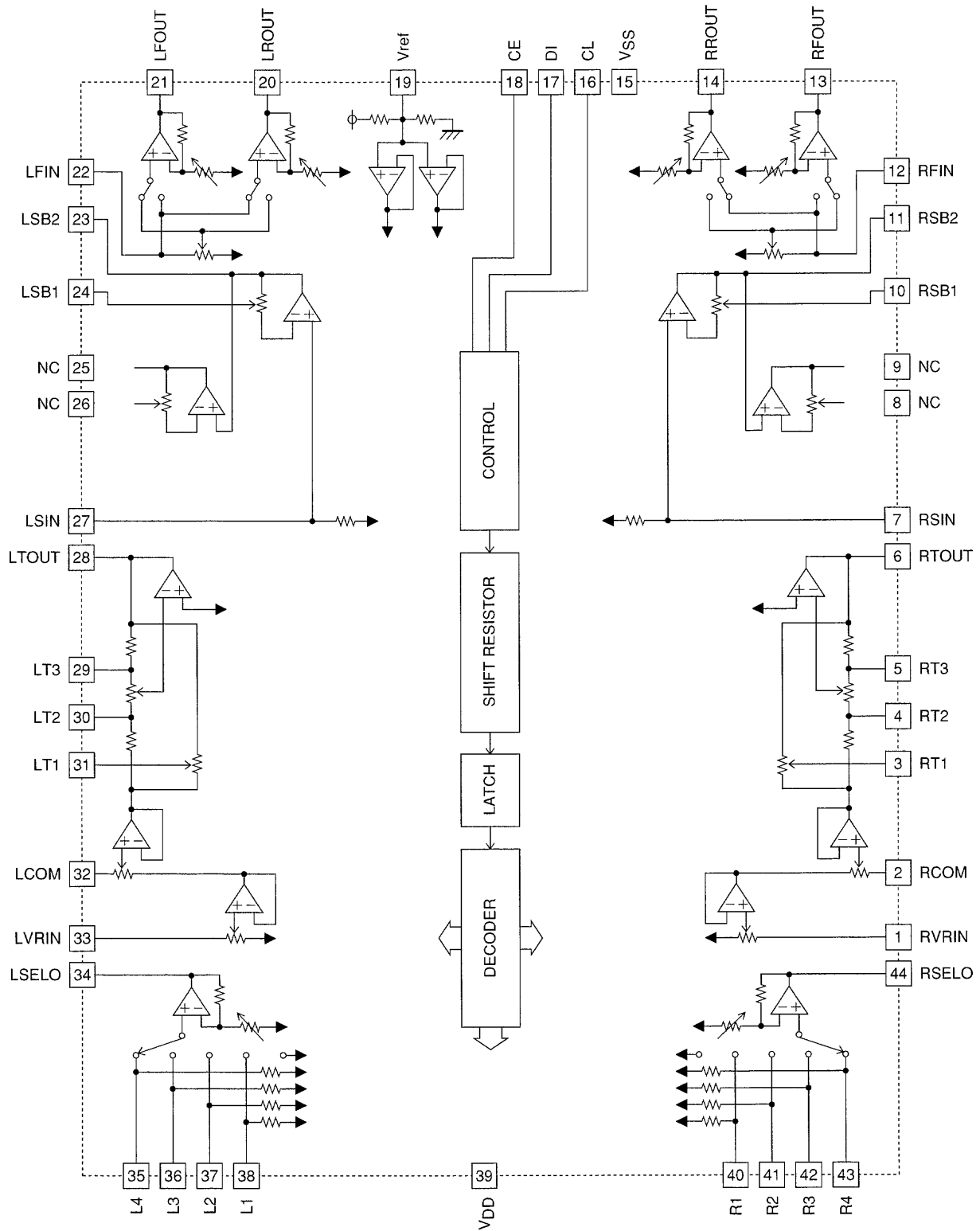
| Parameter | Symbol | Conditions | Ratings | | | Unit |
|-------------------------------|-----------|---|---------|-------|------|---------------|
| | | | min | typ | max | |
| [Super-Bass Block] (T type) | | | | | | |
| Control range | Crange | Max. Boost | | +20 | | dB |
| Step resolution | ATstep | | | +2.0 | | dB |
| Output load resistance | R_L | | 10 | | | $k\Omega$ |
| Output impedance | R_O | LSB2, RSB2 : $R_L = 10\text{ k}\Omega$, $f = 1\text{ kHz}$, $V_{IN} = 1\text{ Vrms}$ | | 70 | | Ω |
| [Overall] | | | | | | |
| Total harmonic distortion | THD | $V_{IN} = 1\text{ Vrms}$, $f = 1\text{ kHz}$, All controls flat overall | | 0.003 | 0.01 | % |
| Crosstalk | CT | $V_{IN} = 1\text{ Vrms}$, $f = 1\text{ kHz}$, All controls flat overall, $R_g = 1\text{ k}\Omega$ | | 80.5 | | dB |
| Output at maximum attenuation | V_o min | $V_{IN} = 1\text{ Vrms}$, $f = 1\text{ kHz}$, Main volume setting: $-\infty$ | | -80 | | dB |
| Output noise voltage | V_{N1} | All controls flat overall, (IHF-A), $R_g = 1\text{ k}\Omega$ | | 8 | | μV |
| | V_{N2} | All controls flat overall, (DIN-AUDIO), $R_g = 1\text{ k}\Omega$ | | 10 | | μV |
| High-level input voltage | I_{IH} | CL, DI, CE, $V_{IN} = 8\text{ V}$ | | | 10 | μA |
| Low-level input voltage | I_{IL} | CL, DI, CE, $V_{IN} = 0\text{ V}$ | -10 | | | μA |

Pin Assignment



A10540

Equivalent Circuit

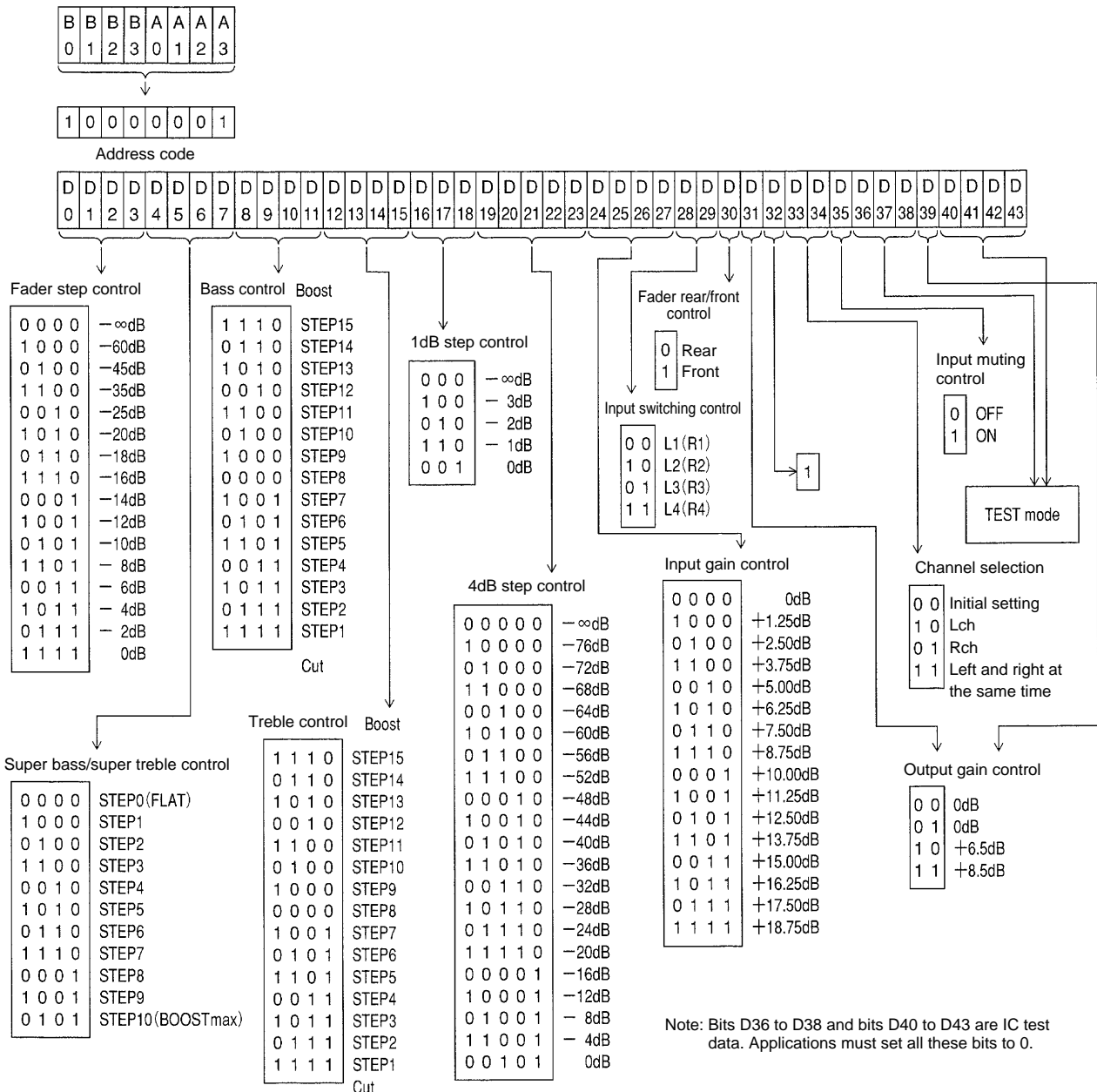
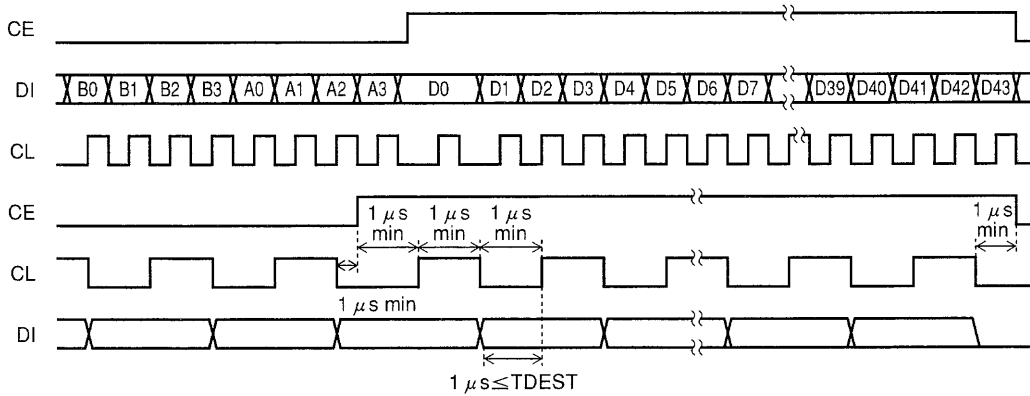


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LC75374E

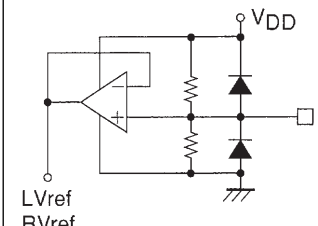
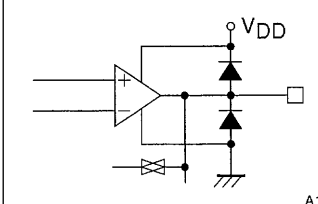
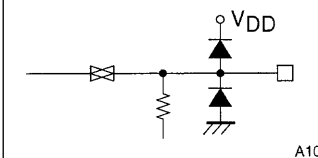
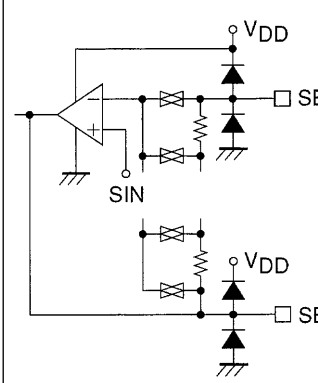
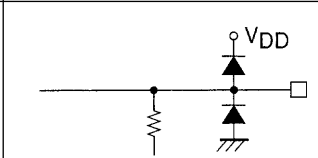
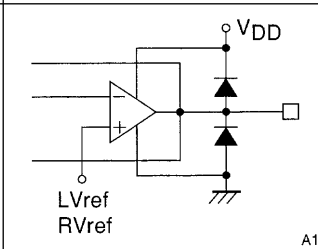
Control System Timing and Data Format

Applications must input the stipulated serial data to the CE, CL, and DI pins to control the LC75374E. The data consists of a total of 52 bits, of which 8 bits are address and 44 bits are data.



LC75374E

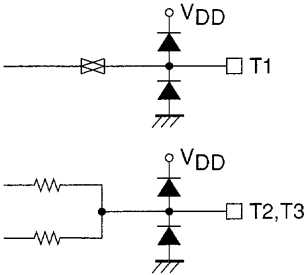
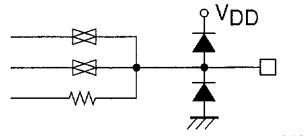
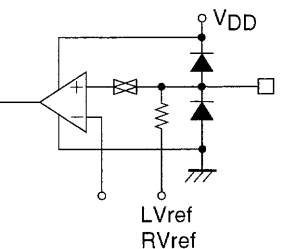
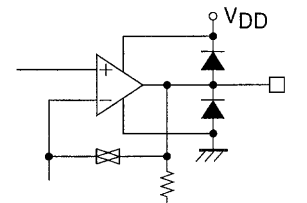
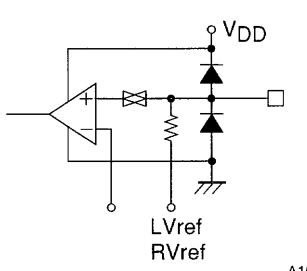
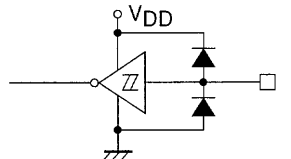
Pin Functions

| Pin No. | Pin | Description | Notes |
|----------------------|----------------------------------|--|--|
| 19 | Vref | <ul style="list-style-type: none"> Supply voltage generator ($0.525 \times V_{DD}$) used for the analog ground. A capacitor must be connected between Vref and V_{SS} to remove power supply ripple. |  <p style="text-align: right;">A10543</p> |
| 20 21 14 13 | LROUT LFOUT RROUT RFOUT | <ul style="list-style-type: none"> Fader outputs. The front and rear outputs can be attenuated independently. |  <p style="text-align: right;">A10544</p> |
| 22 12 | LFIN RFIN | <ul style="list-style-type: none"> Fader inputs These inputs must be driven by low-impedance circuits. |  <p style="text-align: right;">A10545</p> |
| 24 23 10 11 | LSB1 LSB2 RSB1 RSB2 | <ul style="list-style-type: none"> Left channel super bass compensation capacitor connection Left channel super bass output and compensation capacitor connection Right channel super bass compensation capacitor connection Right channel super bass output and compensation capacitor connection |  <p style="text-align: right;">A10547</p> |
| 22 7 | LSIN RSIN | <ul style="list-style-type: none"> Super bass input These inputs must be driven by low-impedance circuits. |  <p style="text-align: right;">A10548</p> |
| 28 6 | LTOUT RTOUT | <ul style="list-style-type: none"> Tone control outputs |  <p style="text-align: right;">A10549</p> |

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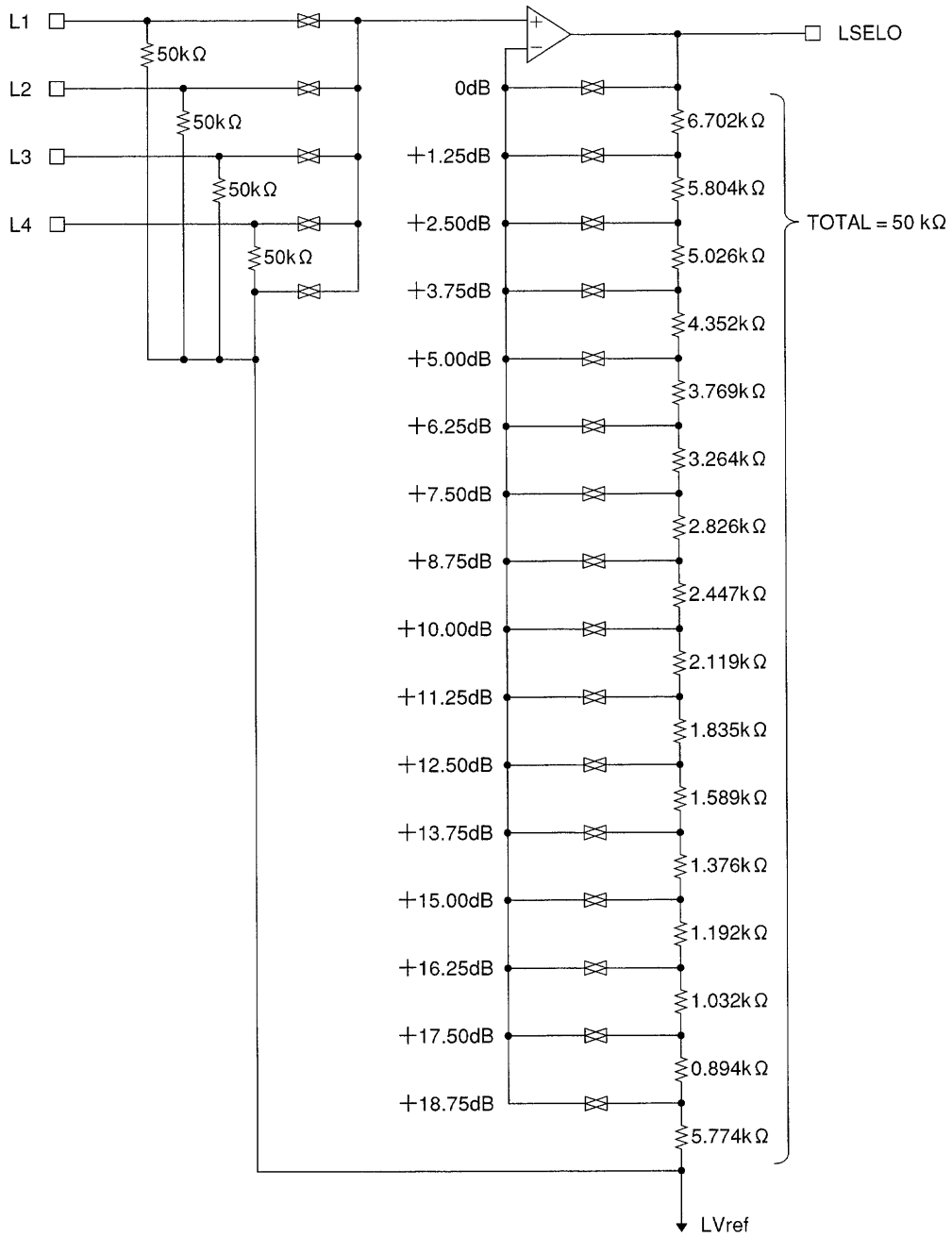
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| Pin No. | Pin | Description | Notes |
|--|--|---|--|
| 31 30 29 3 4 5 | LT1 LT2 LT3 RT1 RT2 RT3 | <ul style="list-style-type: none"> Tone control circuit bass and treble compensation capacitor connections. Connect the high band compensation capacitors between the pins T1 and T2. Connect the low band compensation capacitors between the pins T2 and T3. |  <p style="text-align: right;">A10550</p> |
| 32 2 | LCOM RCOM | <ul style="list-style-type: none"> 1dB volume control common connections |  <p style="text-align: right;">A10551</p> |
| 33 1 | LVRIN RVRIN | <ul style="list-style-type: none"> 4dB volume control inputs These inputs must be driven by low-impedance circuits. |  <p style="text-align: right;">A10552</p> |
| 34 44 | LSEL0 RSEL0 | <ul style="list-style-type: none"> Input selector outputs |  <p style="text-align: right;">A10553</p> |
| 38 37 36 35 40 41 42 43 | L1 L2 L3 L4 R1 R2 R3 R4 | <ul style="list-style-type: none"> Signal inputs |  <p style="text-align: right;">A10554</p> |
| 39 | V _{DD} | <ul style="list-style-type: none"> Power supply | |
| 15 | V _{SS} | <ul style="list-style-type: none"> Ground | |
| 16 17 | CL DI | <ul style="list-style-type: none"> Serial data and clock inputs used for transferring control data | |
| 18 | CE | <ul style="list-style-type: none"> Chip enable input. Data is written into the internal latches and the analog switches operate when this pin goes from high to low. Data transfers are enabled when this pin is high. |  <p style="text-align: right;">A10555</p> |
| 8, 26 9, 25 | NC | <ul style="list-style-type: none"> Unused pins. These pins must be connected to V_{SS}. Unused pins. These pins must be left open. | |

LC75374E

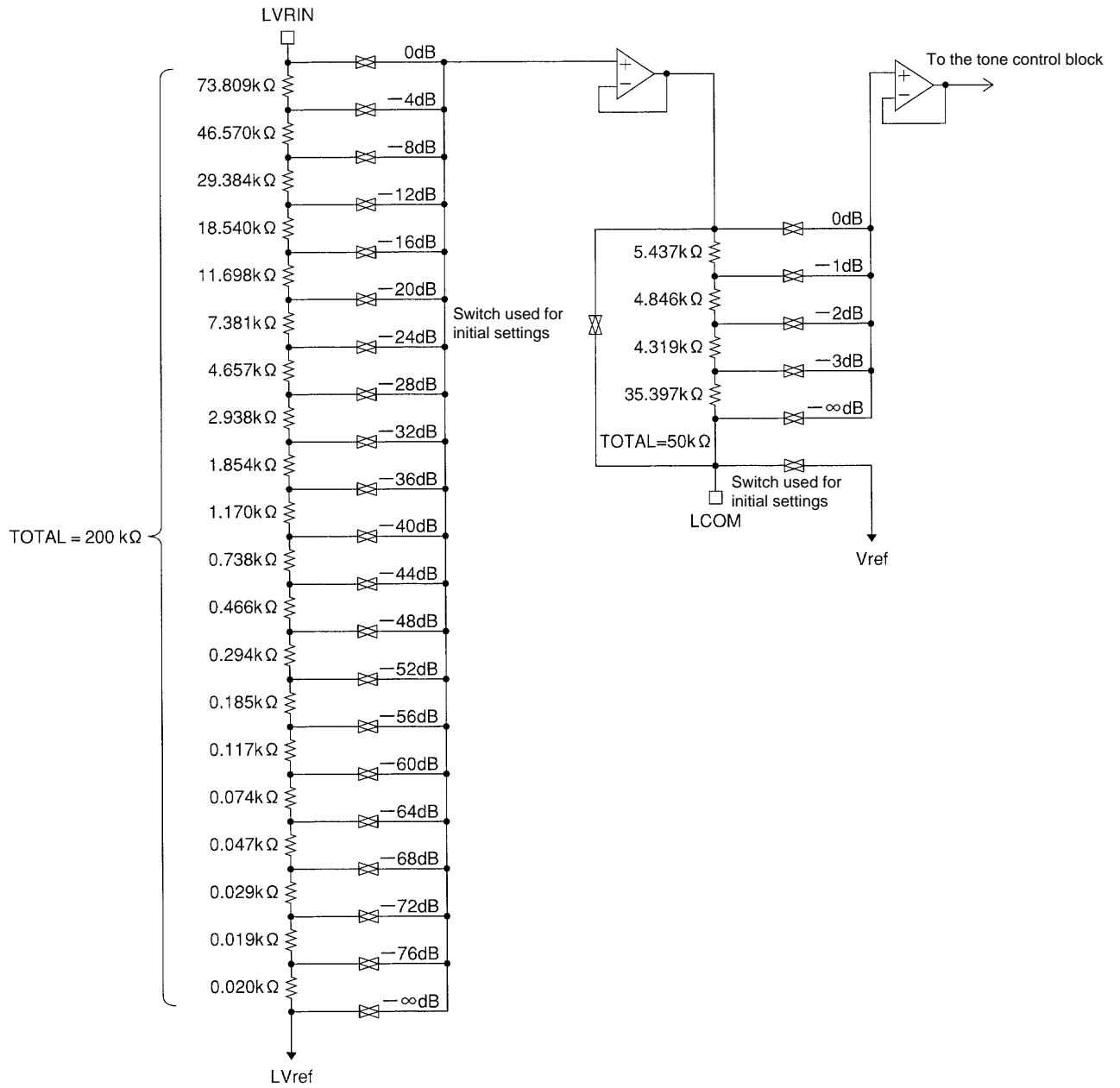
Input Block Equivalent Circuit



A10556

The right channel is identical.

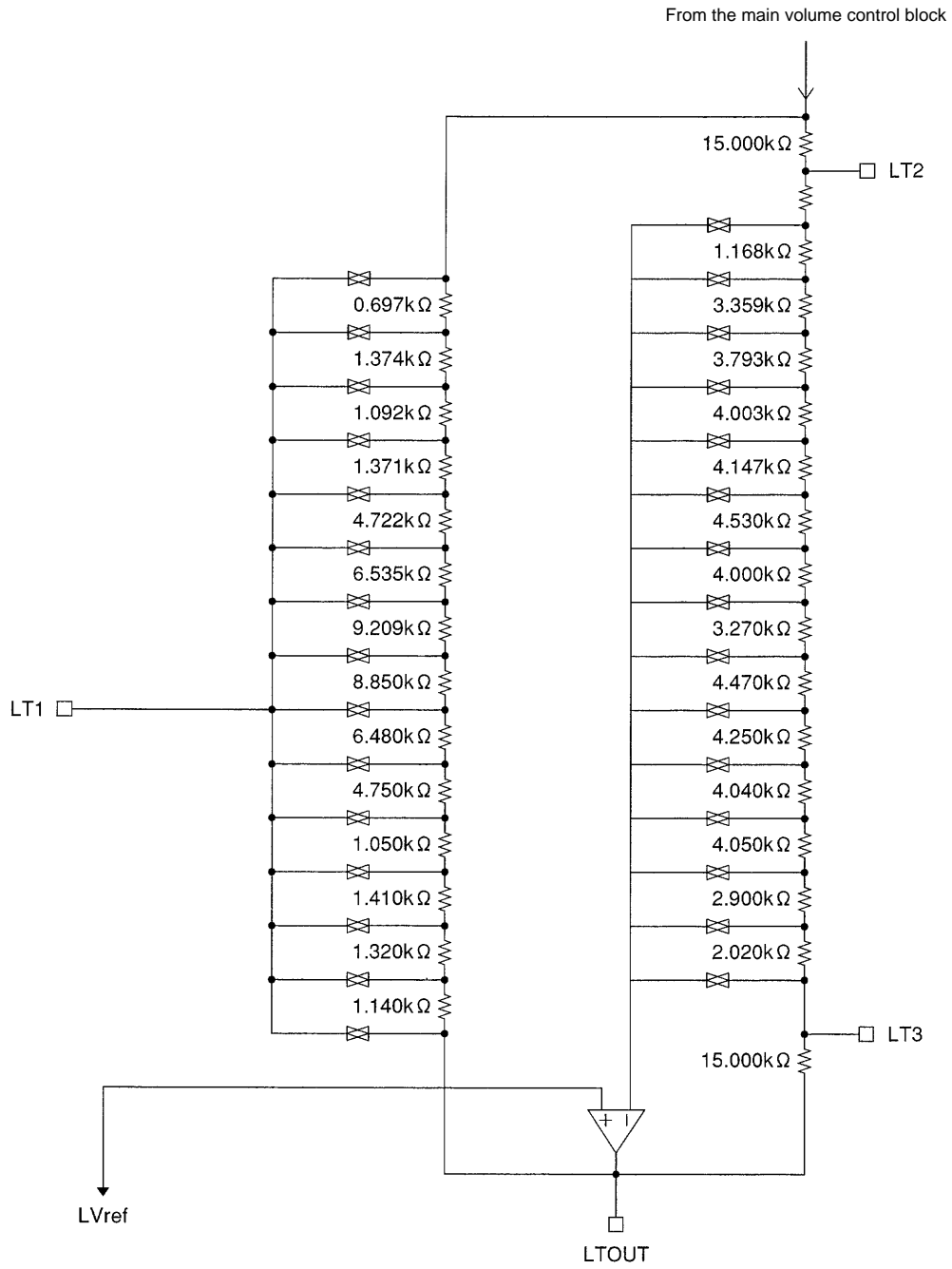
Main Volume Control Block Equivalent Circuit



A10557

The right channel is identical.

Tone Block Equivalent Circuit

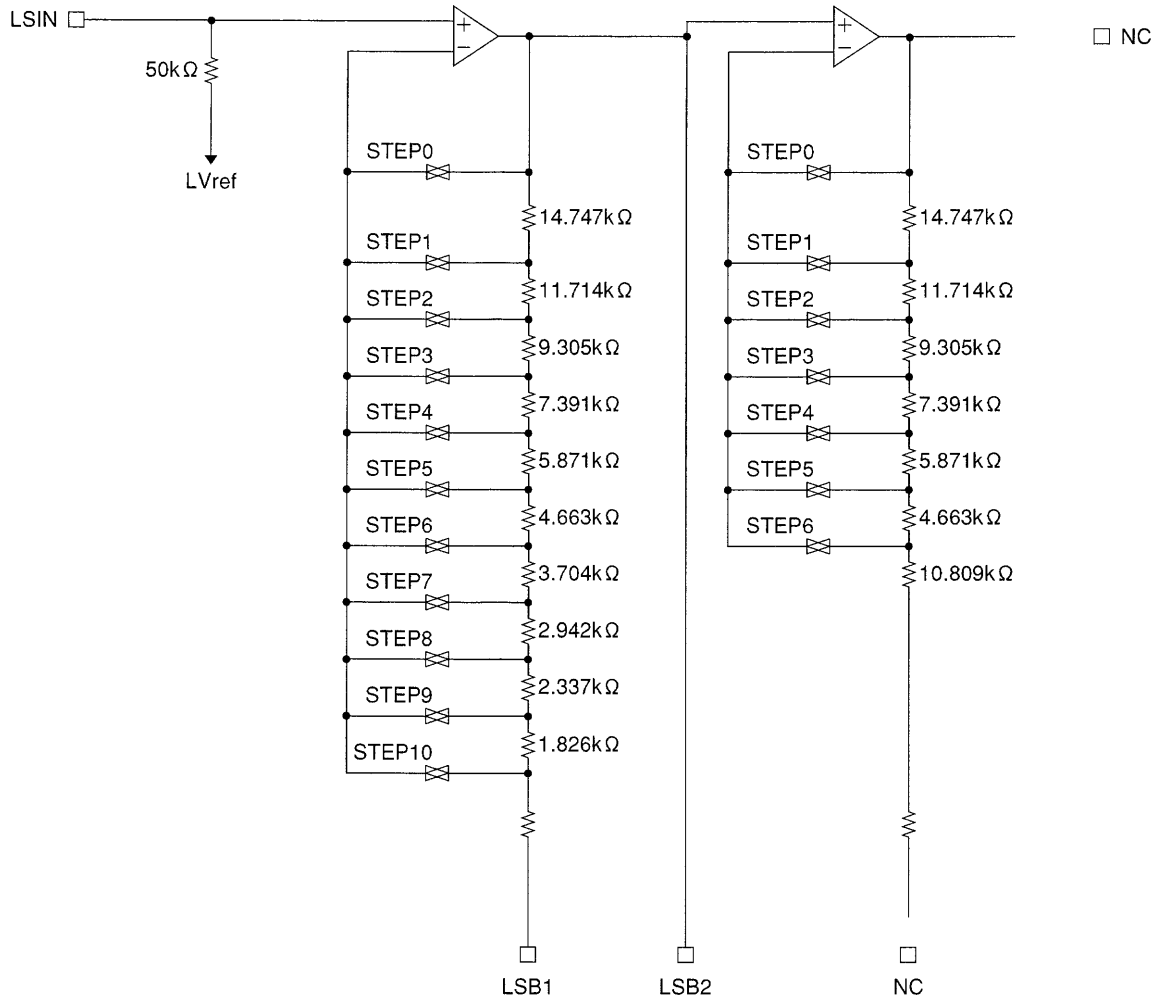


A10558

The right channel is identical.

LC75374E

Super Bass Block Equivalent Circuit



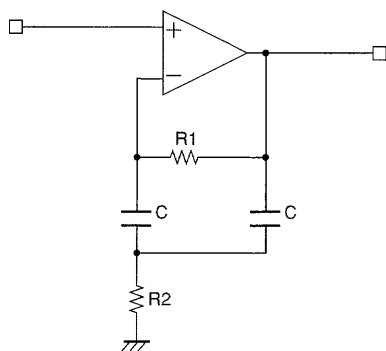
A10559

The right channel is identical.

Sample external constant calculations for the super bass (T type) circuit when full boost is used

The external constants required when full boost is used with the super bass block (T type) are calculated as follows.

- Super bass (T type) equivalent circuit



A10560

Sample calculation

Assume:

R1 = 64.5 kΩ, and

G = 20.65 dB, and

f0 = 72.7 Hz.

- Calculation

(1) Center frequency

$$f_0 = \frac{1}{2 \times \pi \times \sqrt{R1 \times R2 \times C \times C}}$$

(2) Gain

$$G = 20 \log \left(1 + \frac{R1}{2 \times R2} \right)$$

(3) Q

$$Q = \frac{C \times C \times R1}{2 \times C} \times \frac{1}{\sqrt{R1 \times R2 \times C \times C}}$$

- Determine R2

Determine R2 from formula (2).

$$R2 = \frac{64.5}{2 \times (10.78 - 1)} \approx 3.3 \text{ (k}\Omega\text{)}$$

- Determine C

Determine C from formula (1).

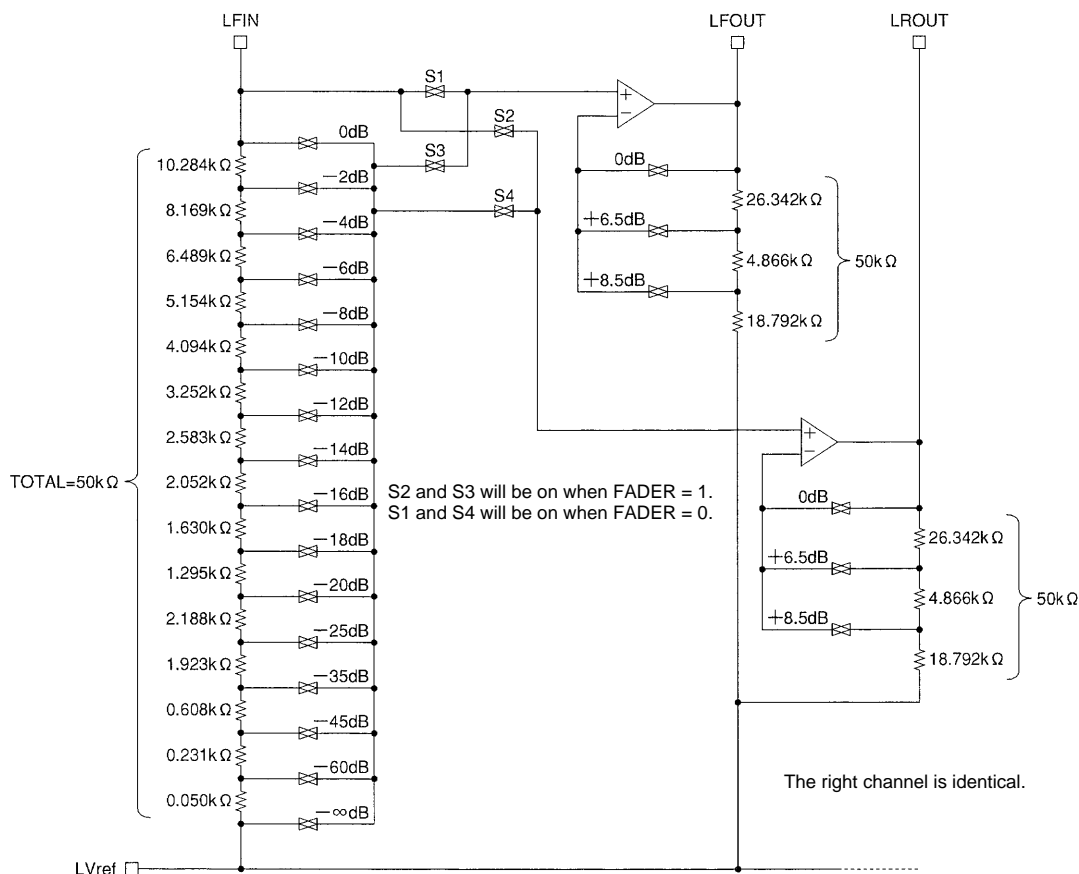
$$C = \frac{1}{\sqrt{R1 \times R2 \times (2 \times \pi \times f_0) \times (2 \times \pi \times f_0)}} \approx 0.15 \text{ (}\mu\text{F)}$$

- Determine Q

Determine Q from formula (3).

Here, Q will be 2.21.

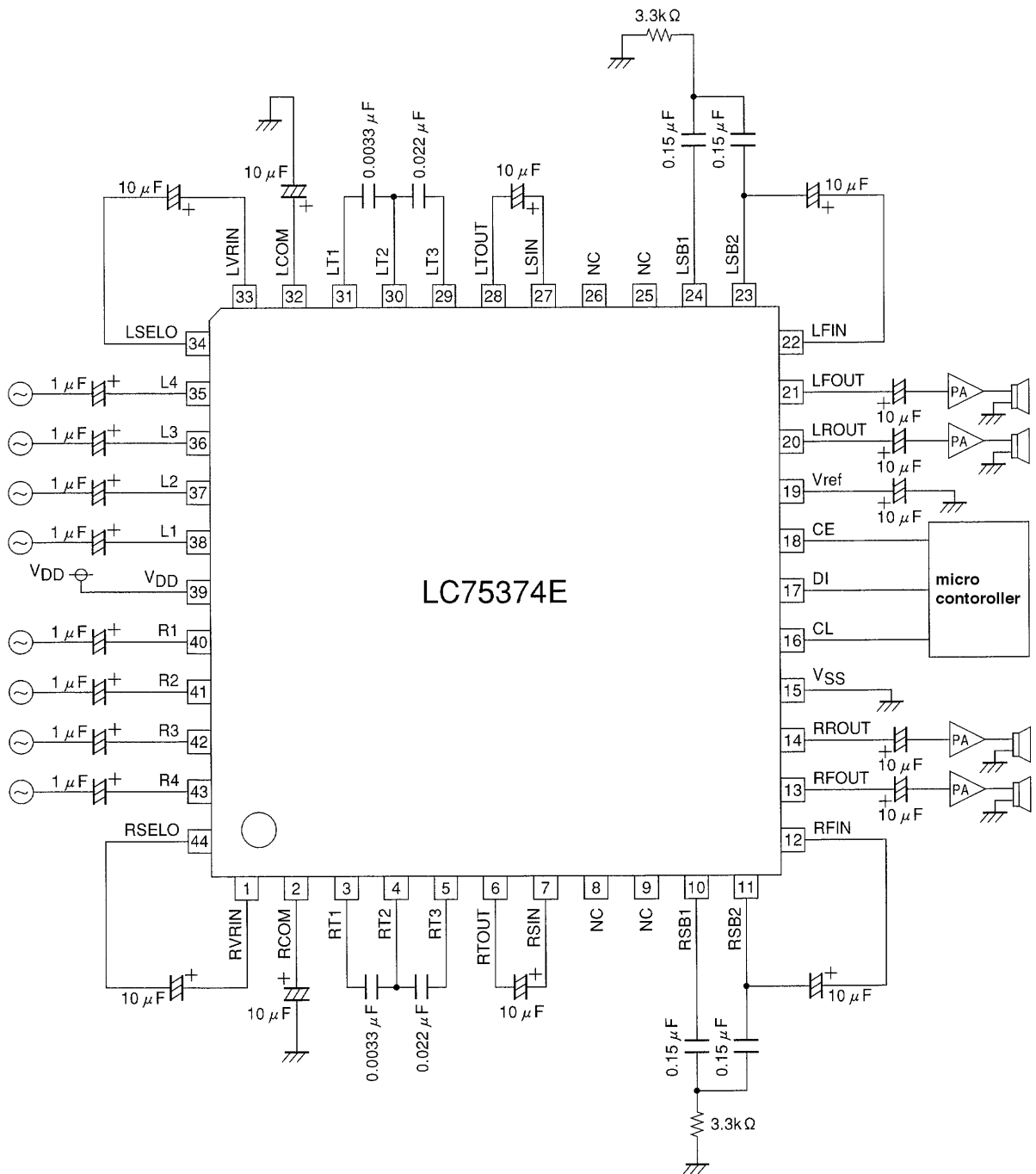
Fader Volume Control Block Equivalent Circuit



A10561

At the point that data corresponding to $-\infty$ is transferred to the 1dB $-\text{step}$ main volume control block, S1 and S2 will go to the open state. S3 and S4 will go to the on state at the same time.

Sample Application Circuit

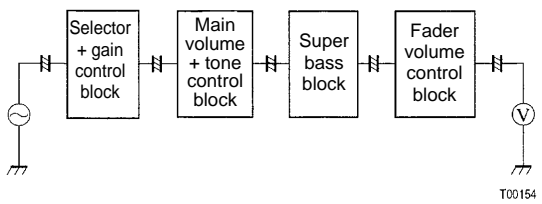
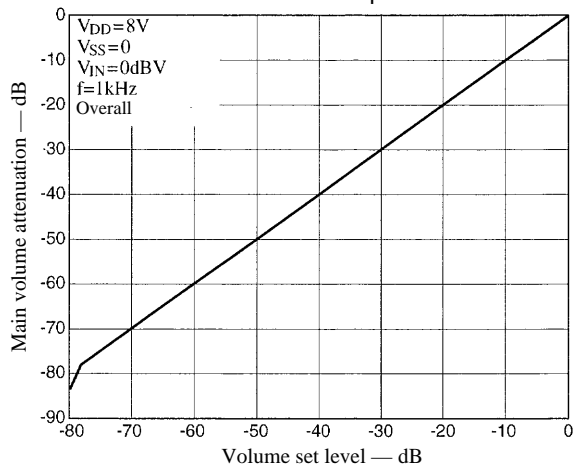


A10562

Usage Notes

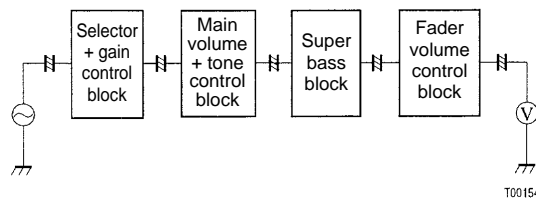
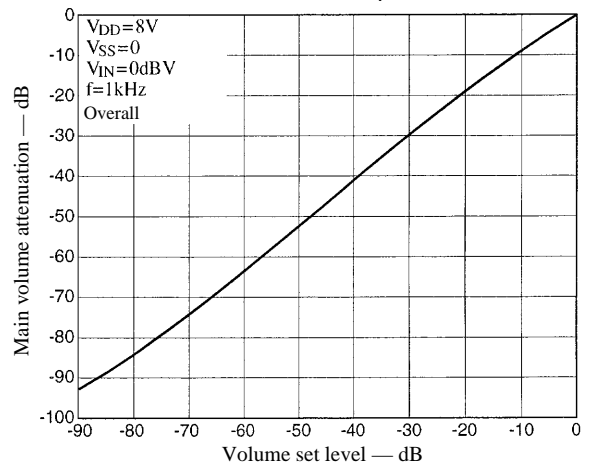
- The internal analog switches are in undefined states when power is first applied. Applications must therefore use external circuits to mute the output until control data has been transferred.
- When setting up the initial data after power is first applied, applications must first transfer a set of IC initialization data. This initialization data consists of an address field of (10000001) and a data field of all zeros (D0 to D43 = 0). Applications must only send the actual initial data after this initialization data has been sent.
- Applications must either cover the CL, DI, and CE lines with the ground pattern or use shielded cables for these lines to prevent the high-frequency digital signals that are transmitted over these lines from entering the analog signal system.

Main Volume Control Step Characteristics



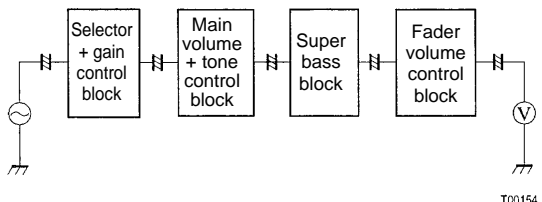
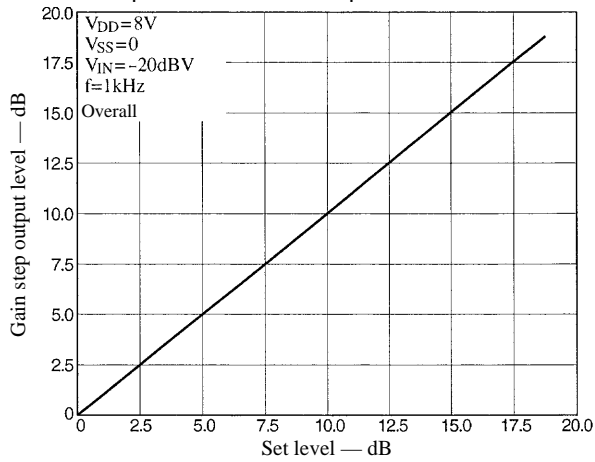
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Fader Volume Control Step Characteristics



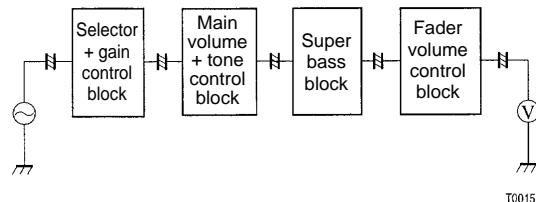
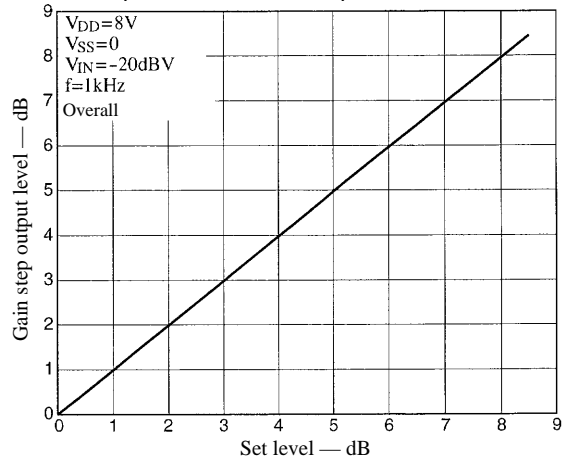
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Input Gain Control Step Characteristics

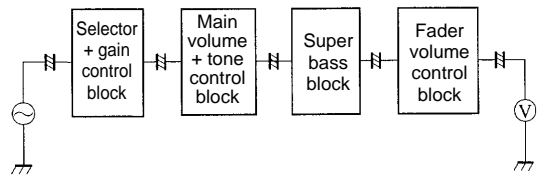
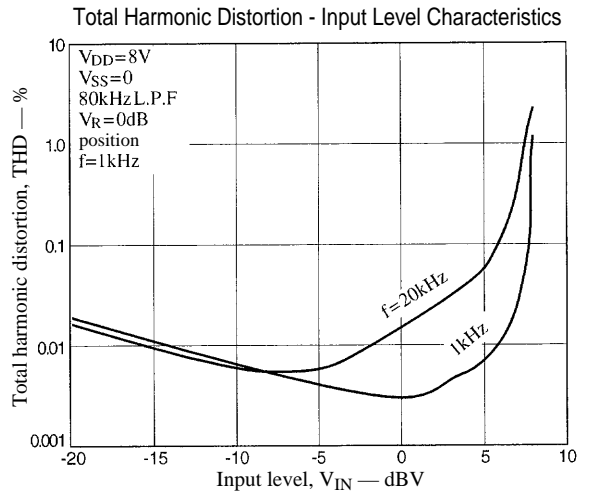
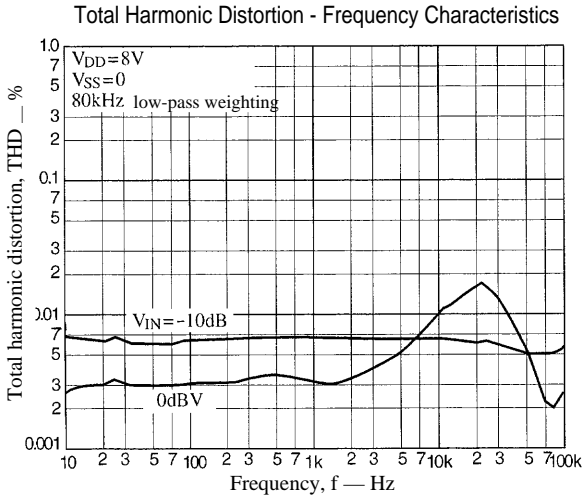


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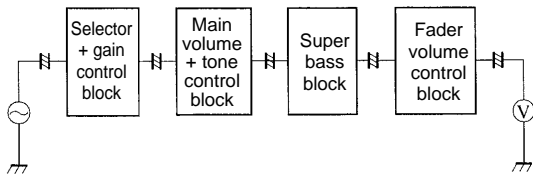
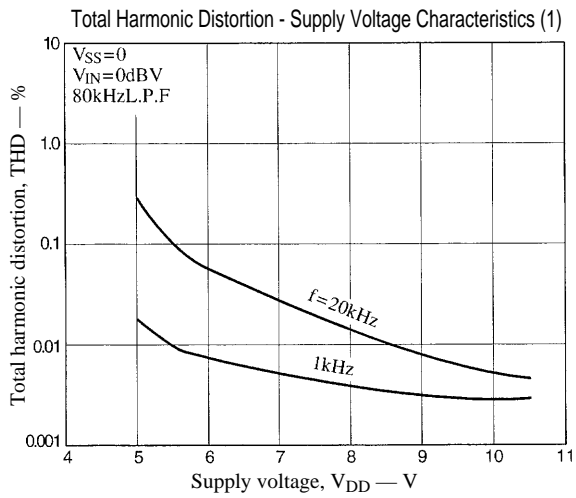
Output Gain Control Step Characteristics



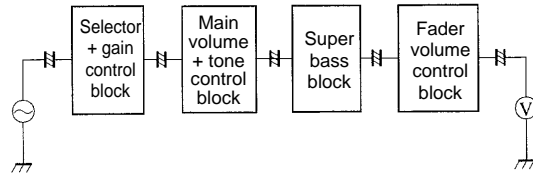
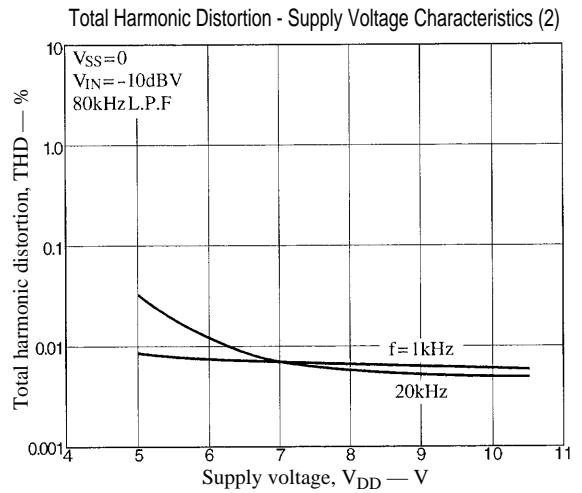
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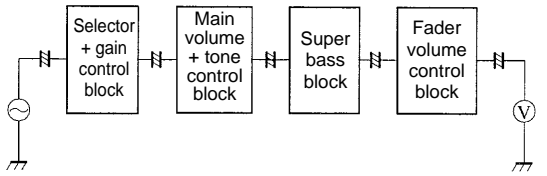
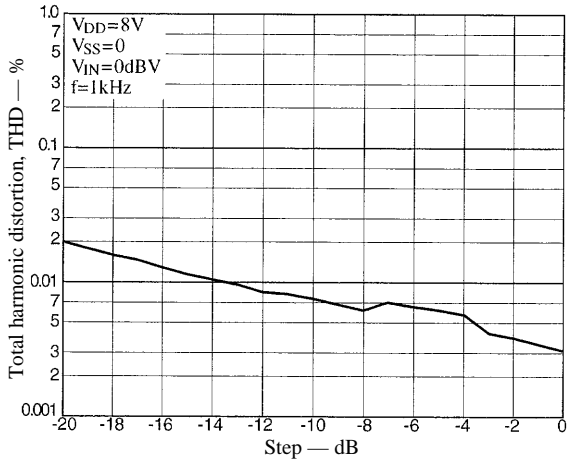


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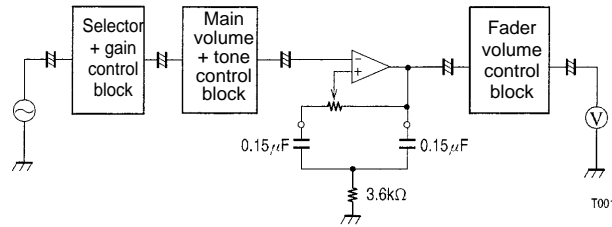
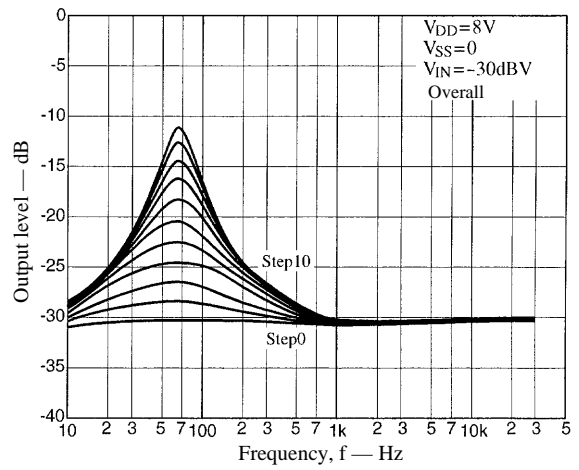
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Total Harmonic Distortion – Main Volume Control Step Characteristics



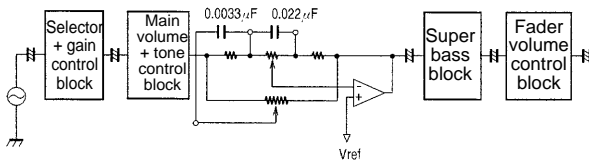
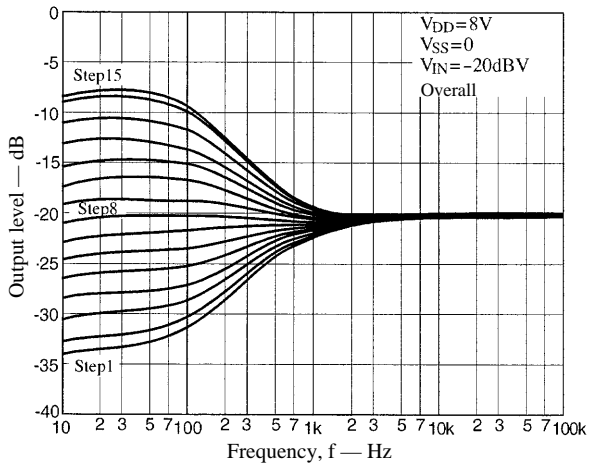
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Super Bass Characteristics



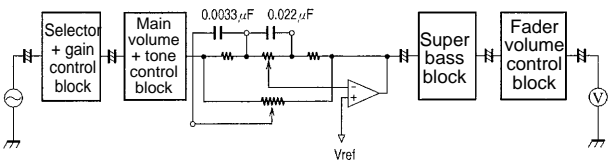
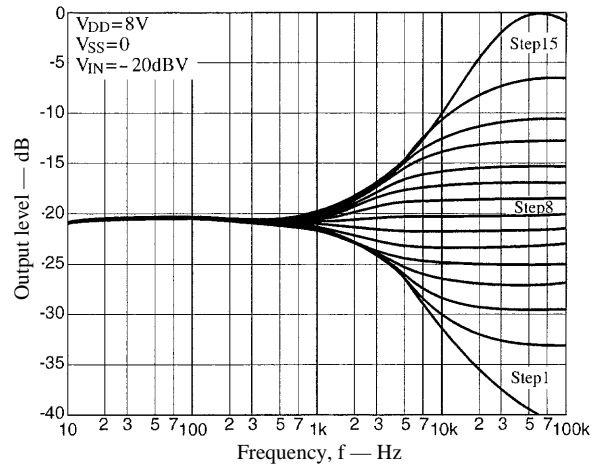
T00155

Bass Characteristics



T00156

Treble Characteristics



T00156

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