



# LC78855KM

## Digital Audio D/A Converter with Built-in Digital Filters

### Preliminary

### Overview

The LC78855KM is a  $\Sigma\Delta$  D/A converter with built-in digital filters for use in digital audio products.

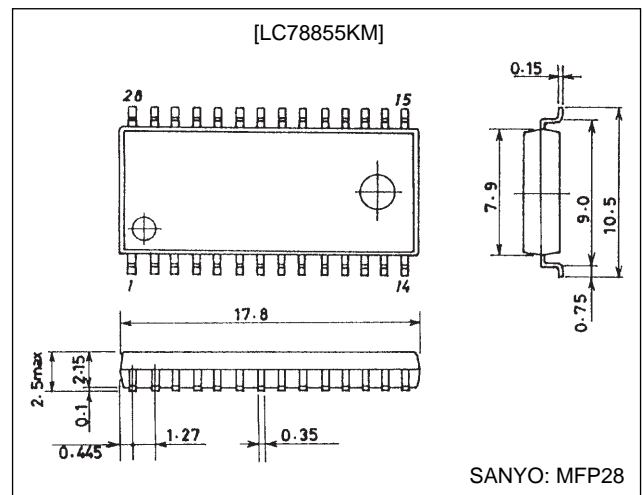
### Features

- 8× oversampling digital filters
- Digital de-emphasis (for  $F_s = 44.1$  kHz)
- Digital attenuation (with serial input)
- Soft muting (with parallel inputs)
- Supports double-speed playback.
- Supports a 384 fs system clock.
- PWM output
- Single 5 V power supply
- Si gate CMOS process

### Package Dimensions

unit: mm

3091-MFP28



### Specifications

#### Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD}$ max		-0.3 to +7.0	V
Maximum input voltage	$V_{IN}$ max		-0.3 to $V_{DD} + 0.3$	V
Maximum output voltage	$V_{OUT}$ max		-0.3 to $V_{DD} + 0.3$	V
Operating temperature	$T_{opr}$		-30 to +75	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-40 to +125	$^\circ\text{C}$

#### Allowable Operating Ranges at $T_a = -30$ to $+75^\circ\text{C}$

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	$V_{DD}$		4.5	5.0	5.5	V
Input voltage range	$V_{IN}$		0		$V_{DD}$	V

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## LC78855KM

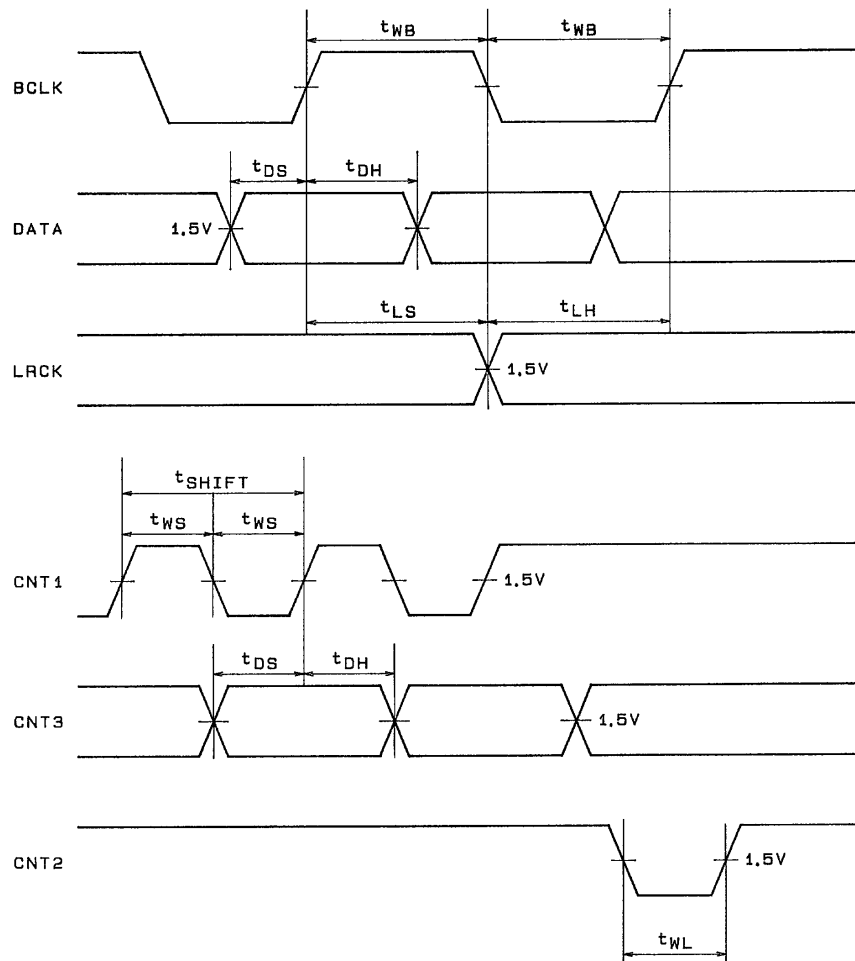
### DC Characteristics at $T_a = -30$ to $+75^\circ\text{C}$ , $V_{DD} = 4.5$ to $5.5$ V, $V_{SS} = 0$ V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high level voltage (1)	$V_{IH1}$	The XIN pin	$0.7 V_{DD}$			V
Input low level voltage (2)	$V_{IL1}$	The XIN pin			$0.3 V_{DD}$	V
Input high level voltage (1)	$V_{IH2}$	Pins other than the XIN pin	2.2			V
Input low level voltage (2)	$V_{IL2}$	Pins other than the XIN pin			0.8	V
Output high level voltage	$V_{OH}$	$I_{OH} = -1 \mu\text{A}$	$V_{DD} - 0.1$			V
Output low level voltage	$V_{OL}$	$I_{OL} = 1 \mu\text{A}$			0.1	V
Allowable power dissipation	$P_d$	$V_{DD} = 5.0$ V		175	250	mW

### AC Characteristics at $T_a = -30$ to $+75^\circ\text{C}$ , $V_{DD} = 4.5$ to $5.5$ V, $V_{SS} = 0$ V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Oscillator frequency	$f_X$			16.9	18.5	MHz
BCLK frequency	$f_{BCK}$				2.4	MHz
BCLK pulse width	$t_{WB}$		100			ns
Data setup time	$t_{DS}$		20			ns
Data hold time	$t_{DH}$		20			ns
LRCK setup time	$t_{LS}$		50			ns
LRCK hold time	$t_{LH}$		50			ns
CNT1 pulse period	$t_{SHIFT}$		1000			ns
CNT1 pulse width	$t_{WS}$		300			ns
CNT2 pulse width	$t_{WL}$		300			ns

### Timing Diagrams



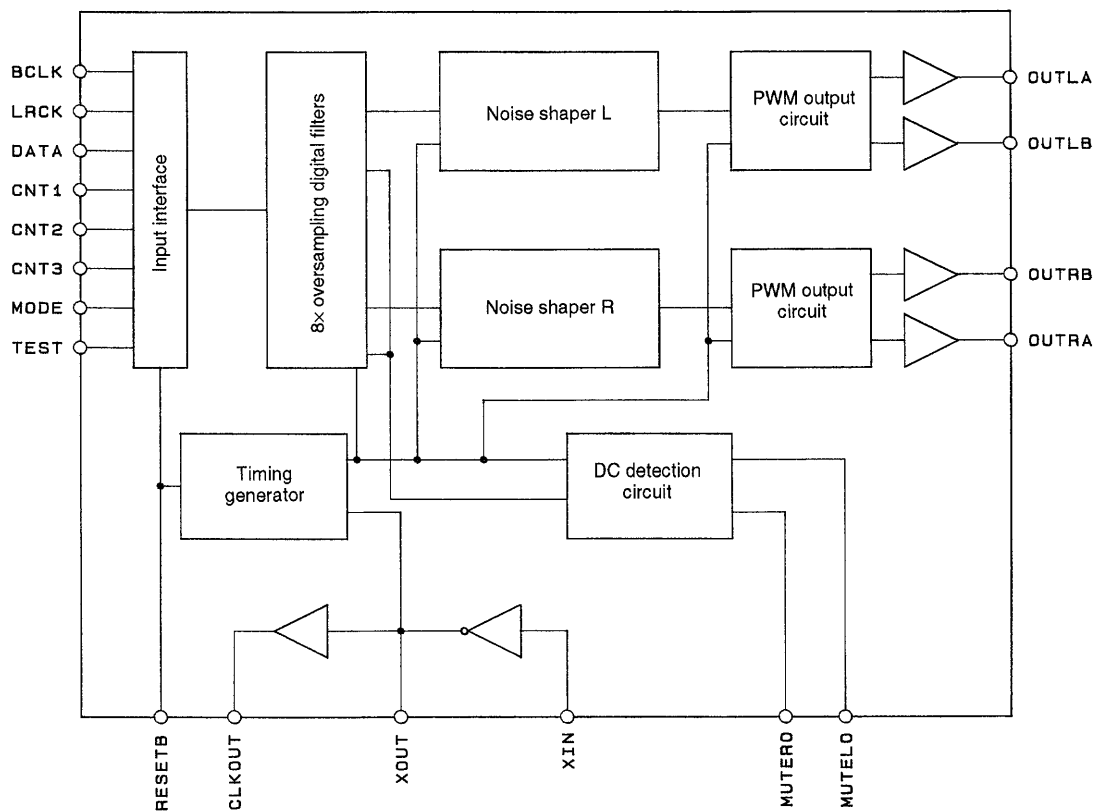
# LC78855KM

## Analog Characteristics at $T_a = 25^\circ\text{C}$ , $V_{DD} = 5.0\text{ V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Total harmonic distortion	THD + N	1 kHz, 0 dB			0.01	%
Signal-to-noise ratio	S/N	JIS-A	93			dB
Crosstalk	CT	1 kHz, 0 dB	80			dB
Full-scale output level	VFS	*		1.7		V <sub>rms</sub>
Dynamic range	DR	JIS-A	83			dB

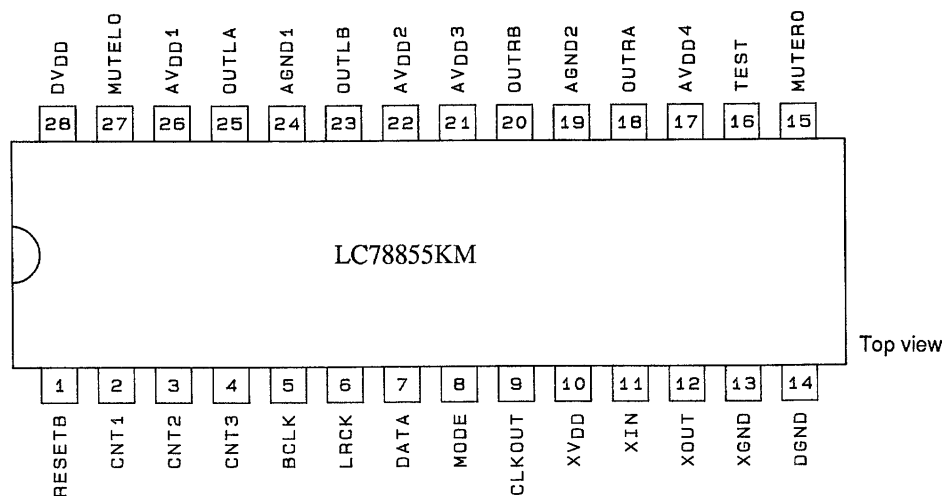
Note: \* For a 1 kHz, 0 dB input, measured in the circuit presented as a sample application circuit.

## Block Diagram



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## Pin Assignment



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## LC78855KM

### Pin Functions

Pin No.	Function	Description
1	RESETB	Reset input (Internal circuits are initialized when a low level is input to this pin.)
2	CNT1	When MODE = low: Control data shift clock When MODE = high: Emphasis on/off switch
3	CNT2	When MODE = low: Control data latch signal input When MODE = high: Standard speed/double speed switch
4	CNT3	When MODE = low: Control data input When MODE = high: Soft muting input
5	BCLK	Bit clock input
6	LRCK	LR clock input
7	DATA	Digital audio data input
8	MODE	Serial/parallel input setting
9	CLKOUT	Clock output
10	XV <sub>DD</sub>	Oscillator amplifier power supply
11	XIN	Oscillator amplifier input
12	XOUT	Oscillator amplifier output
13	XGND	Oscillator amplifier ground
14	DGND	Digital system ground
15	MUTERO	Right channel muting signal output
16	TEST	Test pin (Must be tied low in normal operation.)
17	AV <sub>DD4</sub>	Analog system power supply
18	OUTRA	Right channel output A
19	AGND2	Analog system ground
20	OUTRB	Right channel output B
21	AV <sub>DD3</sub>	Analog system ground
22	AV <sub>DD2</sub>	Analog system ground
23	OUTLB	Left channel output B
24	AGND1	Analog system ground
25	OUTLA	Left channel output A
26	AV <sub>DD1</sub>	Analog system ground
27	MUTELO	Left channel muting signal output
28	DV <sub>DD</sub>	Digital system power supply

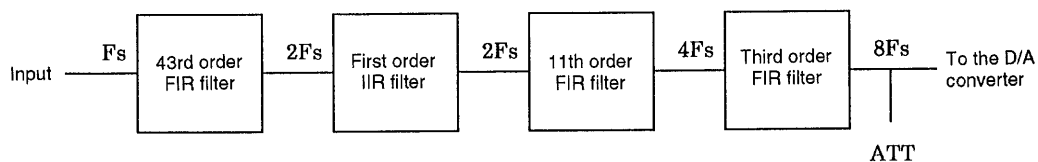
### LC78855KM Operation

The LC78855KM consists of two major sections; a digital filter block and a D/A converter.

#### 1. Digital Filter Block

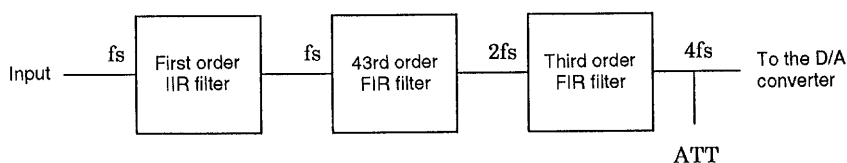
- Standard speed operation

The LC78855KM implements 8× oversampling using three filters: a 43rd order FIR filter, an 11th order FIR filter and a third order FIR filter. De-emphasis is performed using a first order IIR filter.



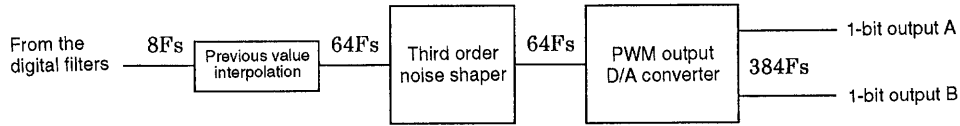
- Double speed operation

This mode is used, for example, for dubbing a CD to a cassette at double speed. The XIN pin functions in the same manner as in standard mode, but the BCLK, LRCK and DATA signals are input at twice the speed. After de-emphasis is performed with a first order IIR filter 4× oversampling is performed using two filters: a 43rd order FIR filter and a third order FIR filter.



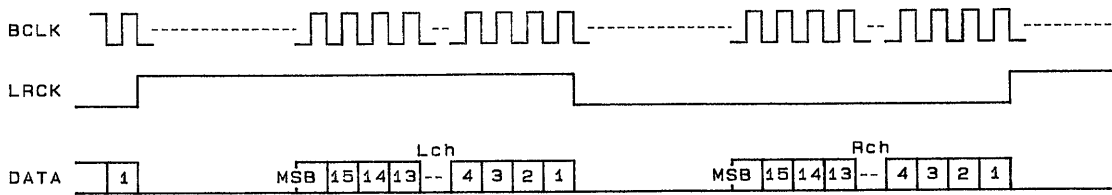
2. 1-Bit D/A Converter Block

The 1-bit D/A converter block takes the 8 Fs data input and outputs it as a 384 Fs 1-bit data series.



Input Settings

1. Input data format

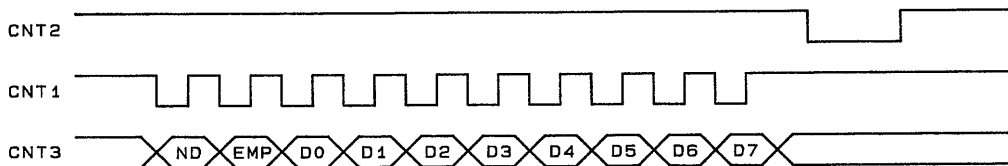


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2. Mode setting

• Serial input mode (MODE = low)

Attenuation data, de-emphasis on/off and the standard speed/double speed settings are input to the three lines CNT1, CNT2 and CNT3.



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• Parallel input mode (MODE = high)

CNT1 functions as emphasis on/off.  
 CNT2 functions as the standard/double speed switch.  
 CNT3 functions as the soft muting on/off switch.

— Standard speed/double speed settings

Mode	Input signal	Low	High
Serial input mode	ND	Standard speed	Double speed
Parallel input mode	CNT2	Standard speed	Double speed

— De-emphasis settings

Mode	Input signal	Low	High
Serial input mode	EMP	Off	On
Parallel input mode	CNT1	Off	On

De-emphasis supports an Fs of 44.1 kHz.

— Attenuation data settings (serial input mode)

When D7 is low: Bits D0 to D6 are input as attenuation data.

When D7 is high: Bits D0 to D6 are not input and no attenuation data transformation is performed.

The table below shows the relationship between the attenuation data and the output.

Attenuation data	Audio output (dB)
7F (HEX)	0
7E (HEX)	-0.137
.	.
.	.
01 (HEX)	-42.144
00 (HEX)	$-\infty$

The attenuation for the values 01 to 7E (hexadecimal) is given by the following formula.

$$\text{Attenuation} = 20 \cdot \log(\text{input data}/128) \text{ (dB)}$$

The digital attenuation interval shifts with a slope of  $1024/F_s$  (s) from 0 to  $-\infty$  (dB). If new data is input during a transition, the value begins to change towards the new value at that time.

— Soft muting switch (parallel input mode)

Soft muting can be applied by switching the value input to pin CNT3.

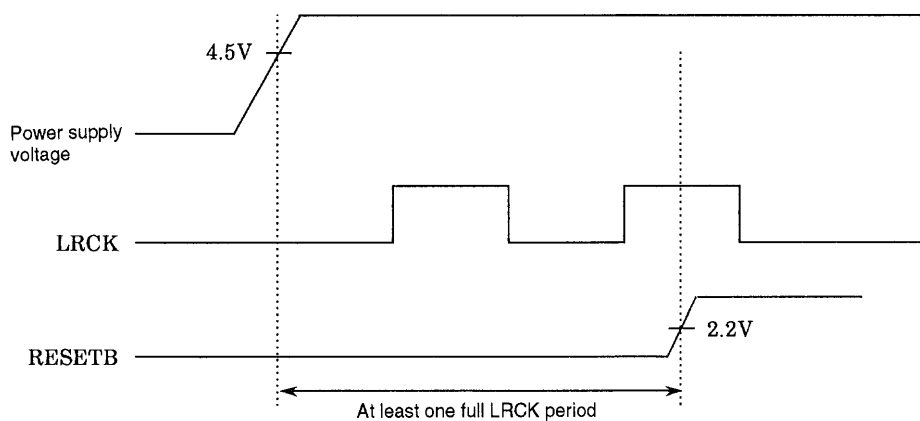
When CNT3 is high, soft muting will be applied.

Soft muting shifts the amplitude from 0 to  $-\infty$  (dB) at  $1024/F_s$  (s).

3. Initialization

The LC78855KM requires initialization when power is first applied and when the system clock is switched. A reset can be effected by setting the RESETB pin to the low level. The time that low level is held must be at least the time necessary for the power supply voltage to stabilize, the XIN, BCLK and LRCK signals to be applied and for LRCK to complete at least one cycle as shown in the figure below.

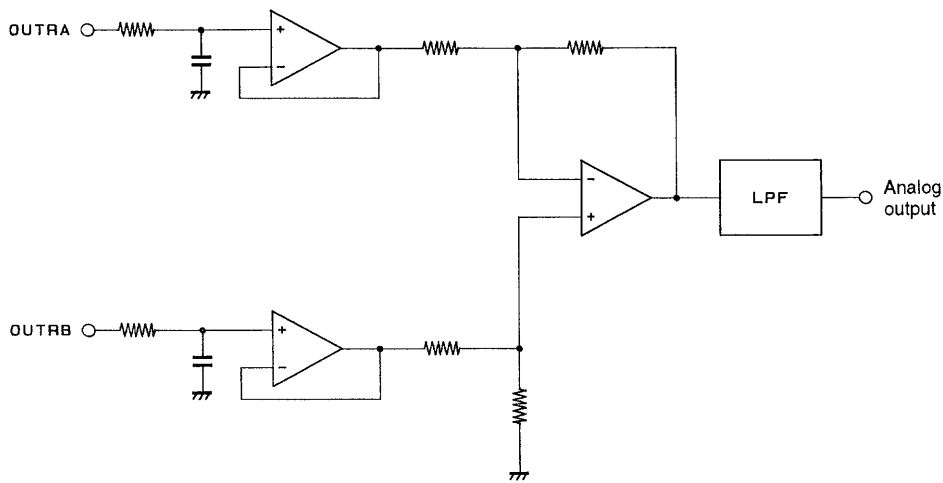
When RESETB is low, all digital outputs and the internal noise shaper go to zero and the D/A converter outputs an analog zero.



**LC78855KM Outputs**

1. CLKOUT  
This pin outputs a clock with the same frequency as the signal input to XIN.
2. MUTELO, MUTERO  
These signals output a high level if the attenuation coefficient goes to zero or if the data in each channel has been zero for  $2^{13}$  or more times in a row.
3. OUTLA, OUTLB, OUTRA, OUTRB  
The LC78855KM data output is output from these four pins in synchronization with the XIN clock. High precision analog signals can be acquired by passing these outputs through differential amplifiers and a low-pass filter. The figure below shows the details of this circuit structure.

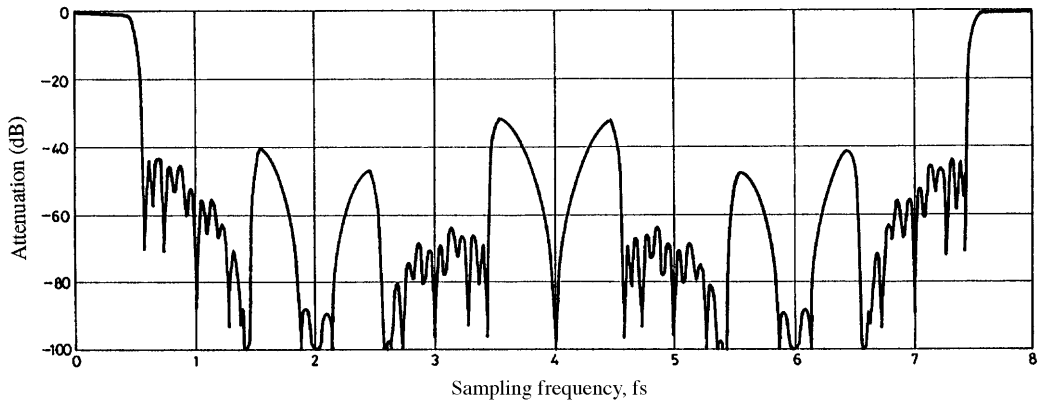
**Sample Output Block Structure**



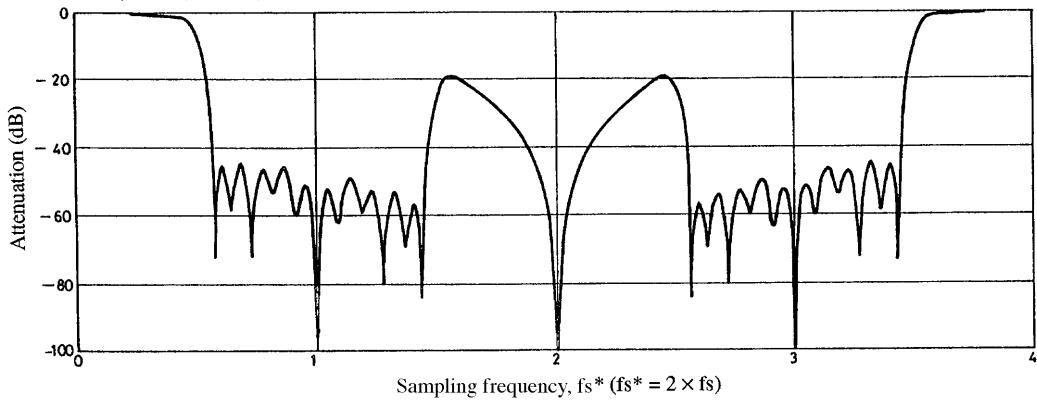
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Filter Characteristics

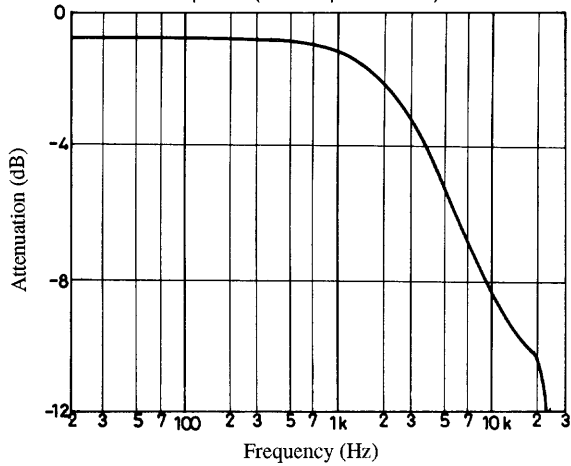
Standard speed (de-emphasis off)



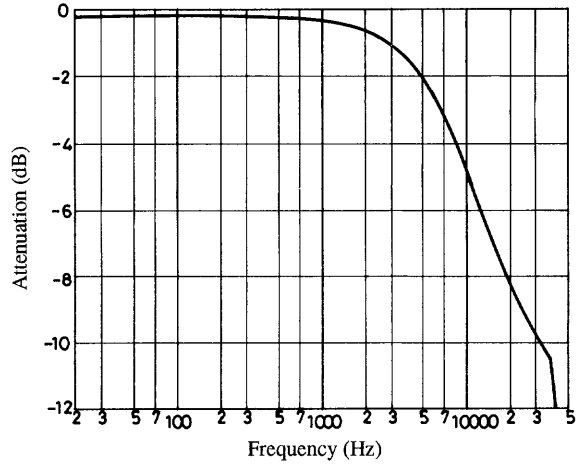
Double speed (de-emphasis off)



Standard speed (de-emphasis on)

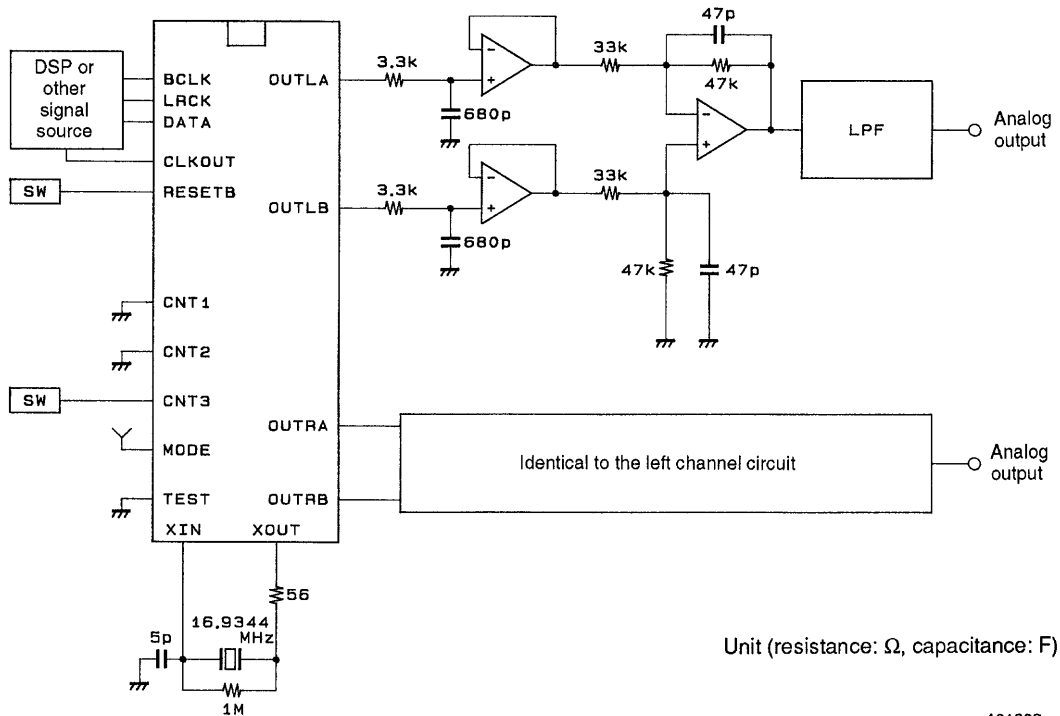


Double speed (de-emphasis on)





Sample Application Circuit



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