Ordering number : ENN*6696

CMOS IC

# LC863364/56/48/40A

## 8-Bit Single Chip Microcontroller

**Preliminary**

## Overview

The LC863364/56/48/40A are 8-bit single chip microcontrollers with the following on-chip functional blocks:

- CPU : Operable at a minimum bus cycle time of 0.424μs
- On-chip ROM capacity
  - Program ROM : 64K/56K/48K/40K bytes
  - CGROM : 16K bytes
- On-chip RAM capacity : 640 bytes
- OSD RAM : 352 × 9 bits
- Five channels × 8-bit AD Converter
- Three channels × 7-bit PWM
- Two 16-bit timer/counters, 14-bit base timer
- 8-bit synchronous serial interface circuit
- IIC-bus compliant serial interface circuit (Multi-master type)
- ROM correction function
- 15-source 9-vectored interrupt system
- Integrated system clock generator and display clock generator
  - X'tal oscillator (32.768kHz) for PLL reference is used for TV control.

All of the above functions are fabricated on a single chip


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## Features

(1) Read-Only Memory (ROM) : 65024 × 8 bits / 57344 × 8 bits / 49152 × 8 bits
40960 × 8 bits for program
16128 × 8 bits for CGROM

(2) Random Access Memory (RAM) : 640 × 8 bits (including 128 bytes for ROM correction function)
352 × 9 bits (for CRT display)

(3) OSD functions
- Screen display : 36 characters × 16 lines (by software)
- RAM : 352 words (9 bits per word)
  - Display area : 36 words × 8 lines
  - Control area : 8 words × 8 lines
- Characters
  - Up to 252 kinds of 16 × 32 dot character fonts
    (4 characters including 1 test character are not programmable)
  - Each font can be divided into two parts and used as two fonts :
    a 16 × 17 dot and 8 × 9 dot character font
- Various character attributes
  - Character colors : 16 colors
  - Character background colors : 16 colors
  - Fringe / shadow colors : 16 colors
  - Full screen colors : 16colors
  - Rounding
  - Underline
  - Italic character (slanting)
- Attribute can be changed without spacing
- Vertical display start line number can be set for each row independently (Rows can be overlapped)
- Horizontal display start position can be set for each row independently
- Horizontal pitch (bit 9 - 16)[*1] and vertical pitch (bit-32) can be set for each row independently
- Different display modes can be set for each row independently
  - Caption • Text mode / OSD mode 1 / OSD mode 2 (Quarter size) / Simplifed graphic mode
- Ten character sizes [*1]
  - Horez. × Vert. = (1 × 1), (1 × 2), (2 × 2), (2 × 4), (0.5 × 0.5)
    (1.5 × 1), (1.5 × 2), (3 × 2), (3 × 4), (0.75 × 0.5)
- Shuttering and scrolling on each row
- Simplified Graphic Display

*1 Note : range depends on display mode : refer to the manual for details.

(4) Bus Cycle Time / Instruction-Cycle Time

| Bus cycle time | Instruction cycle time | System clock oscillation | Oscillation Frequency | Voltage |
|---|---|---|---|---|
| 0.424μs | 0.848μs | Internal VCO<br>(Ref : X'tal 32.768kHz) | 14.156MHz | 4.5V to 5.5V |
| 7.5μs | 15.0μs | Internal RC | 800kHz | 4.5V to 5.5V |
| 183.1μs | 366.2μs | Crystal | 32.768kHz | 4.5V to 5.5V |

(5) Ports
- Input / Output Ports : 5 ports (28 terminals)
  Data direction programmable in nibble units : 1 port (8 terminals)

(If the N-ch open drain output is selected by option, the corresponding port data can be read in output mode.)
  Data direction programmable for each bit individually : 4 ports (20 terminals)
- Input port : 1 port (1 terminal)

(6) AD converter
- 5 channels × 8-bit AD converters

(7) Serial interfaces
- IIC-bus compliant serial interface (Multi-master type)
  Consists of a single built-in circuit with two I/O channels. The two data lines and two clock lines can be connected internally.
- Synchronous 8-bit serial interface

(8) PWM output
- 3 channels × 7-bit PWM

(9) Timer
- Timer 0 : 16-bit timer/counter
  With 2-bit prescaler + 8-bit programmable prescaler
  Mode 0 : Two 8-bit timers with a programmable prescaler
  Mode 1 : 8-bit timer with a programmable prescaler + 8-bit counter
  Mode 2 : 16-bit timer with a programmable prescaler
  Mode 3 : 16-bit counter
  The resolution of timer is 1 tCYC.
- Timer 1 : 16-bit timer/PWM
  Mode 0 : Two 8-bit timers
  Mode 1 : 8-bit timer + 8-bit PWM
  Mode 2 : 16-bit timer
  Mode 3 : Variable bit PWM (9 to 16 bits)
  In mode0/1,the resolution of Timer1/PWM is 1 tCYC
  In mode2/3,the resolution is selectable by program; tCYC or 1/2 tCYC
- Base timer
  Generate every 500ms overflow for a clock application (using 32.768kHz crystal oscillation for the base timer clock)
  Generate every 976μs, 3.9ms, 15.6ms, 62.5ms overflow (using 32.768kHz crystal oscillation for the base timer clock)
  Clock for the base timer is selectable from 32.768kHz crystal oscillation, system clock or programmable prescaler output of Timer 0

(10) Remote control receiver circuit (connected to the P73/INT3/T0IN terminal)
- Noise rejection function
- Polarity switching

(11) Watchdog timer
External RC circuit is required
Interrupt or system reset is activated when the timer overflows

(12) ROM correction function
Max 128 bytes / 2 addresses

(13) Interrupts
- 15 sources 9 vectored interrupts
  1. External Interrupt INT0
  2. External Interrupt INT1
  3. External Interrupt INT2, Timer/counter T0L (Lower 8 bits)
  4. External Interrupt INT3, base timer
  5. Timer/counter T0H (Upper 8 bits)
  6. Timer T1H,T1L
  7. SIO0
  8. Vertical synchronous signal interrupt ( $\overline{VS}$ ), horizontal line ( $\overline{HS}$ ), AD
  9. IIC, Port 0

- Interrupt priority control

  Three interrupt priorities are supported (low, high and highest) and multi-level nesting is possible. Low or high priority can be assigned to the interrupts from 3 to 9 listed above. For the external interrupt INT0 and INT1, high or highest priority can be set.

(14) Sub-routine stack level
- A maximum of 128 levels (stack is built in the internal RAM)

(15) Multiplication/division instruction
- 16 bits × 8 bits (7 instruction cycle times)
- 16 bits / 8 bits (7 instruction cycle times)

(16) 3 oscillation circuits
- Built-in RC oscillation circuit used for the system clock
- Built-in VCO circuit used for the system clock and OSD
- X'tal oscillation circuit used for base timer, system clock and PLL reference

(17) Standby function
- HALT mode

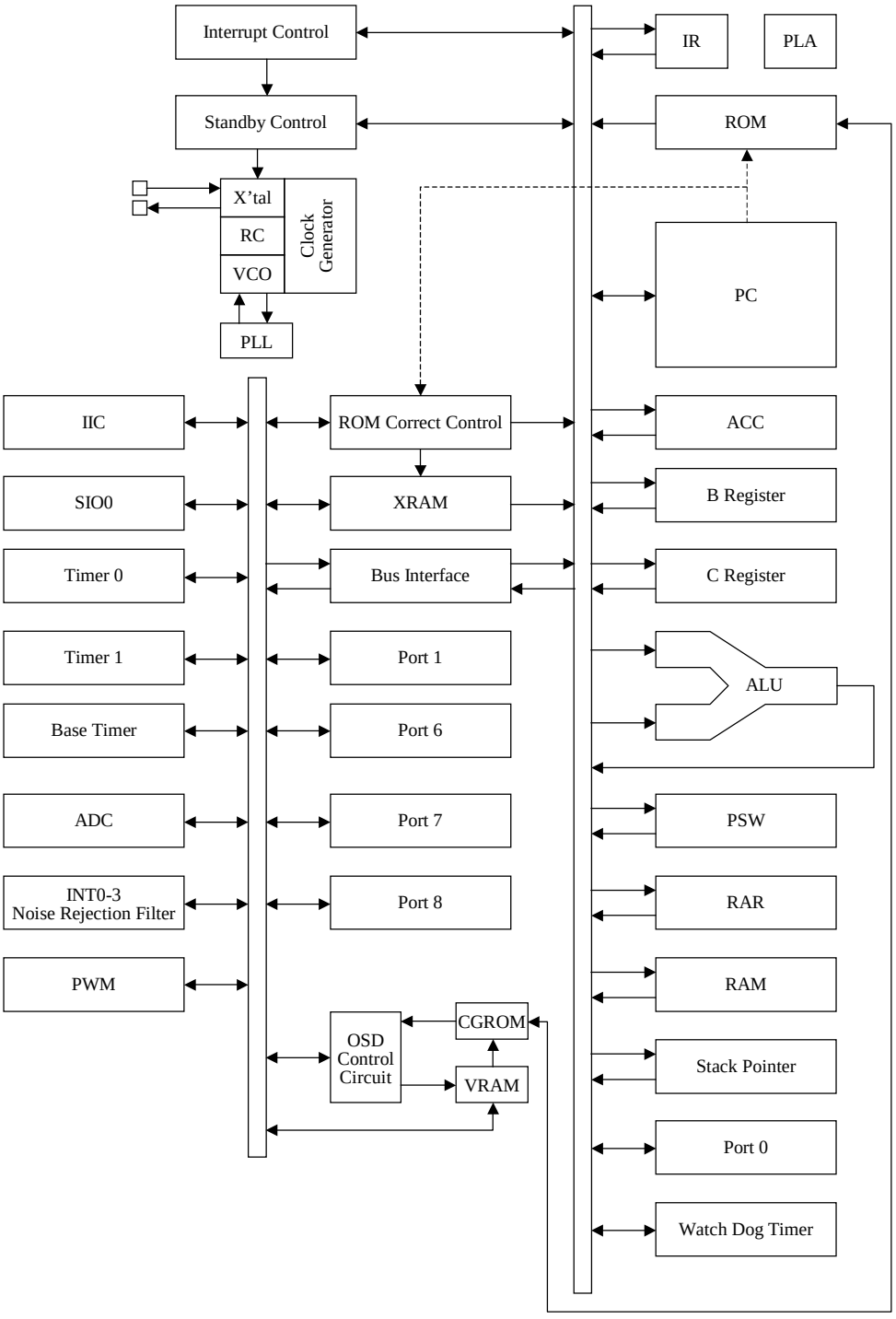
  The HALT mode is used to reduce the power dissipation. In this operation mode, the program execution is stopped. This mode can be released by the interrupt request or the system reset.
- HOLD mode

  The HOLD mode is used to stop the oscillations; RC (internal), VCO, and X'tal oscillations. This mode can be released by the following conditions.
  - Pull the reset terminal ( $\overline{\text{RES}}$ ) to low level.
  - Feed the selected level to either P70/INT0 or P71/INT1.
  - Input the interrupt condition to Port 0.

(18) Package
- DIP42S
- QIP48E

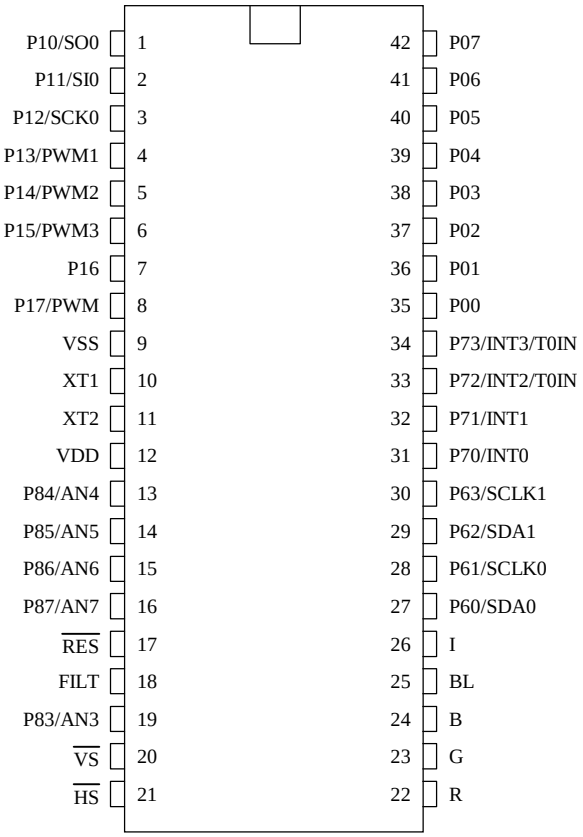
(19) Development tools
- Flash EEPROM: 2 Flash microcontrollers are available:LC86F3364A,LC86F3348A. Flash version is different on which microcontroller is used.
  LC86F3364A (LC863364A / LC863356A) (under development)
  LC86F3348A (LC863348A / LC863340A)
- Evaluation chip: LC863096
- Emulator: EVA86000 (main) + ECB863200 (evaluation chip board)
  + POD863300 (pod: DIP42S) or POD863301 (QIP48E)

## System Block Diagram



## Pin Assignment

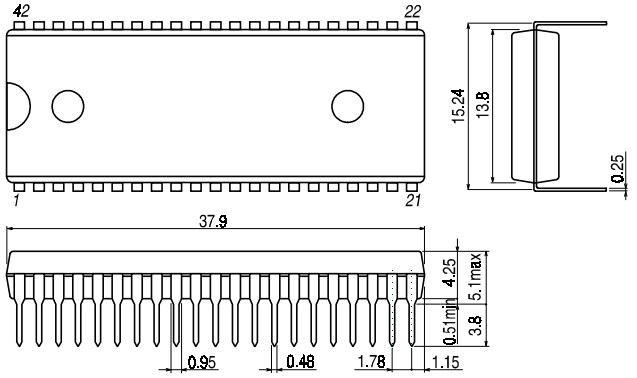
• DIP42S




### Package Dimension

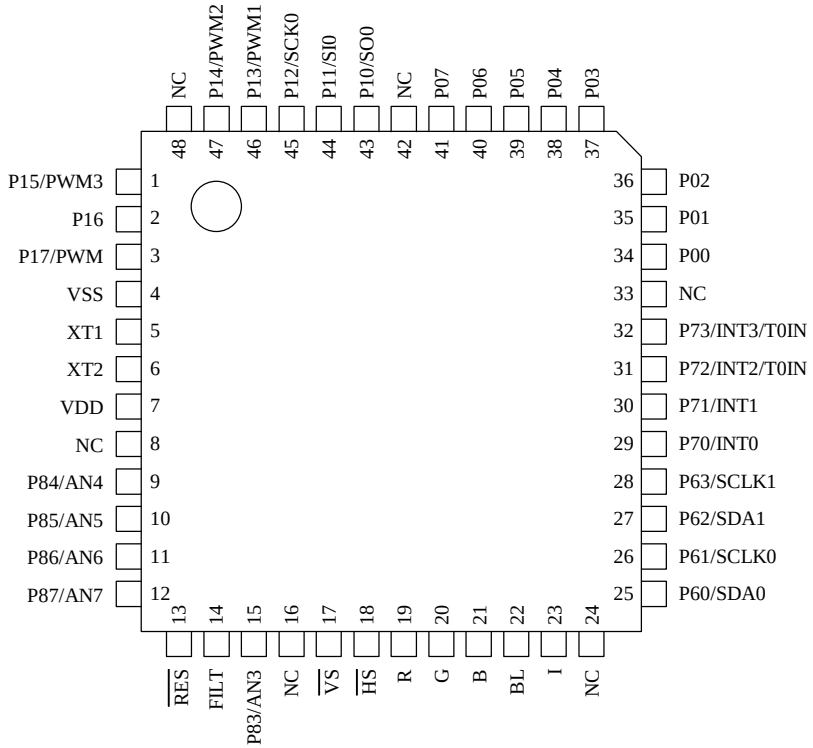
(unit : mm)

3025B




SANYO : DIP-42S(600mil)

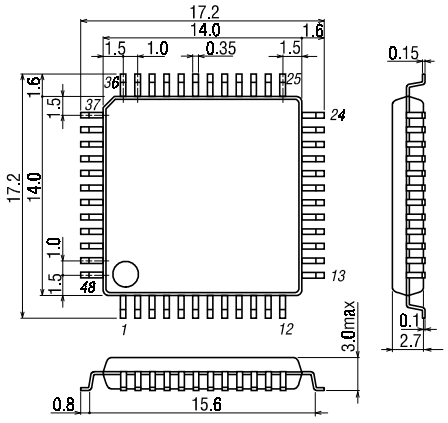
• QIP48E




### Package Dimension

(unit : mm)

3156




SANYO : QIP-48E

## Pin Description

Pin Description Table

| Terminal | I/O | Function Description | Option |
|---|---|---|---|
| VSS | - | Negative power supply | |
| XT1 | I | Input terminal for crystal oscillator | |
| XT2 | O | Output terminal for crystal oscillator | |
| VDD | - | Positive power supply | |
| $\overline{RES}$ | I | Reset terminal | |
| FILT | O | Filter terminal for PLL | |
| $\overline{VS}$ | I | Vertical synchronization signal input terminal | |
| $\overline{HS}$ | I | Horizontal synchronization signal input terminal | |
| R | O | Red (R) output terminal of RGB image output | |
| G | O | Green (G) output terminal of RGB image output | |
| B | O | Blue (B) output terminal of RGB image output | |
| I | O | Intensity ( I ) output terminal of RGB image output | |
| BL | O | Fast blanking control signal<br>Switch TV image signal and OSD image signal | |
| Port 0<br>P00 - P07 | I/O | •8-bit input/output port,<br>Input/output can be specified in nibble unit<br>•Other functions<br>HOLD release input<br>Interrupt input | Pull-up resistor provided/not provided<br>Output Format CMOS/Nch-OD |
| Port 1<br>P10 - P17 | I/O | •8-bit input/output port<br>Input/output can be specified in a bit<br>•Other functions<br>P10: SIO0 data output<br>P11: SIO0 data input/bus input/output<br>P12: SIO0 clock input/output<br>P13: PWM1 output<br>P14: PWM2 output<br>P15: PWM3 output<br>P17: Timer1 (PWM) output | Output Format CMOS/Nch-OD |
| Port 6<br>P60 - P63 | I/O | •4-bit input/output port<br>Input/output can be specified for each bit<br>•Other functions<br>P60: IIC0 data I/O<br>P61: IIC0 clock output<br>P62: IIC1 data I/O<br>P63: IIC1 clock output | |

<table>
<tr><th>Terminal</th><th>I/O</th><th>Function Description</th><th>Option</th></tr>
<tr><td>Port 7<br>P70<br>P71 - P73</td><td>I/O</td><td>•4-bit input/output port<br>Input or output can be specified for each bit<br>•Other function<br>
<table>
<tr><td>P70</td><td>INT0 input/HOLD release input/<br>Nch-Tr. output for wachdog timer</td></tr>
<tr><td>P71</td><td>INT1 input/HOLD release input</td></tr>
<tr><td>P72</td><td>INT2 input/Timer 0 event input</td></tr>
<tr><td>P73</td><td>INT3 input (noise rejection filter connected)/<br>Timer 0 event input</td></tr>
</table>
Interrupt receiver format, vector addresses
<table>
<tr><th></th><th>rising</th><th>falling</th><th>rising/<br>falling</th><th>H level</th><th>L level</th><th>vector</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>03H</td></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>0BH</td></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>13H</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>1BH</td></tr>
</table></td><td></td></tr>
<tr><td>Port 8<br>P83<br>P84-P87</td><td>I<br>I/O</td><td>•1-bit input port<br>4-bit input/output port<br>Input or output can be specified for each bit<br>•Other function<br>AD converter input port (5 lines)</td><td></td></tr>
<tr><td>NC</td><td>-</td><td>unused terminal<br>Leave open</td><td></td></tr>
</table>

- Output form and existance of pull-up resistor for all ports can be specified for each bit.
- Programmable pull-up resistor is always connected regardless of port option, CMOS or N-ch open drain output in port 1.

- Port status in reset

| Terminal | I/O | Pull-up resistor status at selecting pull-up option |
|---|---|---|
| Port 0 | I | Pull-up resistor OFF, ON after reset release |
| Port 1 | I | Programmable pull-up resistor OFF |

1. Absolute Maximum Ratings at VSS=0V and Ta=25°C

| Parameter | | Symbol | Pins | Conditions | | Ratings | | | unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | VDD[V] | min. | typ. | max. | |
| Supply voltage | | VDDMAX | VDD | | | -0.3 | | +7.0 | V |
| Input voltage | | VI(1) | • $\overline{RES}$, $\overline{HS}$, $\overline{VS}$, CVIN | | | -0.3 | | VDD+0.3 | |
| Output voltage | | VO(1) | R, G, B, I, BL, FILT | | | -0.3 | | VDD+0.3 | |
| Input/output voltage | | VIO | •Ports 0, 1, 6, 7, 8 | | | -0.3 | | VDD+0.3 | |
| High level output current | Peak output current | IOPH(1) | •Ports 0, 1, 7, 8 | •CMOS output<br>•For each pin. | | -4 | | | mA |
| | | IOPH(2) | R, G, B, I, BL | •CMOS output<br>•For each pin. | | -5 | | | |
| | Total output current | ∑IOAH(1) | •Ports 0, 1 | Total of all pins. | | -20 | | | |
| | | ∑IOAH(2) | Ports 7, 8 | Total of all pins. | | -10 | | | |
| | | ∑IOAH(3) | R, G, B, I, BL | Total of all pins. | | -15 | | | |
| Low level output current | Peak output current | IOPL(1) | Ports 0, 1, 6, 8 | For each pin. | | | | 20 | |
| | | IOPL(2) | Port 7 | For each pin. | | | | 15 | |
| | | IOPL(3) | R, G, B, I, BL | For each pin. | | | | 5 | |
| | Total output current | ∑IOAL(1) | Ports 0, 1 | Total of all pins. | | | | 40 | |
| | | ∑IOAL(2) | Ports 6, 7, 8 | Total of all pins. | | | | 40 | |
| | | ∑IOAL(3) | R, G, B, I, BL | Total of all pins. | | | | 15 | |
| Maximum power dissipation | | Pdmax | DIP42S | Ta=-10 to +70°C | | | | 800 | mW |
| | | | QIP48E | | | | | 400 | |
| Operating temperature range | | Topr | | | | -10 | | +70 | °C |
| Storage temperature range | | Tstg | | | | -55 | | +125 | |

2. Recommended Operating Range at Ta=-10°C to +70°C, VSS=0V

| Parameter | Symbol | Pins | Conditions | | Ratings | | | unit |
|---|---|---|---|---|---|---|---|---|
| | | | | VDD[V] | min. | typ. | max. | |
| Operating supply voltage range | VDD(1) | VDD | 0.844μs ≤ tCYC ≤ 0.852μs | | 4.5 | | 5.5 | V |
| | VDD(2) | | 4μs ≤ tCYC ≤ 400μs | | 4.5 | | 5.5 | |
| Hold voltage | VHD | VDD | RAMs and the registers data are kept in HOLD mode. | | 2.0 | | 5.5 | |
| High level input voltage | VIH(1) | Port 0 (Schumitt) | Output disable | 4.5 - 5.5 | 0.6VDD | | VDD | |
| | VIH(2) | •Ports 1,6 (Schumitt)<br>•Port 7 (Schumitt) port input/interrupt<br>• $\overline{HS}$ , $\overline{VS}$ , $\overline{RES}$ (Schumitt) | Output disable | 4.5 - 5.5 | 0.75VDD | | VDD | |
| | VIH(3) | Port 70 Watchdog timer input | Output disable | 4.5 - 5.5 | VDD-0.5 | | VDD | |
| | VIH(4) | •Port 8 port input | Output disable | 4.5 - 5.5 | 0.7VDD | | VDD | |
| Low level input voltage | VIL(1) | Port 0 (Schumitt) | Output disable | 4.5 - 5.5 | VSS | | 0.2VDD | |
| | VIL(2) | •Ports 1,6 (Schumitt)<br>•Port 7 (Schumitt) port input/interrupt<br>• $\overline{HS}$ , $\overline{VS}$ , $\overline{RES}$ (Schumitt) | Output disable | 4.5 - 5.5 | VSS | | 0.25VDD | |
| | VIL(3) | Port 70 Watchdog timer input | Output disable | 4.5 - 5.5 | VSS | | 0.6VDD | |
| | VIL(4) | Port 8 port input | Output disable | 4.5 - 5.5 | VSS | | 0.3VDD | |
| CVIN | VCVIN | CVIN | | 5.0 | 1Vp-p -3dB | 1Vp-p | 1Vp-p +3dB | Vp-p * |
| Operation cycle time | tCYC(1) | | •All functions operating | 4.5 - 5.5 | 0.844 | 0.848 | 0.852 | μs |
| | tCYC(2) | | •AD converter operating<br>•OSD and Data slicer are not operating | 4.5 - 5.5 | 0.844 | | 30 | |
| | tCYC(3) | | •OSD, AD converter and Data slicer are not operating | 4.5 - 5.5 | 0.844 | | 400 | |
| Oscillation frequency range | FmRC | | Internal RC oscillation | 4.5 - 5.5 | 0.4 | 0.8 | 3.0 | MHz |

* Vp-p : Peak-to-peak voltage

3. Electrical Characteristics at Ta=-10°C to +70°C, VSS=0V

| Parameter | Symbol | Pins | Conditions | | Ratings | | | unit |
|---|---|---|---|---|---|---|---|---|
| | | | | VDD[V] | min. | typ. | max. | |
| High level input current | IIH(1) | Ports 0, 1, 6, 7, 8 | •Output disable<br>•Pull-up MOS Tr. OFF<br>•VIN=VDD (including the off-leak current of the output Tr.) | 4.5 - 5.5 | | | 1 | μA |
| | IIH(2) | • $\overline{RES}$<br>• $\overline{HS}$ , $\overline{VS}$ | •VIN=VDD | 4.5 - 5.5 | | | 1 | |
| Low level input current | IIL(1) | Ports 0, 1, 6, 7, 8 | •Output disable<br>•Pull-up MOS Tr. OFF<br>•VIN=VSS (including the off-leak current of the output Tr.) | 4.5 - 5.5 | -1 | | | |
| | IIL(2) | • $\overline{RES}$<br>• $\overline{HS}$ , $\overline{VS}$ | VIN=VSS | 4.5 - 5.5 | -1 | | | |
| High level output voltage | VOH(1) | •CMOS output of ports 0,1,71-73,8 | IOH=-1.0mA | 4.5 - 5.5 | VDD-1 | | | V |
| | VOH(2) | R, G, B, I, BL | IOH=-0.1mA | 4.5 - 5.5 | VDD-0.5 | | | |
| Low level output voltage | VOL(1) | Ports 0,1,71-73,8 | IOL=10mA | 4.5 - 5.5 | | | 1.5 | |
| | VOL(2) | Ports 0,1,71-73,8 | IOL=1.6mA | 4.5 - 5.5 | | | 0.4 | |
| | VOL(3) | •R, G, B, I, BL<br>•Port 6 | IOL=3.0mA | 4.5 - 5.5 | | | 0.4 | |
| | VOL(4) | Port 6 | IOL=6.0mA | 4.5 - 5.5 | | | 0.6 | |
| | VOL(5) | Port 70 | IOL=1mA | 4.5 - 5.5 | | | 0.4 | |
| Pull-up MOS Tr. resistance | Rpu | •Ports 0, 1, 7, 8 | VOH=0.9VDD | 4.5 - 5.5 | 13 | 38 | 80 | kΩ |
| Bus terminal short circuit resistance (SCL0-SCL1, SDA0-SDA1) | RBS | •P60-P62<br>•P61-P63 | | 4.5 - 5.5 | | | 130 | Ω |
| Hysteresis voltage | VHIS | •Ports 0, 1, 6, 7<br>• $\overline{RES}$<br>• $\overline{HS}$ , $\overline{VS}$ | Output disable | 4.5 - 5.5 | | 0.1VDD | | V |
| Input clump votage | VCLMP | CVIN | | 5.0 | 2.3 | 2.5 | 2.7 | |
| Pin capacitance | CP | All pins | •f=1MHz<br>•Every other terminals are connected to VSS.<br>•Ta=25°C | 4.5 - 5.5 | | 10 | | pF |

4. Serial Input/Output Characteristics at Ta=-10°C to +70°C, VSS=0V

| Parameter | | | Symbol | Pins | Conditions | Ratings | | | | unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | VDD[V] | min. | typ. | max. | |
| Serial clock | Input clock | Cycle | tCKCY(1) | •SCK0<br>•SCLK0 | Refer to figure 4. | 4.5 - 5.5 | 2 | | | tCYC |
| | | Low Level pulse width | tCKL(1) | | | | 1 | | | |
| | | High Level pulse width | tCKH(1) | | | | 1 | | | |
| | Output clock | Cycle | tCKCY(2) | •SCK0<br>•SCLK0 | •Use pull-up resistor (1kΩ) when Nch open-drain output.<br>•Refer to figure 4. | 4.5 - 5.5 | 2 | | | |
| | | Low Level pulse width | tCKL(2) | | | | | 1/2tCKCY | | |
| | | High Level pulse width | tCKH(2) | | | | | 1/2tCKCY | | |
| Serial input | Data set up time | | tICK | SI0 | •Data set-up to SCK0.<br>•Data hold from SCK0.<br>•Refer to figure 4. | 4.5 - 5.5 | 0.1 | | | µs |
| | Data hold time | | tCKI | | | | 0.1 | | | |
| Serial output | Output delay time (Using external clock) | | tCKO(1) | SO0 | •Data hold from SCK0.<br>•Use pull-up resistor (1kΩ) when Nch open-drain output.<br>•Refer to figure 4. | 4.5 - 5.5 | | | 7/12tCYC +0.2 | |
| | Output delay time (Using internal clock) | | tCKO(2) | SO0 | | 4.5 - 5.5 | | | 1/3tCYC +0.2 | |

5. IIC Input/Output Conditions at Ta=-10°C to +70°C, VSS=0V

| Parameter | Symbol | Standard | | High speed | | unit |
|---|---|---|---|---|---|---|
| | | min. | max. | min. | max. | |
| SCL Frequency | fSCL | 0 | 100 | 0 | 400 | kHz |
| BUS free time between stop - start | tBUF | 4.7 | - | 1.3 | - | µs |
| HOLD time of start, restart condition | tHD;STA | 4.0 | - | 0.6 | - | µs |
| L time of SCL | tLOW | 4.7 | - | 1.3 | - | µs |
| H time of SCL | tHIGH | 4.0 | - | 0.6 | - | µs |
| Set-up time of restart condition | tSU;STA | 4.7 | - | 0.6 | - | µs |
| HOLD time of SDA | tHD;DAT | 0 | - | 0 | 0.9 | µs |
| Set-up time of SDA | tSU;DAT | 250 | - | 100 | - | ns |
| Rising time of SDA, SCL | tR | - | 1000 | 20+0.1Cb | 300 | ns |
| Falling time of SDA, SCL | tF | - | 300 | 20+0.1Cb | 300 | ns |
| Set-up time of stop condition | tSU;STO | 4.0 | - | 0.6 | - | µs |

Refer to figure 10

(Note) Cb : Total capacitance of all BUS (unit : pF)

6. Pulse Input Conditions at Ta=-10°C to +70°C, VSS=0V

| Parameter | Symbol | Pins | Conditions | VDD[V] | Ratings min. | Ratings typ. | Ratings max. | unit |
|---|---|---|---|---|---|---|---|---|
| High/low level pulse width | tPIH(1)<br>tPIL(1) | •INT0, INT1<br>•INT2/T0IN | •Interrupt acceptable<br>•Timer0-countable | 4.5 - 5.5 | 1 | | | tCYC |
| | tPIH(2)<br>tPIL(2) | INT3/T0IN<br>(1/1 is selected for noise rejection clock.) | •Interrupt acceptable<br>•Timer0-countable | 4.5 - 5.5 | 2 | | | |
| | tPIH(3)<br>tPIL(3) | INT3/T0IN<br>(1/16 is selected for noise rejection clock.) | •Interrupt acceptable<br>•Timer0-countable | 4.5 - 5.5 | 32 | | | |
| | tPIH(4)<br>tPIL(4) | INT3/T0IN<br>(1/64 is selected for noise rejection clock.) | •Interrupt acceptable<br>•Timer0-countable | 4.5 - 5.5 | 128 | | | |
| | tPIL(5) | $\overline{RES}$ | Reset acceptable | 4.5 - 5.5 | 200 | | | µs |
| | tPIH(6)<br>tPIL(6) | $\overline{HS}$ , $\overline{VS}$ | •Display position controllable (Note)<br>•The active edge of $\overline{HS}$ and $\overline{VS}$ must be apart at least 1 tCYC.<br>•Refer to figure 6. | 4.5 - 5.5 | 8 | | | |
| Rising/falling time | tTHL<br>tTLH | $\overline{HS}$ | Refer to figure 6. | 4.5 - 5.5 | | | 500 | ns |

7. AD Converter Characteristics at Ta=-10°C to + 70°C, VSS=0V

| Parameter | Symbol | Pins | Conditions | VDD[V] | Ratings min. | Ratings typ. | Ratings max. | unit |
|---|---|---|---|---|---|---|---|---|
| Resolution | N | | | 4.5 – 5.5 | | 8 | | bit |
| Absolute precision | ET | | (Note 3) | | | | ±1.5 | LSB |
| Conversion time | tCAD | | ADCR2=0 (Note 4) | | | 16 | | tCYC |
| | | | ADCR2=1 (Note 4) | | | 32 | | |
| Analog input voltage range | VAIN | AN4 - AN7 | | | VSS | | VDD | V |
| Analog port input current | IAINH | | VAIN=VDD | | | | 1 | µA |
| | IAINL | | VAIN=VSS | | -1 | | | |

(Note 3) Absolute precision does not include quantizing error (1/2LSB).
(Note 4) Conversion time is the time till the complete digital conversion value for analog input value is set to a register after the instruction to start conversion is sent.

8. Sample Current Dissipation Characteristics at Ta=-10°C to +70°C, VSS=0V

The sample current dissipation characteristics is the measurement result of Sanyo provided evaluation board when the recommended circuit parameters shown in the sample oscillation circuit characteristics are used externally. The currents through the output transistors and the pull-up MOS transistors are ignored.

| Parameter | Symbol | Pins | Conditions | | Ratings | | | unit |
|---|---|---|---|---|---|---|---|---|
| | | | | VDD[V] | min. | typ. | max. | |
| Current dissipation during basic operation (Note 3) | IDDOP(1) | VDD | •FmX'tal=32.768kHz X'tal oscillation<br>•System clock : VCO<br>•VCO for OSD operating<br>•Internal RC oscillation stops | 4.5 - 5.5 | | 19 | 32 | mA |
| Current dissipation in HALT mode (Note 3) | IDDHALT(1) | VDD | •HALT mode<br>•FmX'tal=32.768kHz X'tal oscillation<br>•System clock : VCO<br>•VCO for OSD stops<br>•Internal RC oscillation stops | 4.5 - 5.5 | | 7 | 12 | mA |
| | IDDHALT(2) | VDD | •HALT mode<br>•FmX'tal=32.768kHz X'tal oscillation<br>•VCO for system stops<br>•VCO for OSD stops<br>•System clock : Internal RC | 4.5 - 5.5 | | 300 | 1200 | μA |
| | IDDHALT(3) | VDD | •HALT mode<br>•FmX'tal=32.768kHz X'tal oscillation<br>•VCO for system stops<br>•VCO for OSD stops<br>•System clock : X'tal | 4.5 - 5.5 | | 50 | 200 | |
| Current dissipation in HOLD mode (Note 3) | IDDHOLD | VDD | •HOLD mode<br>•All oscillation stops. | 4.5 - 5.5 | | 0.05 | 20 | μA |

(Note 3) The currents through the output transistors and the pull-up MOS transistors are ignored.

Recommended Oscillation Circuit and Sample Characteristics

The sample oscillation circuit characteristics in the table below is based on the following conditions:

- Recommended circuit parameters are verified by an oscillator manufacturer using a Sanyo provided oscillation evaluation board.
- Sample characteristics are the result of the evaluation with the recommended circuit parameters connected externally.

Recommended oscillation circuit and sample characteristics (Ta = -10 to +70°C)

| Frequency | Manufacturer | Oscillator | Recommended circuit parameters | | | | Operating supply voltage range | Oscillation stabilizing time | | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | C1 | C2 | Rf | Rd | | typ. | max | |
| 32.768kHz | Seiko Epson | C-002RX | 18pF | 18pF | Open | 390kΩ | 4.5 – 5.5V | 1.00s | 1.50s | |

Notes The oscillation stabilizing time period is the time until the VCO oscillation for the internal system becomes stable after the following conditions. (Refer to Figure 2.)

1. The VDD becomes higher than the minimum operating voltage after the power is supplied.
2. The HOLD mode is released.

The sample oscillation circuit characteristics may differ applications. For further assistance, please contact with oscillator manufacturer with the following notes in your mind.

- Since the oscillation frequency precision is affected by wiring capacity of the application board, etc., adjust the oscillation frequency on the production board.
- The above oscillation frequency and the operating supply voltage range are based on the operating temperature of -10°C to +70°C. For the use with the temperature outside of the range herein, or in the applications requiring high reliability such as car products, please consult with oscillator manufacturer.
- When using the oscillator which is not shown in the sample oscillation circuit characteristics, please consult with Sanyo sales personnel.

Since the oscillation circuit characteristics are affected by the noise or wiring capacity because the circuit is designed with low gain in order to reduce the power dissipation, refer to the following notices.

- The distance between the clock I/O terminal (XT1 terminal XT2 terminal) and external parts should be as short as possible.
- The capacitors' VSS should be allocated close to the microcontroller's GND terminal and be away from other GND.
- The signal lines with rapid state changes or with large current should be allocated away from the oscillation circuit.

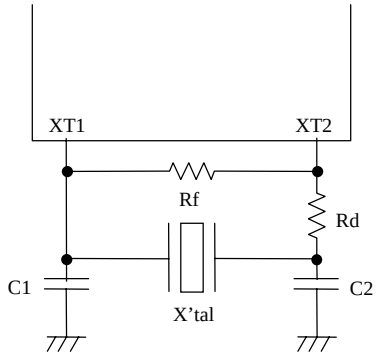



Figure 1 Recommended oscillation circuit.

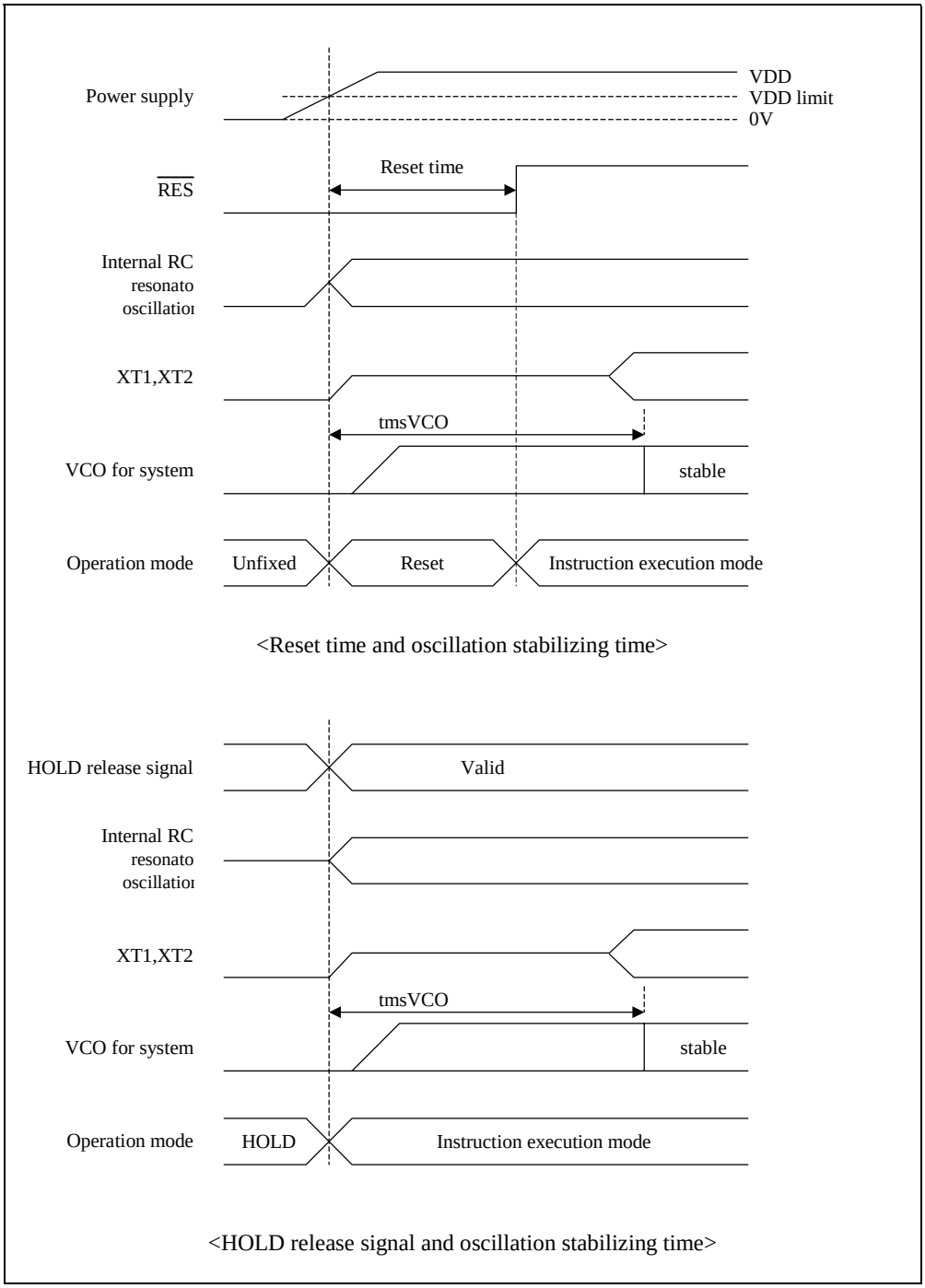
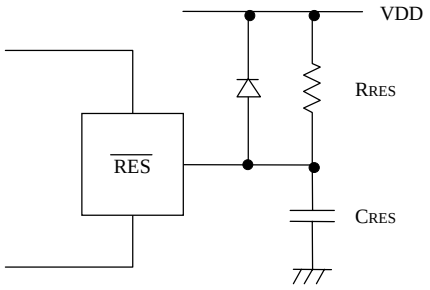


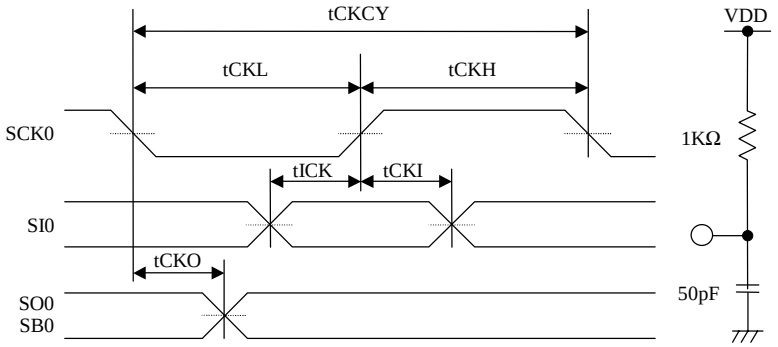

Figure 2 Oscillation stabilizing time




(Note) Determine the CRES, RRES value to generate more than 200μs reset time.

Figure 3 Reset circuit


<AC timing measurement point>




< Timing > < Test load >

Figure 4 Serial input / output test condition

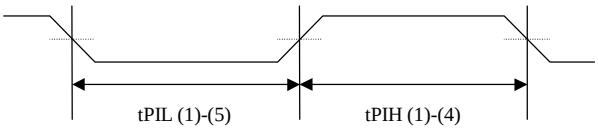



Figure 5 Pulse input timing condition – 1

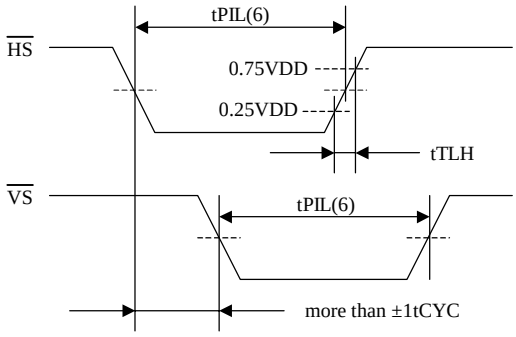



Figure 6 Pulse input timing condition - 2

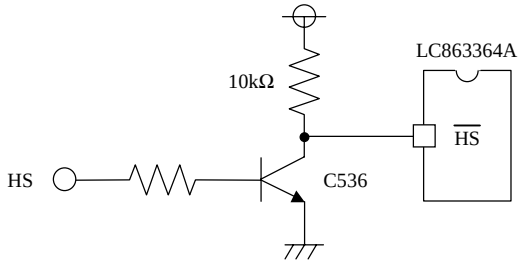
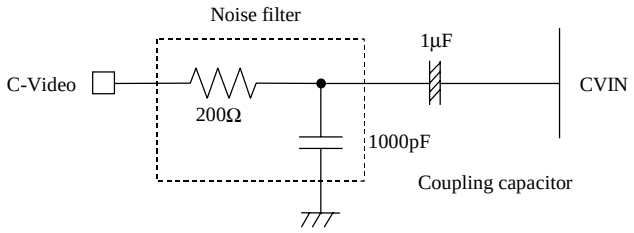



Figure 7 Recommended Interface circuit




Output impedance of C-Video before Noise filter should be less then 100Ω.

Figure 8 CVIN recommended circuit

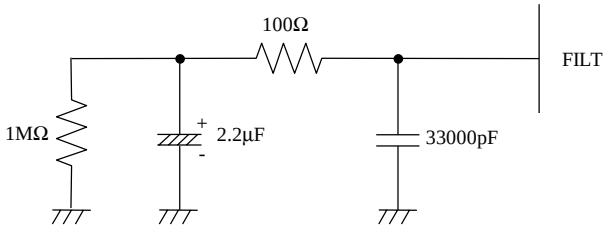
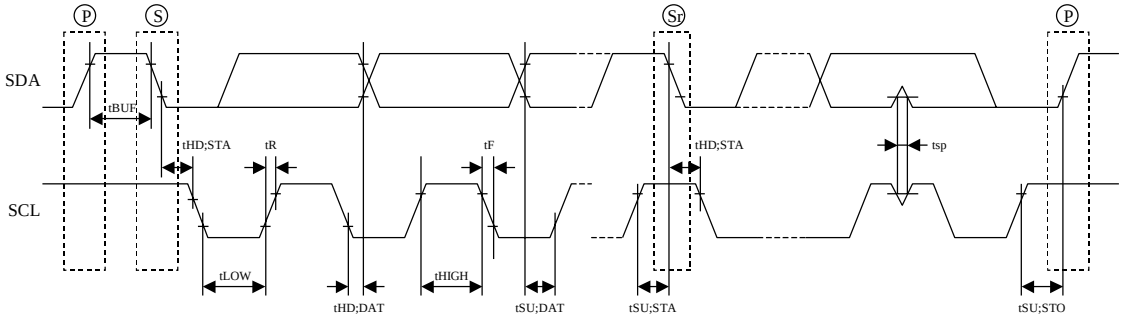



Figure 9 FILT recommended circuit

(Note) Place FILT parts on board as close to the microcontroller as possible.




S : start condition
P : stop condition
Sr : restart condition

tsp : Spike suppression

Standard mode : not exist
High speed mode : less than 50ns

Figure 10 IIC timing

memo:

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