Ordering number : ENN6237

CMOS IC

LC895198

CD-ROM Decoder for 32× ATAPI (IDE) Drives

Overview

The LC895198 is a CD-ROM decoder that supports ATAPI (IDE) and includes 1 MB of on-chip DRAM.

Functions

- CD-ROM ECC function
- Sub-code read function
- Built-in ATAPI (IDE) I/F (register and other blocks)
- CAV audio function
- Built-in DVD-ROM I/F (8-bit width)
- Built-in 1-Mbit DRAM

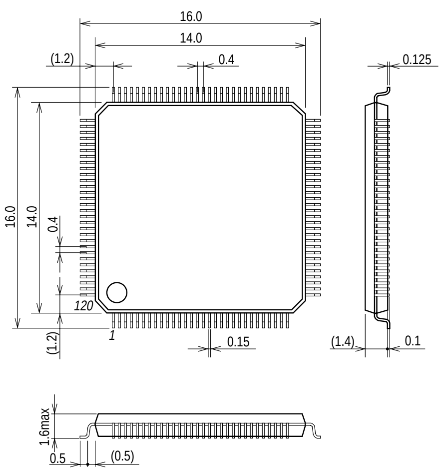
Features

- 32× speed supported
  16.6MBytes/s (with IORDY)
  Operation frequency: 33.8688 MHz
- 32× speed supported
  16.6MBytes/s (without IORDY)
  Operation frequency: 36 MHz
- CD main channel, C2 flag, and subcode areas in buffer RAM can be set freely by user
- Built-in batch transfer function (function for sending CD main channel, C2 flag, subcode, etc., at one time)
- Built-in multi transfer function (function for sending several blocks at one time)
- Built-in CAV-AUDIO function
- Built-in intelligent functions (auto buffering, auto decoding, CD-R support, etc.)
- Built-in subcode P to W buffering function (NO-ECC) and CD-TEXT support

Package Dimensions

unit: mm

3237-LQFP120



SANYO: LQFP120

Specifications

Absolute Maximum Ratings at V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	Ta = 25°C	–0.3 to +7.0	V
Input/output voltage	V_I, V_O	Ta = 25°C	–0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max	Ta ≤ 70°C	400	mW
Operating temperature	Topr		0 to +70	°C
Storage temperature	Tstg		–55 to +125	°C
Soldering temperature (pin part only)		10 s	235	°C
Input/output power	I_I, I_O	Per 1 input/output reference cell	±20	mA

SANYO Electric Co.,Ltd. Semiconductor Company
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Allowable Operating Ranges at Ta = 0 to +70°C, V_{SS} = 0 V

I_O cell 5.0 V supply voltage

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}		4.5	5.0	5.5	V
Input voltage range	V_{IN}		0		V_{DD}	V

Internal cell 3.3 V supply voltage

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}		3.0	3.3	3.6	V
Input voltage range	V_{IN}		0		V_{DD}	V

Electrical Characteristics at Ta = 0 to +70°C, V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V

Parameter	Symbol	Conditions	Applicable pins	Ratings			Unit
				min	typ	max	
Input high-level voltage	V_{IH}	TTL levels	(1)	2.2	—	—	V
Input low-level voltage	V_{IL}			—	—	0.8	V
Input high-level voltage	V_{IH}	TTL levels with pull-up resistor	(9)	2.2	—	—	V
Input low-level voltage	V_{IL}			—	—	0.8	V
Input high-level voltage	V_{IH}	TTL levels Schmitt with pull-down resistor	DRESP HDB0 to HDB7	2.2	—	—	V
Input low-level voltage	V_{IL}			—	—	0.8	V
Input high-level voltage	V_{IH}	TTL levels Schmitt	(2), (3), (10)	2.4	—	—	V
Input low-level voltage	V_{IL}			—	—	0.8	V
Output high-level voltage	V_{OH}	I_{OH} = –2 mA	(9)	V_{DD} – 2.1	—	—	V
Output low-level voltage	V_{OL}	I_{OL} = 2 mA		—	—	0.4	V
Output high-level voltage	V_{OH}	I_{OH} = –8 mA	(4)	V_{DD} – 2.1	—	—	V
Output low-level voltage	V_{OL}	I_{OL} = 8 mA		—	—	0.4	V
Output high-level voltage	V_{OH}	I_{OH} = –4 mA	(7), (10)	V_{DD} – 2.1	—	—	V
Output low-level voltage	V_{OL}	I_{OL} = 24 mA		—	—	0.4	V
Output low-level voltage	V_{OL}	I_{OL} = 24 mA	(8)	—	—	0.4	V
Output low-level voltage	V_{OL}	I_{OL} = 8 mA	(5), (6)	—	—	0.4	V
Input leak current	I_{IL}	V_I = V_{SS}, V_{DD}	(1), (2), (3), (10)	–10		+10	µA
Output leak current	I_{OZ}	During high-impedance output	(5), (7), (8), (10)	–10		+10	µA
Pull-up resistance	R_{UP}		(6), (9)	40	80	160	kΩ
Pull-down resistance	R_{DN}	DRESP, DREQ, HDB0 to HDB7		40	80	160	kΩ

The applicable pin sets are as follows.

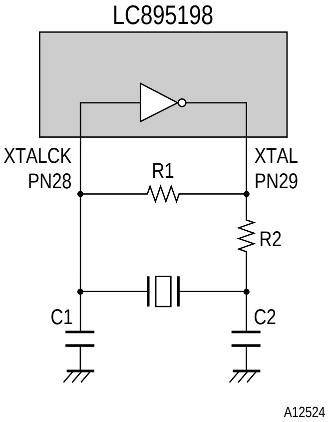
INPUT
(1) ATPINSEL, CSCTRL, SUA0 to SUA6, BCK, C2PO, LRCK, DSDATA, SBS0, SCOR, WFCK, TEST0 to TEST1, AUDIOCK
(2) ZRESET, ZCS, ZRD, ZWR, CSEL
(3) DA0 to DA2, ZCS1FX, ZCS3FX, ZDIOR, ZDIOW, ZDMACK, ZHRST

OUTPUT
(4) EXCK, DREQ, MCK, MCK3
(5) ZRSTCPU
(6) ZINT, ZINT1, ZSWAIT
(7) DMARQ, HINTRQ
(8) IORDY, ZIOCS16

INOUT
(9) D0 to D7
(10) DD0 to DD15, ZDASP, ZPDIAG

Note: Pins other than XTAL and XTALCK are not included in DC characteristics.

Recommended Oscillator Circuit Example



R1 = 1 MΩ

R2 = 15 Ω

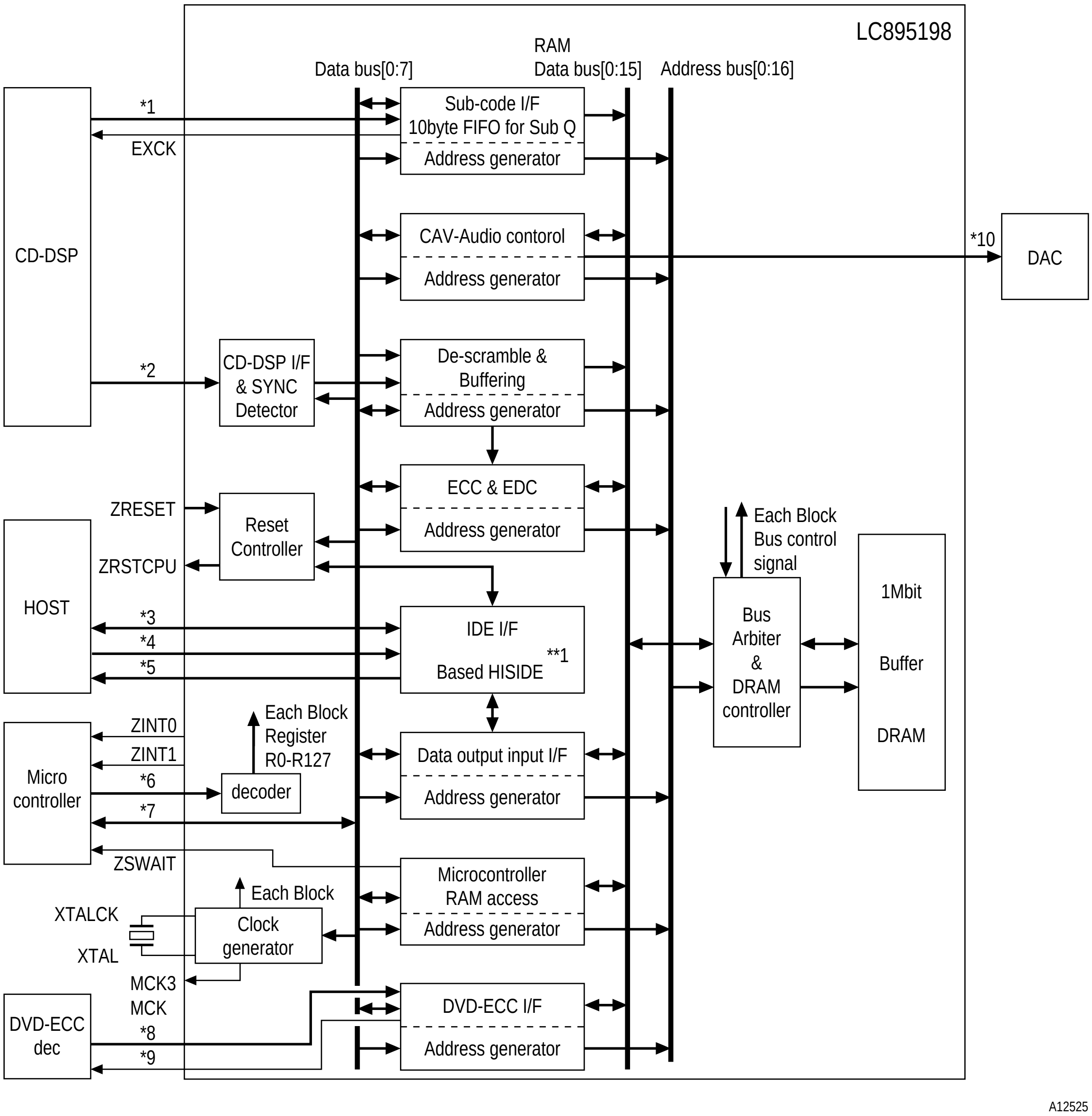
C1 = 0

C2 = 47 pF

When the ceramic clock oscillator frequency is 33.8688 MHz:
(The 33.8688 MHz in this recommended example is the third harmonic.)

The exact values of the components are influenced by the printed circuit board used. Consult with the manufacturer of the oscillator element used to determine these values.

Block Diagram



*1 WFCK, SBSO, SCOR
*2 BCK, SDATA, LRCK, C2PO
*3 DD0 to DD15, ZDASP, ZPDIAG
*4 ZCS1FX, ZCS3FX, DA0 to DA2, ZDIOR, ZDIOW, ZDMACK, CSEL
*5 DMARQ, HINTRQ, ZIOCS16, IORDY, ZHRST
*6 ZRD, ZWR, SUA0 to SUA6, ZCS, CSCTRL
*7 D0 to D7
*8 HDB0 to HDB7, DRESP
*9 DREQ
*10 DBCK, DLRCK, DSDATA
**1 HISIDE(WD25C32) is made by WESTERN DIGITAL

Pin Functions

LC895198 Pin Functions 1
(When ATPINSEL (pin 113) is 0)

Type					
I	INPUT	B	BIDIRECTION	NC	NOT CONNECT
O	OUTPUT	P	POWER		

Pin No.	Pin	Type	Function
1	V_{DD0}	P	5.0 V
2	DREQ	O	DVD ECC data request output
3	DRESP	I	DVD ECC data latch signal input
4	HDB7 (IOP0)	B	DVD ECC data I/O These pins can be switched to function as general-purpose I/O ports by register settings.
5	HDB6 (IOP1)	B	
6	HDB5 (IOP2)	B	
7	HDB4 (IOP3)	B	
8	HDB3 (IOP4)	B	
9	HDB2 (IOP5)	B	
10	HDB1 (IOP6)	B	
11	HDB0 (IOP7)	B	
12	MCK3	O	XTALCLK 1/1, 1/2, and stop output
13	V_{SS0}	P	
14	V_{DD1}	P	3.3 V
15	V_{DD0}	P	5.0 V
16	DSDATA	O	D/A converter output
17	DLRCK	O	
18	DBCK	O	
19	C2PO	I	CD DSP interface
20	SDATA	I	
21	BCK	I	
22	LRCK	I	
23	EXCK	O	Subcode I/O
24	WFCK	I	
25	SBSO	I	
26	SCOR	I	
27	MCK	O	XTALCLK 1/1, 1/2, and stop output
28	XTALCK	I	Crystal oscillator circuit input
29	XTAL	O	Crystal oscillator circuit output
30	V_{SS0}	P	
31	V_{DD1}	P	3.3 V
32	V_{DD0}	P	5.0 V
33	V_{SS0}	P	
34	CSCTRL	I	Active low/active high selection for the microcontroller CS pin
35	ZRD	I	Microcontroller data read signal input
36	ZWR	I	Microcontroller data write signal input
37	ZCS	I	Register chip select input from the microcontroller
38	SUA0	I	Microcontroller register selection signals
39	SUA1	I	
40	SUA2	I	
41	SUA3	I	
42	SUA4	I	
43	SUA5	I	
44	SUA6	I	
45	V_{DD1}	P	3.3 V
46	V_{DD0}	P	5.0 V
47	V_{SS0}	P	

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Pin No.	Pin	Type	Function
48	D0	B	Microcontroller data signals. These pins have built-in pull-up resistors.
49	D1	B	
50	D2	B	
51	D3	B	
52	D4	B	
53	D5	B	
54	D6	B	
55	D7	B	
56	ZINT0	O	Interrupt request signal output to the microcontroller
57	ZINT1	O	
58	ZSWAIT	O	WAIT signal output to the microcontroller
59	ZRSTCPU	O	CPU reset signal output
60	V_{SS0}	P	
61	V_{DD0}	P	5.0 V
62	CSEL	I	ATAPI control signals
63	ZHRST	I	
64	ZDASP	B	
65	ZCS3FX	I	
66	ZCS1FX	I	
67	V_{SS1}	P	
68	DA2	I	ATAPI control signals
69	DA0	I	
70	ZPDIAG	B	
71	DA1	I	
72	V_{SS1}	P	
73	ZIOCS16	O	ATAPI control signals
74	HINTRQ	O	
75	V_{SS1}	P	
76	V_{DD1}	P	3.3 V
77	ZDMACK	I	ATAPI control signals
78	IORDY	O	
79	V_{SS1}	P	
80	ZDIOR	I	ATAPI control signals
81	ZDIOW	I	
82	DMARQ	O	
83	DD15	B	ATAPI data bus
84	DD0	B	
85	V_{SS1}	P	
86	DD14	B	ATAPI data bus
87	DD1	B	
88	DD13	B	
89	DD2	B	
90	V_{SS1}	P	
91	V_{DD0}	P	5.0 V
92	DD12	B	ATAPI data bus
93	DD3	B	
94	DD11	B	
95	DD4	B	
96	V_{SS1}	P	
97	DD10	B	ATAPI data bus
98	DD5	B	
99	DD9	B	
100	V_{SS1}	P	

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Pin No.	Pin	Type	Function
101	DD6	B	ATAPI data bus
102	DD8	B	
103	DD7	B	
104	V_{DD1}	P	3.3 V
105	V_{DD1}	P	3.3 V
106	V_{DD0}	P	5.0 V
107	V_{DD1}	P	3.3 V
108	ZRESET	I	IC reset input
109	V_{DD1}	P	3.3 V
110	V_{SS0}	P	
111	TEST1	I	Test pin. This pin must be connected to V_{SS} in normal operation.
112	V_{SS0}	P	
113	ATPINSEL	I	ATAPI pin layout selection. This pin must be connected to V_{SS0}.
114	V_{SS0}	P	
115	TEST0	I	Test pin. This pin must be connected to V_{SS} in normal operation.
116	V_{DD0}	I	5.0 V
117	AUDIOCK	I	Clock input for the CAV audio block
118	V_{DD0}	P	5.0 V
119	V_{DD0}	P	5.0 V
120	V_{SS0}	P	

- Unused ("NC") pins must be left open.
- Pins whose name begin with a Z operate with inverted (negative) logic.
- V_{SS0} is the logic system ground and V_{SS1} is the IDE interface driver ground.
- Applications must supply 5.0 V to V_{DD0} and 3.3 V to V_{DD1}.

Pin Functions

LC895198 Pin Functions 2
(When ATPINSEL (pin 113) is 1)

Type					
I	INPUT	B	BIDIRECTION	NC	NOT CONNECT
O	OUTPUT	P	POWER		

Pin No.	Pin	Type	Function
1	V_{DD0}	P	5.0 V
2	DREQ	O	DVD ECC data request output
3	DRESP	I	DVD ECC data latch signal input
4	HDB7 (IOP0)	B	DVD ECC data I/O These pins can be switched to function as general-purpose I/O ports by register settings.
5	HDB6 (IOP1)	B	
6	HDB5 (IOP2)	B	
7	HDB4 (IOP3)	B	
8	HDB3 (IOP4)	B	
9	HDB2 (IOP5)	B	
10	HDB1 (IOP6)	B	
11	HDB0 (IOP7)	B	
12	MCK3	O	XTALCLK 1/1, 2/5, 1/5, 1/512, and stop output
13	V_{SS0}	P	
14	V_{DD1}	P	3.3 V
15	V_{DD0}	P	5.0 V
16	DSDATA	O	DAC converter output
17	DLRCK	O	
18	DBCK	O	
19	C2PO	I	CD DSP interface
20	SDATA	I	
21	BCK	I	
22	LRCK	I	
23	EXCK	O	Subcode I/O
24	WFCK	I	
25	SBSO	I	
26	SCOR	I	
27	MCK	O	XTALCLK 1/1, 1/2, and stop output
28	XTALCK	I	Crystal oscillator circuit input
29	XTAL	O	Crystal oscillator circuit output
30	V_{SS0}	P	
31	V_{DD1}	P	3.3 V
32	V_{DD0}	P	5.0 V
33	V_{SS0}	P	
34	CSCTRL	I	Active low/active high selection for the microcontroller CS pin
35	ZRD	I	Microcontroller data read signal input
36	ZWR	I	Microcontroller data write signal input
37	ZCS	I	Register chip select input from the microcontroller
38	SUA0	I	Microcontroller register selection signals
39	SUA1	I	
40	SUA2	I	
41	SUA3	I	
42	SUA4	I	
43	SUA5	I	
44	SUA6	I	
45	V_{DD1}	P	3.3 V
46	V_{DD0}	P	5.0 V
47	V_{SS0}	P	

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Pin No.	Pin	Type	Function
48	D0	B	Microcontroller data signals. These pins have built-in pull-up resistors.
49	D1	B	
50	D2	B	
51	D3	B	
52	D4	B	
53	D5	B	
54	D6	B	
55	D7	B	
56	ZINT0	O	Interrupt request signal output to the microcontroller
57	ZINT1	O	
58	ZSWAIT	O	WAIT signal output to the microcontroller
59	ZRSTCPU	O	CPU reset signal output
60	V_{SS0}	P	
61	V_{DD0}	P	5.0 V
62	CSEL	I	ATAPI control signals ATAPI data bus
63	DD7	B	
64	DD8	B	
65	DD6	B	
66	DD9	B	
67	V_{SS1}	P	
68	DD5	B	ATAPI data bus
69	DD10	B	
70	DD4	B	
71	DD11	B	
72	V_{SS1}	P	
73	DD3	B	ATAPI data bus
74	DD12	B	
75	V_{SS1}	P	
76	V_{DD1}	P	3.3 V
77	DD2	B	ATAPI data bus
78	DD13	B	
79	V_{SS1}	P	
80	DD1	B	ATAPI data bus
81	DD14	B	
82	DD0	B	
83	DD15	B	
84	DMARQ	O	ATAPI control signal
85	V_{SS1}	P	
86	ZDIOW	I	ATAPI control signal
87	ZDIOR	I	
88	IORDY	O	
89	ZDMACK	I	
90	V_{SS1}	P	
91	V_{DD0}	P	5.0 V
92	HINTRQ	O	ATAPI control signal
93	ZIOCS16	O	
94	DA1	I	
95	ZPDIAG	B	
96	V_{SS1}	P	
97	DA0	I	ATAPI control signal
98	DA2	I	
99	ZCS1FX	I	
100	V_{SS1}	P	

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Pin No.	Pin	Type	Function
101	ZCS3FX	I	
102	ZDASP	B	ATAPI control signal
103	ZHRST	I	
104	V_{DD1}	P	3.3 V
105	V_{DD1}	P	3.3 V
106	V_{DD0}	P	5.0 V
107	V_{DD1}	P	3.3 V
108	ZRESET	I	IC reset input
109	V_{DD1}	P	3.3 V
110	V_{SS0}	P	
111	TEST1	I	Test pin. This pin must be connected to V_{SS} in normal operation.
112	V_{SS0}	P	
113	ATPINSEL	I	ATAPI pin layout selection. This pin must be connected to V_{DD0}.
114	V_{SS0}	P	
115	TEST0	I	Test pin. This pin must be connected to V_{SS} in normal operation.
116	V_{DD0}	I	5.0 V
117	AUDIOCK	I	Clock input for the CAV audio block
118	V_{DD0}	P	5.0 V
119	V_{DD0}	P	5.0 V
120	V_{SS0}	P	

- Unused ("NC") pins must be left open.
- Pins whose name begin with a Z operate with inverted (negative) logic.
- V_{SS0} is the logic system ground and V_{SS1} is the IDE interface driver ground.
- Applications must supply 5.0 V to V_{DD0} and 3.3 V to V_{DD1}.

This catalog provides information as of November, 1999. Specifications and information herein are subject to change without notice.