SANYO SEMICONDUCTOR CORP

LV3100M

3159

Bi-CMOS LSI

Parametric Equalizer

OVERVIEW

The LV3100M is a high-performance, parametric equalizer IC. It features independent center frequency, gain and Q-factor characteristics over all four frequency bands—low, low-mid, high-mid and high.

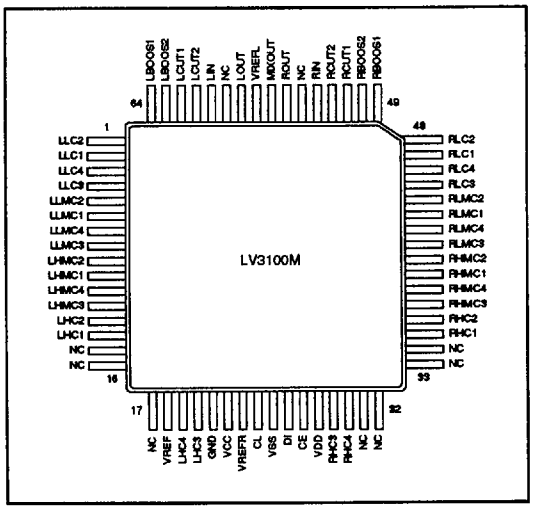
The LV3100M can be controlled digitally using a computer control bus (C^2B) to form an 11-band equalizer with gain adjustable from −12 to 12 dB in 2 dB steps and Q adjustable from 0.404 to 8.65.

The LV3100M operates from 5 V analog and 5 V digital supplies and is available in 64-pin QIPs.

FEATURES

- One-touch center frequency, gain and Q factor controls
- One-touch control using preset memory
- No external, active components required
- Adjustable gain from −12 to 12 dB in 2 dB steps
- 11 center frequency settings
- User-selectable shelving or peaking for the low and high bands
- 5 V analog and 5 V digital supplies
- 64-pin QIP

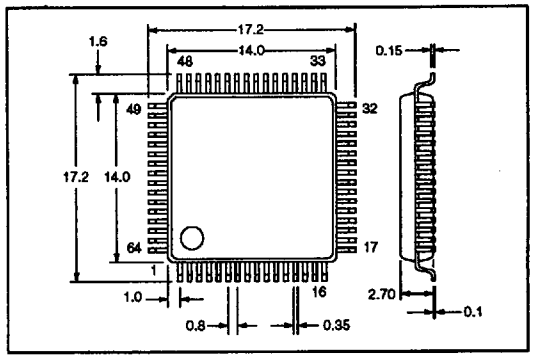
PINOUT



PACKAGE DIMENSIONS

Unit: mm

3159-QIP64E



BLOCK DIAGRAM

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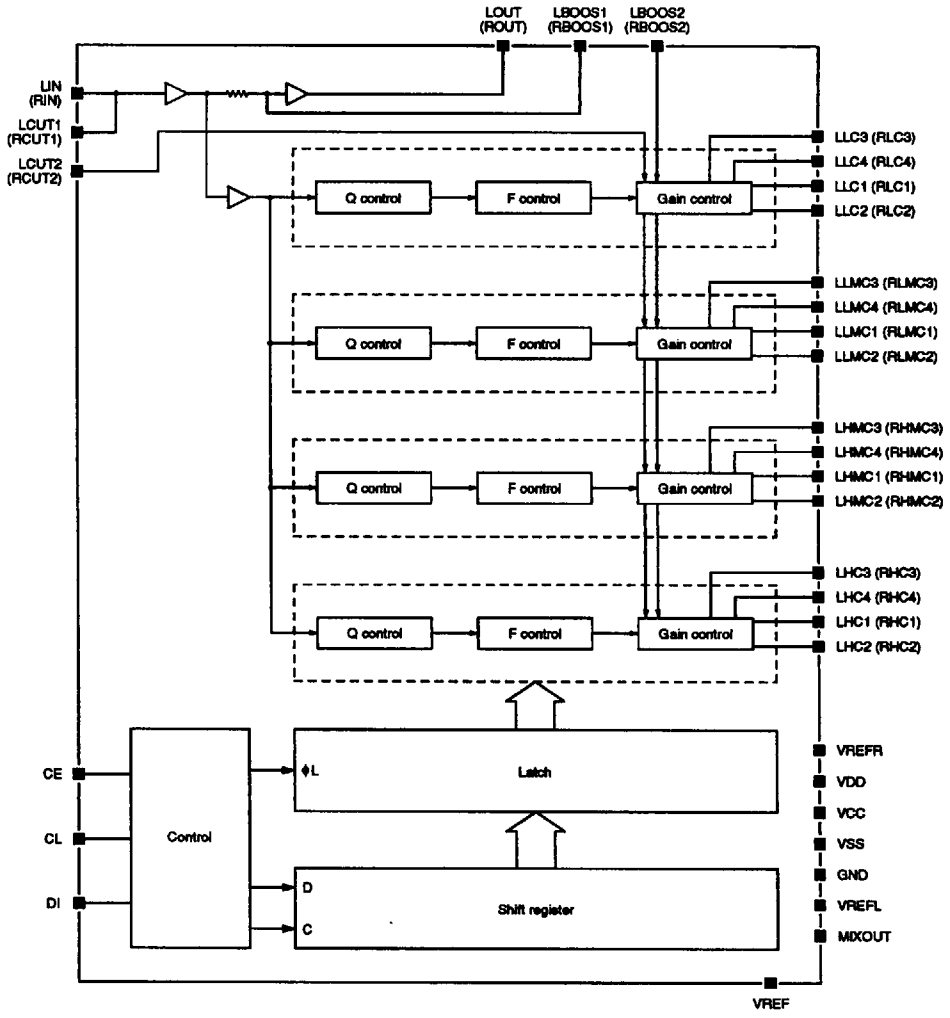

PIN DESCRIPTION

Number	Name	Description
1	LLC2	Left-channel low-band control block capacitor connections
2	LLC1	
3	LLC4	
4	LLC3	
5	LLMC2	Left-channel low-mid band control block capacitor connections
6	LLMC1	
7	LLMC4	
8	LLMC3	

Number	Name	Description
9	LHMC2	Left-channel high-mid band control block capacitor connections
10	LHMC1	
11	LHMC4	
12	LHMC3	
13	LHC2	Left-channel high-band control block capacitor connections
14	LHC1	
19	LHC4	
20	LHC3	
15 to 17, 31 to 34, 54, 59	NC	No connection
18	VREF	Internal op-amp reference voltage output. Connect a 10 μF ripple filter capacitor to ground.
21	GND	Ground
22	VCC	5 V supply
23	VREFR	Right-channel reference voltage output. Connect a 10 μF ripple filter capacitor to ground.
24	CL	Serial data clock input
25	VSS	Ground
26	DI	Serial data input
27	CE	Chip enable input
28	VDD	5 V supply
29	RHC3	Right-channel high-band control block capacitor connections
30	RHC4	
35	RHC1	
36	RHC2	
37	RHMC3	Right-channel high-mid band control block capacitor connections
38	RHMC4	
39	RHMC1	
40	RHMC2	
41	RLMC3	Right-channel low-mid band control block capacitor connections
42	RLMC4	
43	RLMC1	
44	RLMC2	
45	RLC3	Right-channel low-band control block capacitor connections
46	RLC4	
47	RLC1	
48	RLC2	
49	RBOOS1	Right-channel internal filter DC offset voltage blocking capacitor connections. Connect a 10 μF capacitor between RBOOS1 and RBOOS2 and between RCUT1 and RCUT2.
50	RBOOS2	
51	RCUT1	
52	RCUT2	

Number	Name	Description
53	RIN	Right-channel audio signal input. Low load capacitance
55	ROUT	Right-channel audio signal output. Low load capacitance
56	MIXOUT	Mixer (L + R) output
57	VREFL	Left-channel reference voltage output. Connect a 10 µF ripple filter capacitor to ground.
58	LOUT	Left-channel audio signal output. Low load capacitance
60	LIN	Left-channel audio signal input. Low load capacitance
61	LCUT2	Left-channel internal filter DC offset voltage blocking capacitor connections. Connect a 10 µF capacitor between LBOOS1 and LBOOS2 and between LCUT1 and LCUT2.
62	LCUT1	
63	LBOOS2	
64	LBOOS1	

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltages	V_{CC}	7	V
	V_{DD}	7	
LIN and RIN input voltage range	V_{I1}	0 to V_{CC} + 0.3	V
CL, CE and DI input voltage range	V_{I2}	0 to 7	V
Power dissipation	P_D	300	mW
Operating temperature range	T_{opg}	–20 to 75	°C
Storage temperature range	T_{stg}	–40 to 125	°C

Recommended Operating Conditions

T_a = 25 °C

Parameter	Symbol	Rating	Unit
Supply voltages	V_{CC}	5	V
	V_{DD}	5	
Supply voltage ranges	V_{CC}	4.0 to 6.3	V
	V_{DD}	4.0 to 6.3	

Note

$V_{CC} \geq V_{DD}$

Electrical Characteristics

V_{CC} = 5 V, V_{DD} = 5 V, T_a = 25 °C, f = 1 kHz

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply currents	I_{CC}		–	14	22	mA
	I_{DD}		–	2	5	
LIN and RIN input voltage	V_I		0	–	V_{CC}	V

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
CE, CL and DI LOW-level input voltage	V_{IL}		V_{SS}	–	$0.3V_{DD}$	V
CE, CL and DI HIGH-level input voltage	V_{IH}		$0.7V_{DD}$	–	V_{DD}	V
LOUT, ROUT and MIXOUT rms output voltage	V_O	THD = 1%	–	1.5	–	V_{rms}
LOUT, ROUT and MIXOUT load resistance	R_L		1	–	–	kΩ
Total harmonic distortion	THD	V_I = –10 dBV, flat output	–	0.03	0.1	%
		V_I = –15 dBV, R_f = 100 kΩ, 2 dB gain, boosted output	–	0.1	1	
LOUT, ROUT and MIXOUT output noise voltage	V_{NO}	R_g = 1 kΩ, IHF-A filter	–	10	25	μV
		R_g = 1 kΩ, DIN filter	–	15	–	
Channel crosstalk	CT	V_I = 0 dBV	60	80	–	dB

FUNCTIONAL DESCRIPTION

Input Data

The LV3100M is controlled using a computer control bus (C²B). The serial input data comprises an 8-bit chip address followed by a 20-bit data word. Each bit is latched on the falling edge of CL. Data input is enabled after the chip is addressed by taking CE HIGH. After the data is latched, internal analog switches operate to configure the equalizer with the specified characteristics. The input timing is shown in figure 1.

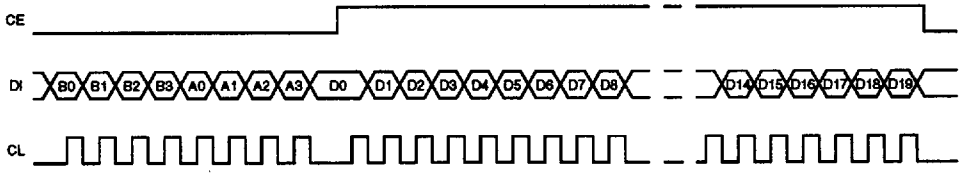

Figure 1. Input timing

The function of each bit is shown in figure 2 and in tables 1 to 7.

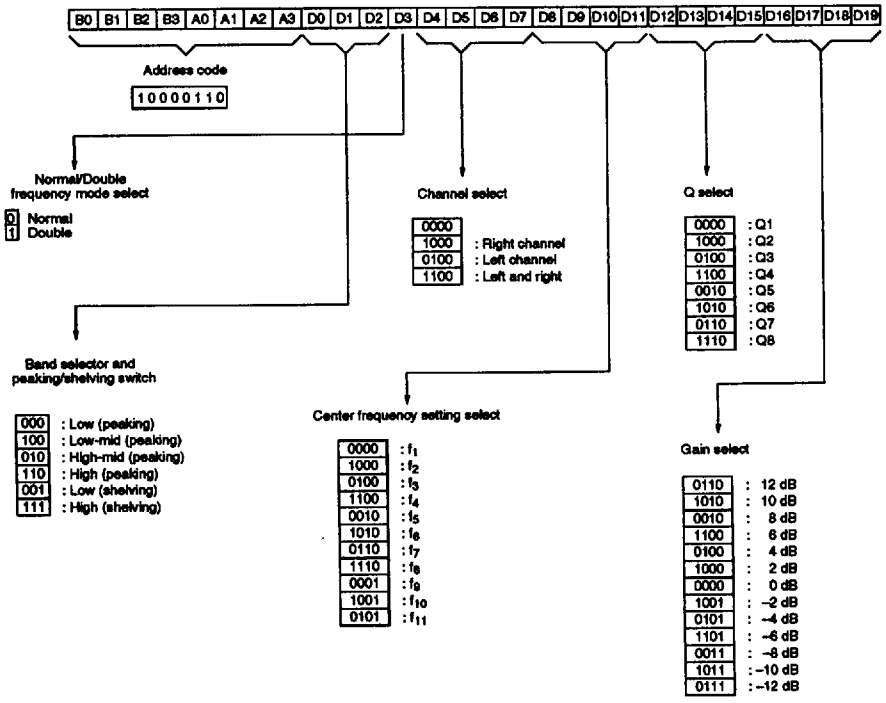

Figure 2. Input data functions

Table 1. Address code

B0	B1	B2	B3	A0	A1	A2	A3
1	0	0	0	0	1	1	0

Table 2. Band and peaking/shelving select

D0	D1	D2	Band	Peaking/shelving
0	0	0	Low	Peaking
1	0	0	Low-mid	Peaking
0	1	0	High-mid	Peaking
1	1	0	High	Peaking
0	0	1	Low	Shelving
1	1	1	High	Shelving

Note
All other input combinations are invalid.

Table 3. Normal/double frequency mode select

D3	Frequency mode
0	Normal
1	Double

Note
When D3 is 1, the center frequency for each setting is doubled. In double frequency mode, either D1 to D19 can be set, as in normal frequency mode, or D4 and D5 can be set to 0 with the other bits as don't care.

Table 4. Channel select

D4	D5	D6	D7	Channel
0	0	0	0	
1	0	0	0	Right
0	1	0	0	Left
1	1	0	0	Left and right

Note
All other input combinations are invalid.

Table 5. Center frequency setting select

D8	D9	D10	D11	Frequency setting
0	0	0	0	f_1
1	0	0	0	f_2
0	1	0	0	f_3
1	1	0	0	f_4
0	0	1	0	f_5
1	0	1	0	f_6

Table 5. Center frequency setting select—continued

D8	D9	D10	D11	Frequency setting
0	1	1	0	f_7
1	1	1	0	f_8
0	0	0	1	f_9
1	0	0	1	f_{10}
0	1	0	1	f_{11}

Note
All other input combinations are invalid.

Table 6. Q-factor select

D12	D13	D14	D15	Q factor	Octaves
0	0	0	0	0.404	3
1	0	0	0	0.667	2
0	1	0	0	1.41	1
1	1	0	0	2.15	2/3
0	0	1	0	2.87	1/2
1	0	1	0	4.32	1/3
0	1	1	0	5.76	1/4
1	1	1	0	8.65	1/6

Note
All other input combinations are invalid.

Table 7. Gain select

D16	D17	D18	D19	Gain (dB)
0	1	1	0	12
1	0	1	0	10
0	0	1	0	8
1	1	0	0	6
0	1	0	0	4
1	0	0	0	2
0	0	0	0	0
1	0	0	1	−2
0	1	0	1	−4
1	1	0	1	−6
0	0	1	1	−8
1	0	1	1	−10
0	1	1	1	−12

Note
All other input combinations are invalid.

The center frequency is determined using the selected band and center frequency settings as shown in table 8.

Table 8. Center frequency settings

Band	Center frequency (Hz)											External capacitance (μF)
	f_1	f_2	f_3	f_4	f_5	f_6	f_7	f_8	f_9	f_{10}	f_{11}	
Low	31.5	40	50	63	80	100	125	160	200	250	315	0.047
Low-mid	160	200	250	315	400	500	630	800	1 k	1.25 k	1.6 k	0.0094
High-mid	630	800	1 k	1.25 k	1.6 k	2 k	2.5 k	3.15 k	4 k	5 k	6.3 k	0.00235
High	1.6 k	2 k	2.5 k	3.15 k	4 k	5 k	6.3 k	8 k	10 k	12.5 k	16 k	0.00094

The frequency characteristics are controlled by the filter circuit shown in figure 3. This circuit can be configured for 11 different center frequencies, each displaced by one-third of an octave. When a center frequency setting is selected, the corresponding analog switch turns ON. The filter equivalent circuit is shown in figure 4.

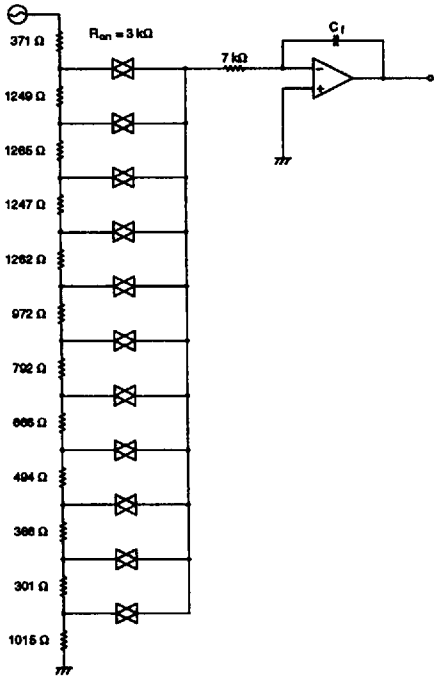

Figure 3. Filter circuit

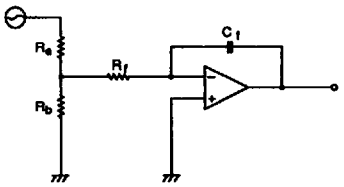

Figure 4. Filter equivalent circuit

The capacitance of the external feedback capacitor is determined from the following equation.

$$C_f = \frac{1}{2\pi R_f f_o(max)} \cdot \frac{R_b \| R_f}{R_a + (R_b \| R_f)}$$

where $f_o(max)$ is the maximum center frequency for each band. For example, $f_o(max)$ for the low band is 315 Hz.

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TYPICAL APPLICATION

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