Ordering number : ENN*6739

CMOS IC

LC866432A/28A/24A/20A/16A/12A/08A

8-Bit Single Chip Microcontroller

Preliminary

Overview

The LC866432A / 28A / 24A / 20A / 16A / 12A / 08A are 8-bit single chip microcontrollers with the following on-chip functional blocks:

- CPU : Operable at a minimum bus cycle time of 0.5μs (microsecond)
- On-chip ROM Maximum Capacity : 32K bytes
- On-chip RAM Capacity : 768 bytes (LC866432A / 28A / 24A)
  : 640 bytes (LC866420A / 16A)
  : 512 bytes (LC866412A / 08A)
- VFD automatic display controller / driver
- 16-bit timer / counter (or two 8-bit timers)
- 16-bit timer / PWM (or two 8-bit timers)
- 8 channel × 8-bit AD converter
- Two 8-bit synchronous serial-interface circuits (1-channel × 16-bit, 1-channel × 8-bit)
- 14-source 10-vectored interrupt system

All of the above functions are fabricated on a single chip.

Features

(1) Read-Only Memory (ROM) :

LC866432A	32768 × 8 bits
LC866428A	28672 × 8 bits
LC866424A	24576 × 8 bits
LC866420A	20480 × 8 bits
LC866416A	16384 × 8 bits
LC866412A	12288 × 8 bits
LC866408A	8192 × 8 bits

(2) Random Access Memory (RAM) :

LC866432A / 28A / 24A	768 × 8 bits
LC866420A / 16A	640 × 8 bits
LC866412A / 08A	512 × 8 bits

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(3) Bus Cycle Time / Instruction Cycle Time

The LC866432A / 28A / 24A / 20A / 16A / 12A / 08A are constructed to read ROM twice within one instruction cycle. It has 1.7 times more performance capability within the same instruction cycle compared to our 4-bit microcontrollers (LC66000 series).

Bus cycle time indicates the speed to read ROM.

Bus cycle time	Cycle time	Clock divider	System clock oscillation	Oscillation Frequency	Voltage
0.5μs	1μs	1 / 1	Ceramic resonator oscillation	6MHz	4.5 - 6.0V
2μs	4μs	1 / 1	Ceramic resonator oscillation	3MHz	2.5 - 6.0V
7.5μs	15μs	1 / 1	RC resonator oscillation	800kHz	2.5 - 6.0V
183μs	366μs	1 / 2	Crystal oscillation	32.768kHz	2.5 - 6.0V

(4) Ports :

- Input / output ports : 1 ports (8 terminals : port 1)
  Input / output port programmable in a bit
- 15V withstand Input / Output ports : 2 ports (12 terminals)
  Input / output port programmable nibble unit : 1 port (8 terminals : port 0)
  (When the N-channel open drain output is selected, the data in a bit can be inputted.)
  Input / output port programmable in a bit : 1 port (4 terminals : port3)
- Input port : 2 ports (14 terminals : port 7, 8)
- VFD output port : 38 terminals
  Large current output for digit : 16 terminals
  Pull-down resistor option available
- Other function
  Input / output port : 1 port (6 terminals : port E)
  Input port : 2 ports (16 terminals : port C, D)

(5) VFD automatic display controller

- Segment / digit output pattern programmable
  Any segment / digit combination available
  VFD parallel-drive available
- 16-step dimmer function available

(6) AD converter

- 8-channel × 8-bit AD converter

(7) Serial-interface

- 1-channel × 16-bit serial-interface circuits
- 1-channel × 8-bit serial-interface circuits
- LSB first / MSB first function available
- Internal 8-bit baud-rate generator in common with two serial-interface circuits

(8) Timer

- Timer 0

  16-bit timer / counter
  2-bit prescaler + 8-bit programmable prescaler
  Mode 0 : Two 8-bit timers with programmable prescaler
  Mode 1 : 8-bit timer with programmable prescaler + 8-bit counter
  Mode 2 : 16-bit timer with programmable prescaler
  Mode 3 : 16-bit counter
  The resolution of Timer is tCYC (tCYC : cycle time)

- Timer 1

  16-bit timer / PWM
  Mode 0 : Two 8-bit timers
  Mode 1 : 8-bit timer + 8-bit PWM
  Mode 2 : 16-bit timer
  Mode 3 : Variable-bit PWM (9 - 16 bits)
  In Mode 0 and Mode1, the resolution of Timer and PWM is tCYC.
  In Mode 2 and Mode 3, the resolution of Timer and PWM selectable : tCYC or 1 / 2 tCYC by program.

- Base timer

  Every 500ms overflow system for a clock application (using 32.768kHz crystal oscillation for Base timer clock)
  Every 976μs, 3.9ms, 15.6ms, 62.5ms overflow system (using 32.768kHz crystal oscillation for Base timer clock)
  The Base timer clock selectable ; 32.768kHz crystal oscillation, System clock, and programmable prescaler output of Timer 0

(9) Buzzer output

- The Buzzer sound frequency selectable ; 4KHz, 2KHz (using 32.768kHz crystal oscillation for Base timer clock)

(10) Remote-control receiver circuit (Shares with the P73 / INT3 / T0IN terminal)

- Noise Rejection function (the time constant of noize rejection filter : 1 tCYC / 16 tCYC / 64 tCYC)
  (tCYC : instruction cycle time)
- Switch Polarity function

(11) Watchdog timer

- The watchdog timer is taken on RC outside
- Watchdog timer operation selectable : interrupt system, system reset

(12) Interrupt system

- 14-source 10-vectored interrupts :
  1. External interrupt INT0 (include watchdog timer)
  2. External interrupt INT1
  3. External interrupt INT2, Timer / counter T0L (Lower 8-bit)
  4. External interrupt INT3, base timer
  5. Timer / counter T0H (Upper 8-bit)
  6. Timer T1L, Timer T1H
  7. Serial-interface SIO0
  8. Serial-interface SIO1
  9. AD converter
  10. VFD automatic display controller, Port 0
- Built-in Interrupt Priority control register

  microcontroller allows 3 levels of interrupt; low level, high level, and highest level of multiplex interrupt. It can specify a low level or a high level interrupt priority from INT2 / T0L through port 0 (i.e. the above interrupt number from three through ten). It can also specify a low level or the highest level interrupt priority to INT0 and INT1.

(13) Real-time service operation

The Real-Time Service (RTS) functions the 4-byte data-transfer between the Special Function Registers at acknowledging the interrupt request.
The RTS starts within 1 instruction cycle-time and completes within 5 instructions cycle-time after occurring the interrupt request.

(14) Subroutine stack levels
- 128 levels (Max.) : Stack area included in RAM area

(15) Multiplication and division
16-bit × 8-bit (7 instruction cycle times)
16-bit / 8-bit (7 instruction cycle times)

(16) Three oscillation circuits
- On-chip RC oscillation circuit using for the system clock.
- On-chip CF oscillation circuit using for the system clock.
- On-chip crystal oscillation circuit using for the system clock and for time-base clock.

(17) Standby function
- HALT mode function
The HALT mode is used to reduce power dissipation. In this operation mode, program execution is stopped. This operation mode can be released by interrupt request signals or the initial system reset request signal.
- HOLD mode function
The HOLD mode is used to freeze all the oscillations ;
RC (internal), CF and Crystal oscillations. This mode can be released by the following operations
• Reset terminal ($\overline{RES}$) set to Low level
• Input a assigned level to P70 / INT0 / T0IN or P71 / INT1 / T0IN terminal
• Input a Port 0 interrupt condition

(18) Factory shipment
• QIP80E delivery form

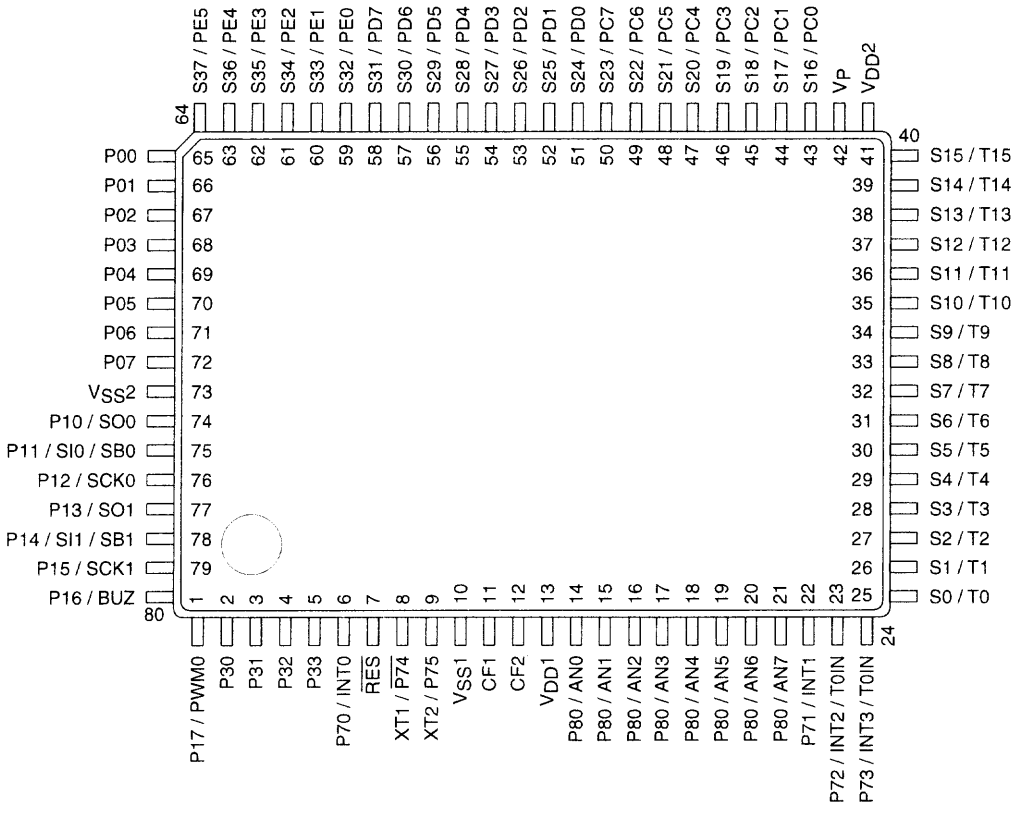
(19) Development support tools
Evaluation (EVA) chip : LC866097
EPROM version : LC86E6448
One time version : LC86P6448
Emulator : EVA-86000 + ECB866400 (Evaluation chip board) + POD866400 (POD)

• Notes for use
1. Set V_{DD}=4.0V to 6.0V at using S16 to S37 as input port.
2. Follow the under table.

Frequency range of the system clock	Voltage range	Clock Divider	Note
15kHz to 30kHz	4.5V to 6.0V	1 / 1	Can not use 1 / 2 divider
30kHz to 6MHz		1 / 1, 1 / 2	
15kHz to 30kHz	2.5V to 6.0V	1 / 1	Can not use 1 / 2 divider
30kHz to 1.5MHz		1 / 1, 1 / 2	
1.5MHz to 3MHz		1 / 2	Can not use 1 / 1 divider
Internal RC oscillation	4.5V to 6.0V	1 / 1, 1 / 2	
	2.5V to 6.0V	1 / 2	Can not use 1 / 1 divider

Pin Assignment

•QFP80E

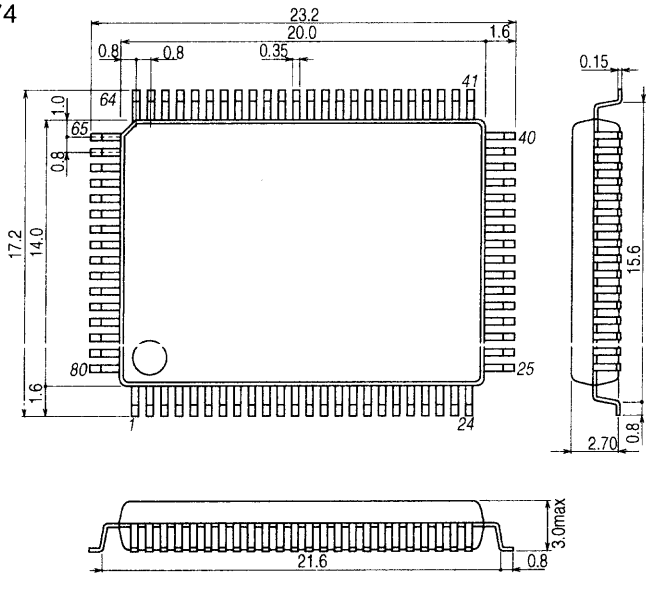


II.C00012

Package Dimensions

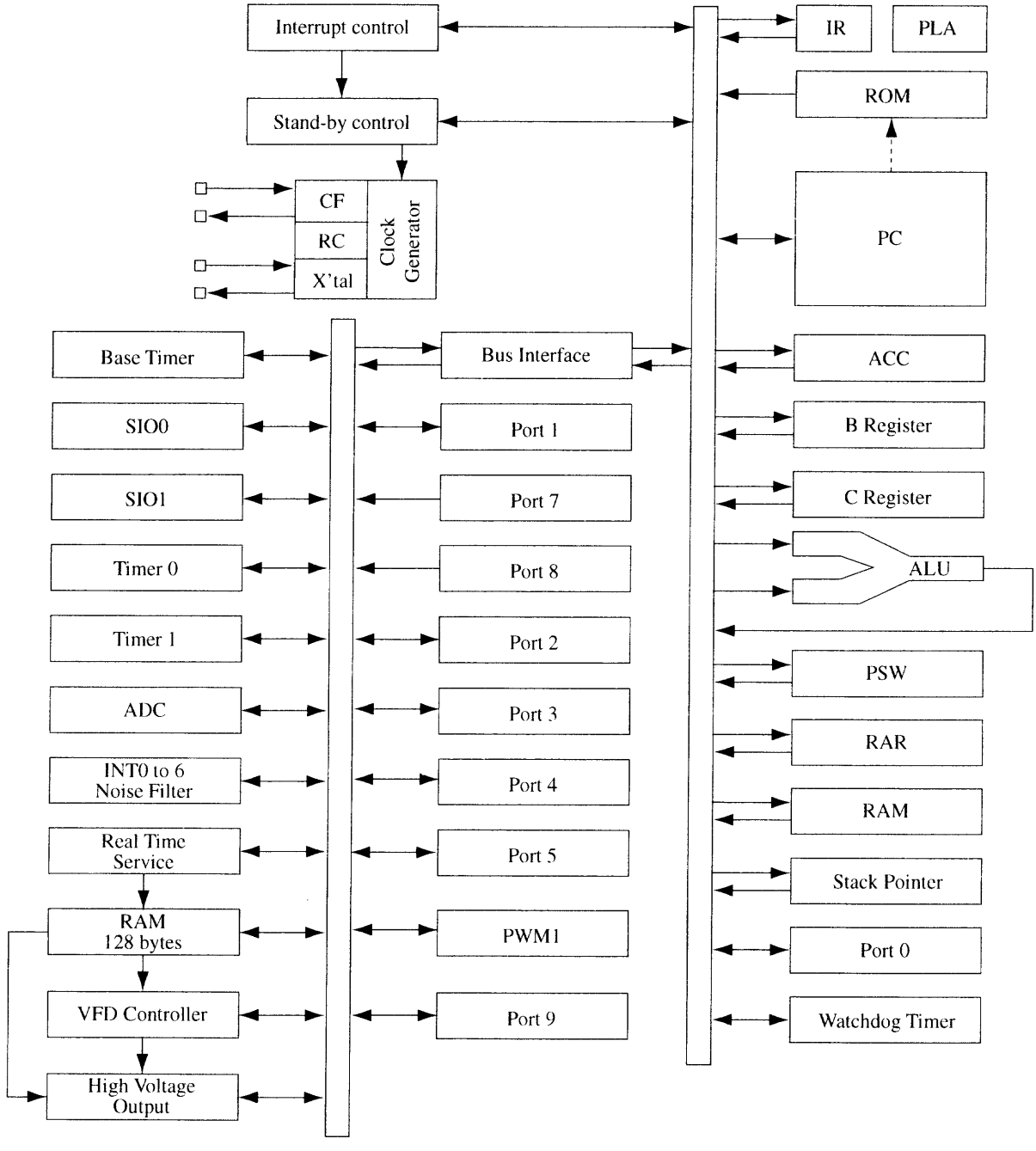
unit : mm

3174



SANYO : QIP80E

System Block Diagram



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LC866432A / 28A / 24A / 20A / 16A / 12A / 08A Pin Description

<table>
<tr><th>Pin name</th><th>I / O</th><th>Function description</th><th>Option</th></tr>
<tr><td>VSS1, 2</td><td></td><td>Power pin (-) Short-circuit VSS1 toVSS2.</td><td></td></tr>
<tr><td>VDD1, 2</td><td></td><td>Power pin (+) *1
Refer to Notes</td><td></td></tr>
<tr><td>VP</td><td></td><td>Power pin (+) for the VFD output pull-down resistor</td><td></td></tr>
<tr><td>PORT0
P00 to P07</td><td>I / O</td><td>•8-bit input / output port
Input / output in nibble units
•Input for port 0 interrupt
•Input for HOLD release
•15V withstand at N-channel open drain output</td><td>•Pull-up resistor :
Provided / Not provided (each nibble)
•Output form :
CMOS / N-channel open drain (each bit)</td></tr>
<tr><td>PORT1
P10 to P17</td><td>I / O</td><td>•8-bit input / output port
•Input / output can be specified in bit unit.
•Other pin functions
P10 : SIO0 data output
P11 : SIO0 data input / bus input / output
P12 : SIO0 clock input / output
P13 : SIO1 data output
P14 : SIO1 data input / bus input / output
P15 : SIO1 clock input / output
P16 : Buzzer output
P17 : Timer1 output (PWM0 output)</td><td>•Output form :
CMOS / N-channel open drain (each bit)</td></tr>
<tr><td>PORT3
P30 to P33</td><td>I / O</td><td>•4-bit input / output port
Input / output in bit unit
•15V withstand at N-channel open drain output</td><td>•Pull-up resistor :
Provided / Not provided (each bit)
•Output form :
CMOS / N-channel open drain (each bit)</td></tr>
<tr><td>PORT7

P70

P71 to P75</td><td>

I / O

I</td><td>•6-bit input port
•Other pin functions
P70 : INT0 input / HOLD release / N-channel Tr. output for watchdog timer
P71 : INT1 input / HOLD release input
P72 : INT2 input / timer 0 event input
P73 : INT3 input with noise filter / timer 0 event input
$\overline{P74}$: Input pin XT1 for 32.768kHz crystal resonator oscillation
P75 : Output pin XT2 for 32.768kHz crystal resonator oscillation
•Interrupt received form, vector address.
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>High level</th><th>Low level</th><th>Vector</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>03H</td></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>0BH</td></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>13H</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>1BH</td></tr>
</table></td><td>•Pull-up resistor :
Provided / Not provided
(P70, 71, 72, 73)
*$\overline{P74}$, P75 don't have the pull-up resistor option.</td></tr>
</table>

Pin name	I / O	Function description	Option
PORT8 P80 to P87	I	•8-bit input port •Other function AD input port (8 port pins)	
S0 / T0 to S6 / T6	O	Output for VFD display controller segment / timing in common	Pull-down resistor : Provided / Not provided (each bit)
S7 / T7 to S15 / T15	O	•Output for VFD display controller segment / timing with internal pull-down resistor in common •Internal pull-down resistor output	
S16 to S31	I / O	•Output for VFD display controller segment •Other function S16 : High voltage input port PC0 S17 : High voltage input port PC1 S18 : High voltage input port PC2 S19 : High voltage input port PC3 S20 : High voltage input port PC4 S21 : High voltage input port PC5 S22 : High voltage input port PC6 S23 : High voltage input port PC7 S24 : High voltage input port PD0 S25 : High voltage input port PD1 S26 : High voltage input port PD2 S27 : High voltage input port PD3 S28 : High voltage input port PD4 S29 : High voltage input port PD5 S30 : High voltage input port PD6 S31 : High voltage input port PD7	Pull-down resistor : Provided / Not provided (each bit)
S32 to S37	I / O	•Output for VFD display controller segment •Other function S32 : High voltage I /O port PE0 S33 : High voltage I /O port PE1 S34 : High voltage I /O port PE2 S35 : High voltage I /O port PE3 S36 : High voltage I /O port PE4 S37 : High voltage I /O port PE5	Pull-down resistor : Provided / Not provided (each bit)
$\overline{\text{RES}}$	I	Reset pin	
XT1 / $\overline{\text{P74}}$	I	•Input pin for 32.768kHz crystal oscillation. •Other function $\overline{\text{P74}}$ for input port In case of non use, connect to $V_{DD}1$.	
XT2 / P75	O	•Output pin for 32.768kHz crystal oscillation. •Other function P75 for input port •In case of non use, At using as oscillator, should be left opened. At using as a port, connect to $V_{DD}1$.	
CF1	I	Input pin for ceramic resonator oscillation	
CF2	O	Output pin for ceramic resonator oscillation	

*All of port options (except pull-up resistor of port 0) can be specified in bit unit.

*A state of pins at reset

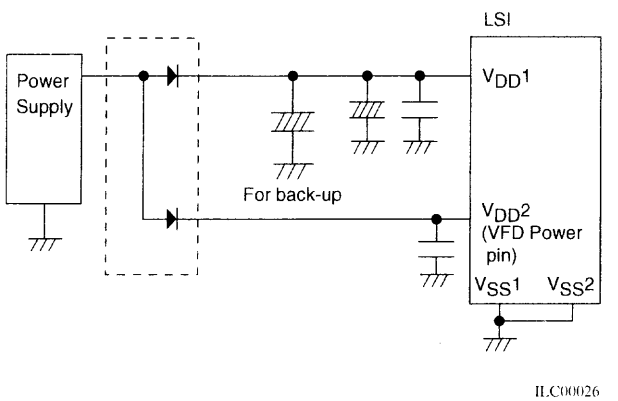
Pin name	Input / output mode	A state of pull-up resistor specified at pull-up option
Port 0	Input	Fixed pull-up resistor exist
Ports 1, 3	Input	Programmable pull-up resistor OFF
Port 70, 71, 72, 73	Input	Fixed pull-up resistor OFF

S0 / T0 to S15 / T15	P-channel Transistor OFF
S16 to S37	P-channel Transistor OFF

[Notes]

When connecting to the power supply, the power pins must be connected like the following figure.

In case of the LC866448B/44B/40B/36B



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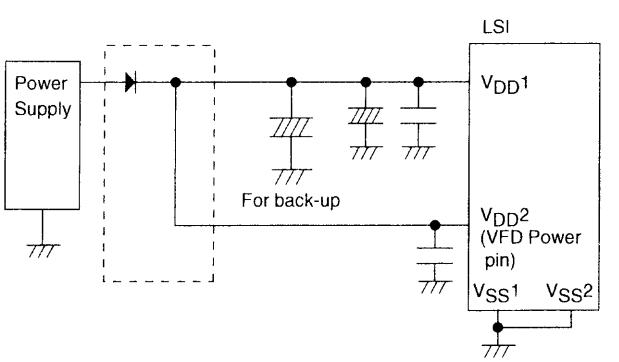
In case of the LC866432A / 28A / 24A / 20A / 16A / 12A / 08A



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*1 Each of the power pins, $V_{DD}1$ and $V_{DD}2$, should be connected the capasitors for reducing the noise into the $V_{DD}1$ pin.

1. Absolute Maximum Ratings at $V_{SS}1=V_{SS}2=0V$ and Ta=25°C

Parameter		Symbol	Pins	Conditions	V_{DD}[v]	Ratings min.	Ratings typ.	Ratings max.	unit
Supply voltage		V_{DD} MAX	$V_{DD}1$, $V_{DD}2$	$V_{DD}1=V_{DD}2$		-0.3		+7.0	V
Input voltage		V_I(1)	•Ports 71, 72, 73 •Ports $\overline{74}$, 75 •Port 8 •$\overline{RES}$			-0.3		V_{DD} + 0.3	
		V_I(2)	V_P			V_{DD}-45		V_{DD} + 0.3	
Output voltage		V_O	•S0 / T0 to S15 / T15			V_{DD}-45		V_{DD} + 0.3	
Input / output voltage		V_{IO}(1)	•Ports1 •Port 70 •Ports 0,3 at CMOS output option			-0.3		V_{DD} + 0.3	
		V_{IO}(2)	Ports 0, 3 at N-ch open drain output option			-0.3		15	
		V_{IO}(3)	S16 to S37			V_{DD}-45		V_{DD} + 0.3	
High Level output current	Peak output current	IOPH(1)	•Ports 0, 1, 3	•CMOS output •At each pins		-10			mA
		IOPH(2)	S0 / T0 to S15 / T15	At each pins		-30			
		IOPH(3)	S16 to S37	At each pins		-15			
	Total output current	ΣIOAH(1)	•Ports 0, 1, 3	The total all pins		-30			
		ΣIOAH(2)	S0 / T0 to S15 / T15	The total all pins		-55			
		ΣIOAH(3)	S16 to S37	The total all pins		-115			
Low Level output current	Peak output current	IOPL(1)	•Ports 0, 1, 3	At each pins				20	
		IOPL(2)	Port 70	At each pins				15	
	Total output current	ΣIOAL(1)	Port 0	The total all pins				40	
		ΣIOAL(2)	Port 1, 3	The total all pins				40	
Power dissipation (max)		Pdmax	QFP80E	Ta= -30 + 70°C				490	mW
Operating temperature range		Topr				-30		70	°C
Storage temperature range		Tstg				-65		150	

2. Recommended Operating Range at $V_{SS}1=V_{SS}2=0V$ and Ta= -30°C to +70°C

Parameter	Symbol	Pins	Conditions	V_{DD} [V]	Ratings min.	Ratings typ.	Ratings max.	unit
Operating supply voltage range	$V_{DD}(1)$	$V_{DD}1=V_{DD}2$	0.98μs ≤ tCYC tCYC ≤ 400μs		4.5		6.0	V
	$V_{DD}(2)$		3.9μs ≤ tCYC tCYC ≤ 400μs		2.5		6.0	
HOLD voltage	V_{HD}	$V_{DD}1=V_{DD}2$	RAMs and Registers hold voltage at HOLD mode.		2.0		6.0	
Pull-down voltage	V_P	V_P		2.5 to 6.0	-35		V_{DD}	
Input high voltage	$V_{IH}(1)$	Port 0 at CMOS output option	Output disable	2.5 to 6.0	0.33V_{DD} +1.0		V_{DD}	
	$V_{IH}(2)$	Port 0 at N-ch open drain output	Output disable	4.0 to 6.0	0.8V_{DD}		13.5	
				2.5 to 4.0	0.75V_{DD}		13.5	
	$V_{IH}(3)$	•Port 1 •Port 72, 73 •Port 3 at CMOS output option	Output disable	2.5 to 6.0	0.75V_{DD}		V_{DD}	
	$V_{IH}(4)$	•Port 3 at N-ch open drain output	Output disable Tr. OFF	4.0 to 6.0	0.8V_{DD}		13.5	
				2.5 to 4.0	0.75V_{DD}		13.5	
	$V_{IH}(5)$	•Port 70 Port input / interrupt •Port 71 •$\overline{RES}$	Output N-channel Tr. OFF	2.5 to 6.0	0.75V_{DD}		V_{DD}	
	$V_{IH}(6)$	•Port 70 Watchdog timer	Output N-channel Tr. OFF	2.5 to 6.0	0.9V_{DD}		V_{DD}	
	$V_{IH}(7)$	•Port 8 •Port $\overline{74}$, 75	Using as port	2.5 to 6.0	0.75V_{DD}		V_{DD}	
	$V_{IH}(8)$	S16 to S37	Output P-channel Tr. OFF	4.0 to 6.0	0.33V_{DD} +1.0		V_{DD}	
Input low voltage	$V_{IL}(1)$	Port 0 at CMOS output option	Output disable	2.5 to 6.0	V_{SS}		0.2V_{DD}	
	$V_{IL}(2)$	Port 0 at N-ch open drain output	Output disable	2.5 to 6.0	V_{SS}		0.25V_{DD}	
	$V_{IL}(3)$	•Port 1, 3 •Port 72, 73	Output disable	2.5 to 6.0	V_{SS}		0.25V_{DD}	
	$V_{IL}(4)$	•Port 70 Port input / interrupt •Port 71 •$\overline{RES}$	Output N-channel Tr. OFF	2.5 to 6.0	V_{SS}		0.25V_{DD}	
	$V_{IL}(5)$	Port 70 Watchdog timer	Output N-channel Tr. OFF	2.5 to 6.0	V_{SS}		0.8V_{DD} -1.0	
	$V_{IL}(6)$	•Port 8 •Port $\overline{74}$, 75	Using as port	2.5 to 6.0	0.75V_{SS}		0.25V_{DD}	
	$V_{IL}(7)$	S16 to S37	Output P-channel Tr. OFF	4.0 to 6.0	V_P		0.2V_{DD}	

Parameter	Symbol	Pins	Conditions		Ratings			unit
				V_{DD} [V]	min.	typ.	max.	
Operation cycle time	tCYC			4.5 to 6.0	0.98		400	µs
				2.5 to 6.0	3.9		400	
Oscillation frequency range (Note 1)	FmCF(1)	CF1, CF2	•6MHz (ceramic resonator oscillation) •Refer to figure 1	4.5 to 6.0	5.88	6	6.12	MHz
	FmCF(2)	CF1, CF2	•3MHz (ceramic resonator oscillation) •Refer to figure 1	2.5 to 6.0	2.94	3	3.06	
	FmRC		RC oscillation	2.5 to 6.0	0.3	0.8	3.0	
	FsXtal	XT1, XT2	•32.768kHz (crystal oscillation) •Refer to figure 2	2.5 to 6.0		32.768		kHz
Oscillation stable time period (Note 1)	tmsCF(1)	CF1, CF2	•6MHz (ceramic resonator oscillation) •Refer to figure 3	4.5 to 6.0		0.05	0.5	ms
	tmsCF(2)	CF1, CF2	•3MHz (ceramic resonator oscillation) •Refer to figure 3	4.5 to 6.0		0.1	1.0	
				2.5 to 6.0		0.1	3.0	
	tssXtal	XT1, XT2	•32.768kHz (crystal oscillation) •Refer to figure 3	4.5 to 6.0		1	1.5	s
				2.5 to 6.0		1	3	

(Note 1) The oscillation constant is shown on table 1 and table 2.

3. Electrical Characteristics at $V_{SS}1=V_{SS}2=0V$ and Ta= -30°C to +70°C

Parameter	Symbol	Pins	Conditions	Ratings				unit
				V_{DD} [V]	min.	typ.	max.	
Input high current	$I_{IH}(1)$	Ports 0, 3 of Open drein output	•Output disable •V_{IN}=13.5V (including off-leak current of the output Tr.)	2.5 to 6.0			5	µA
	$I_{IH}(2)$	•Ports 0 without pull-up MOS Tr. •Potr 1, 3	•Output disable •Pullup MOS Tr. OFF. $V_{IN}=V_{DD}$ (including off-leak current of the output Tr.)	2.5 to 6.0			1	
	$I_{IH}(3)$	•Ports 70, 71, 72, 73 without pull-up MOS Tr. •Potr 8	$V_{IN}=V_{DD}$	2.5 to 6.0			1	
	$I_{IH}(4)$	$\overline{RES}$	$V_{IN}=V_{DD}$	2.5 to 6.0			1	
	$I_{IH}(5)$	Potr $\overline{74}$, 75	•Output disable •$V_{IN}=V_{DD}$	2.5 to 6.0			1	
	$I_{IH}(6)$	•S16 to S37 without pull-down resistor (Potr C, D, E)	•Output disable •$V_{IN}=V_{DD}$	2.5 to 6.0			1	
Input low current	$I_{IL}(1)$	•Ports 1, 3 •Port 0 without pull-up MOS Tr.	•Output disable •Pull-up MOS Tr. OFF. $V_{IN}=V_{SS}$ (including off-leak current of output Tr.)	2.5 to 6.0	-1			
	$I_{IL}(2)$	•Ports 70, 71, 72, 73 without pull-up MOS Tr. •Port 8	$V_{IN}=V_{SS}$	2.5 to 6.0	-1			
	$I_{IL}(3)$	•$\overline{RES}$	$V_{IN}=V_{SS}$	2.5 to 6.0	-1			
	$I_{IL}(4)$	Potr $\overline{74}$, 75	•Using as port •$V_{IN}=V_{SS}$	2.5 to 6.0	-1			
Output high voltage	$V_{OH}(1)$	ports 0, 1, 3 of CMOS output	I_{OH}= -1.0mA	4.5 to 6.0	V_{DD}-1			V
	$V_{OH}(2)$		I_{OH}= -0.1mA	2.5 to 6.0	V_{DD}-0.5			
	$V_{OH}(3)$	S0 / T0 to S15 / T15	I_{OH}= -20mA	4.5 to 6.0	V_{DD}-1.8			
	$V_{OH}(4)$		•I_{OH}= -1mA •The current of any unmeasurement pin is not over 1mA.	2.5 to 6.0	V_{DD}-1			
	$V_{OH}(5)$	S16 to S37	I_{OH}= -5mA	4.5 to 6.0	V_{DD}-1.8			
	$V_{OH}(6)$		The current of any unmeasurement pin is not over 1mA.	2.5 to 6.0	V_{DD}-1			

Parameter	Symbol	Pins	Conditions	VDD [V]	Ratings min.	Ratings typ.	Ratings max.	unit
Output low voltage	$V_{OL}(1)$	•Ports 0, 1, 3 •PWM1	I_{OL}=10mA	4.5 to 6.0			1.5	V
	$V_{OL}(2)$		•I_{OL}=1.6mA	4.5 to 6.0			0.4	
	$V_{OL}(3)$		•I_{OL}=1.0mA •The current of any unmeasurement pin is not over 1mA.	2.5 to 6.0			0.4	
	$V_{OL}(4)$	Port 70	I_{OL}=1mA	4.5 to 6.0			0.4	
	$V_{OL}(5)$		I_{OL}=0.5mA	2.5 to 6.0			0.4	
Pull-up MOS Tr. resistor	Rpu	•Ports 0, 1, 3 •Ports 70, 71, 72, 73	V_{OH}=0.9V_{DD}	4.5 to 6.0	15	40	70	kΩ
				2.5 to 4.5	25	70	150	
Output off-leak current	$I_{OFF}(1)$	•S0 / T0 to S6 / T6, S16 to S37 without pull-down resistor	•Output P-ch Tr. OFF. •V_{OUT}=V_{SS}	2.5 to 6.0	-1			μA
	$I_{OFF}(2)$		•Output P-ch Tr. OFF. •V_{OUT}=V_{DD}-40V	2.5 to 6.0	-30			
Resistance of the low level hold Tr.	Rinpd	S16 to S37	•Output P-ch Tr. OFF. •Using as input ports	4.0 to 6.0		200		kΩ
High voltage pull-down resistor	Rpd	S0 / T0 to S15 / T15, S16 to S37 with pull-down resistor	•Output P-ch Tr. OFF. •V_{OUT}=3V •VP= -30V	5.0	60	100	200	
Hysteresis voltage	VHIS	•Port 1 •Ports 70, 71, 72, 73 •$\overline{RES}$	Output disable	2.5 to 6.0		0.1V_{DD}		V
Pin capacitance	CP	All pins	•f=1MHz Unmeasurement terminals for input are set to V_{SS} level. •Ta=25°C	2.5 to 6.0		10		pF

4. Serial Input / Output Characteristics at $V_{SS}1=V_{SS}2=0V$ and Ta= -30°C to +70°C

Parameter			Symbol	Pins	Conditions	Ratings				unit
						V_{DD} [V]	min.	typ.	max.	
Serial clock	Input clock	Cycle	tCKCY(1)	SCK0, SCK1	Refer to figure 5	2.5 to 6.0	2			tCYC
		Low level pulse width	tCKL(1)			2.5 to 6.0	1			
		High level pulse width	tCKH(1)			2.5 to 6.0	1			
	Output clock	Cycle	tCKCY(2)	SCK0, SCK1	•Use pull-up resistor (1kΩ) when open drain output. •Refer to figure 5	2.5 to 6.0	2			
		Low level pulse width	tCKL(2)			2.5 to 6.0		1 / 2tCKCY		
		High level pulse width	tCKH(2)			2.5 to 6.0		1 / 2tCKCY		
Serial input	Data set-up time		tICK	•SI0, SI1 •SB0, SB1	•Data set-up to SCK0, 1	4.5 to 6.0	0.1			µs
						2.5 to 6.0	0.4			
	Data hold time		tCKI		•Data hold from SCK0, 1	4.5 to 6.0	0.1			
					•Refer to figure 5	2.5 to 6.0	0.4			
Serial output	Output delay time (Serial clock is extrnal clock)		tCKO(1)	•SO0, SO1 •SB0,SB1	•Use pull-up resistor (1kΩ) when open drain output.	4.5 to 6.0			7 / 12tCYC +0.2	
						2.5 to 6.0			7 / 12tCYC +1	
	Output delay time (Serial clock is internal clock)		tCKO(2)		•Data hold from SCK0, 1 •Refer to figure 5	4.5 to 6.0			1 / 3tCYC +0.2	
						2.5 to 6.0			1 / 3tCYC +1	

5. Pulse Input Conditions at $V_{SS}1=V_{SS}2=0V$ and Ta= -30°C to +70°C

Parameter	Symbol	Pins	Conditions	Ratings				unit
				V_{DD} [V]	min.	typ.	max.	
High / low level pulse width	tPIH(1) tPIL(1)	•INT0, INT1 •INT2 / T0IN	•Interrupt acceptable •Timer0-countable	2.5 to 6.0	1			tCYC
	tPIH(2) tPIL(2)	•INT3 / T0IN (The noise rejection clock select to 1 / 1.)	•Interrupt acceptable •Timer0-countable	2.5 to 6.0	2			
	tPIH(3) tPIL(3)	INT3 / T0IN (The noise rejection clock select to 1 / 16.)	•Interrupt acceptable •Timer0-countable	2.5 to 6.0	32			
	tPIL(4) tPIL(4)	INT3 / T0IN (The noise rejection clock select to 1 / 64.)	•Interrupt acceptable •Timer0-countable	2.5 to 6.0	128			
	tPIL(5)	$\overline{RES}$	Reset acceptable	2.5 to 6.0	200			μs

6. A / D converter Characteristics at $V_{SS}1=V_{SS}2=0V$ and Ta= -30°C to +70°C

Parameter	Symbol	Pins	Conditions	Ratings				unit
				V_{DD} [V]	min.	typ.	max.	
Resolution	N			4.5 to 6.0		8		bit
Absolute precision (Note 2)	ET			4.5 to 6.0			±1.5	LSB
Conversion time	CAD		AD conversion time=16 × tCYC (ADCR2=0) (Note 3)	4.5 to 6.0	15.68 (tCYC= 0.98μs)		65.28 (tCYC= 4.08μs)	μs
			AD conversion time=32 × tCYC (ADCR2=1) (Note 3)		31.36 (tCYC= 0.98μs)		130.56 (tCYC= 4.08μs)	
Analog input voltage range	VAIN	AN0 to AN7		4.5 to 6.0	VSS		VDD	V
Analog port input current	IAINH		VAIN=VDD	4.5 to 6.0			1	μA
	IAINL		VAIN=VSS	4.5 to 6.0	-1			

(Note 2) Absolute precision excepts quantizing error (±1 / 2 LSB).

(Note 3) The conversion time means the time from executing the AD conversion instruction to setting the complete digital conversion value to the register.

7. Current Dissipation Characteristics at $V_{SS}1=V_{SS}2=0V$ and Ta= -30°C to +70°C

Parameter	Symbol	Pins	Conditions	Ratings				unit
				V_{DD} [V]	min.	typ.	max.	
Current dissipation during basic operation (Note 4)	IDDOP(1)		•FmCF=6MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation. •System clock : CF oscillation •Internal RC oscillation stops. •1 / 1 divided	4.5 to 6.0		10	25	mA
	IDDOP(2)		•FmCF=3MHz Ceramic resonator oscillation. •FsXtal=32.768kHz crystal oscillation. •System clock : CF oscillation •Internal RC oscillation stops. •1 / 2 divided	4.5 to 6.0		3	9	
	IDDOP(3)			2.5 to 4.5		1.5	5	
	IDDOP(4)		•FmCF=0Hz (when oscillation stops). •FsXtal=32.768kHz crystal oscillation. •System clock : RC oscillation •1 / 2 divided	4.5 to 6.0		0.7	3.4	
	IDDOP(5)			2.5 to 4.5		0.4	2.8	
	IDDOP(6)		•FmCF=0Hz (when oscillation stops). •FsXtal=32.768kHz crystal oscillation •System clock : crystal oscillation •Internal RC oscillation stops. •1 / 2 divided	4.5 to 6.0		35	130	µA
	IDDOP(7)			2.5 to 4.5		15	70	

Parameter	Symbol	Pins	Conditions	VDD [V]	Ratings min.	typ.	max.	unit
Current dissipation HALT mode (Note 4)	IDDHALT(1)		•HALT mode •FmCF=6MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops. •1 / 1 divided	4.5 to 6.0		5	14	mA
	IDDHALT(2)		•HALT mode FmCF=3MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops. •1 / 2 divided	4.5 to 6.0		2.2	7	
	IDDHALT(3)			2.5 to 4.5		0.8	4	
	IDDHALT(4)		•HALT mode FmCF=0Hz (when oscillation stops). •FsXtal=32.768kHz crystal oscillation •System clock : RC oscillation •1 / 2 divided	4.5 to 6.0		400	1600	μA
	IDDHALT(5)			2.5 to 4.5		200	1300	
	IDDHALT(6)		•HALT mode FmCF=0Hz (when oscillation stops). •FsXtal=32.768kHz crystal oscillation •System clock : crystal oscillation •Internal RC oscillation stops. •1 / 2 divided	4.5 to 6.0		25	100	
	IDDHALT(7)			2.5 to 4.5		8	55	
Current dissipation HOLD mode (Note 4)	IDDHOLD(1)		HOLD mode	4.5 to 6.0		0.05	30	
	IDDHOLD(2)			2.5 to 4.5		0.02	20	

(Note 4) The currents of output transistors and pull-up MOS transistors are ignored.

Table 1. Ceramic resonator oscillation guaranteed constant (main-clock)

A kind of oscillation	Producer	Oscillator	C1	C2
6MHz ceramic resonator oscillation	Murata	CSA 6.00MG	33pF	33pF
		CST 6.00MGW	on chip	
	Kyocera	KBR-6.00MSA	33pF	33pF
		PBRC 6.00A(chip type)	33pF	33pF
		KBR-6.0MKS	on chip	
		PBRC 6.00B(chip type)		
3MHz ceramic resonator oscillation	Murata	CSA 3.00MG	33pF	33pF
		CST 3.00MGW	on chip	
	Kyocera	KBR-3.0MS	47pF	47pF

* Both C1 and C2 must use K rank (±10%) and SL characteristics.

Table 2. Crystal oscillation guaranteed constant (sub-clock)

A kind of oscillation	Producer	Oscillator	C3	C4
32.768kHz crystal oscillation	Kyocera	KF-38G-13P0200	18pF	18pF

* Both C3 and C4 must use J rank (±5%) and CH characteristics.
(It is about the application which is not in need of high precision. Use K rank (±10%) and SL characteristics.)

Notes • Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest possible pattern length.
• If you use other oscillators herein, we provide no guarantee for the characteristics.

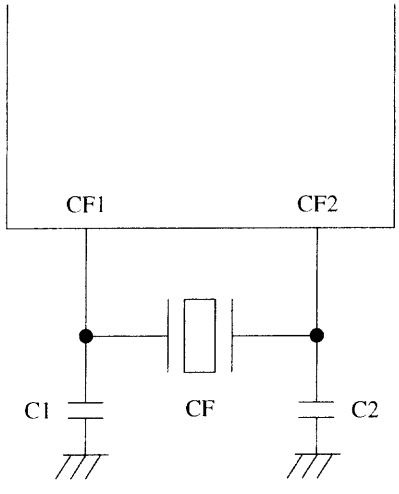


Figure1. Main-clock
Ceramic resonator oscillation

ILC00059

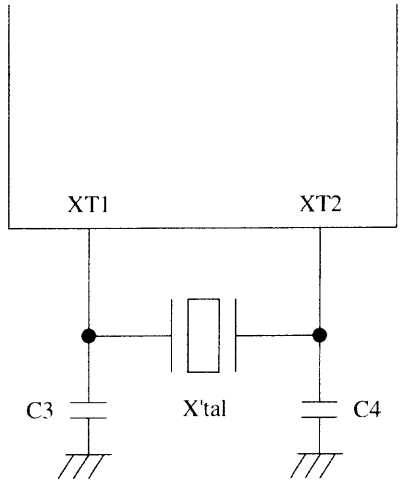


Figure2. Sub-clock
Crystal oscillation

ILC00065

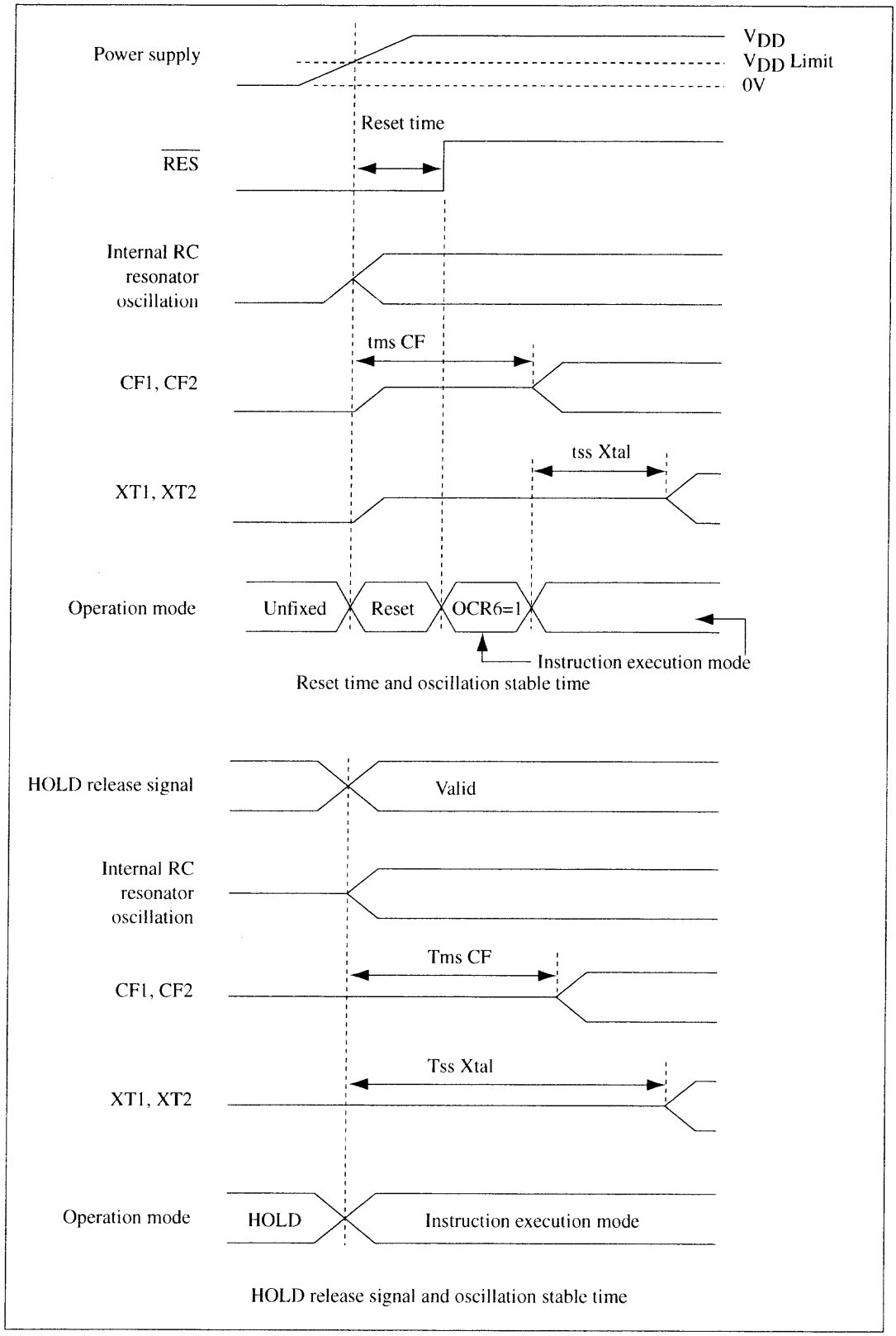
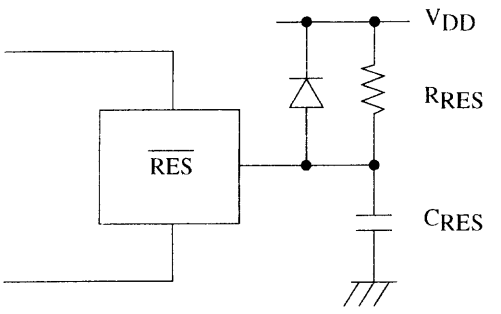


Figure3. Oscillation stable time

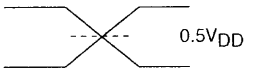
B.C00044



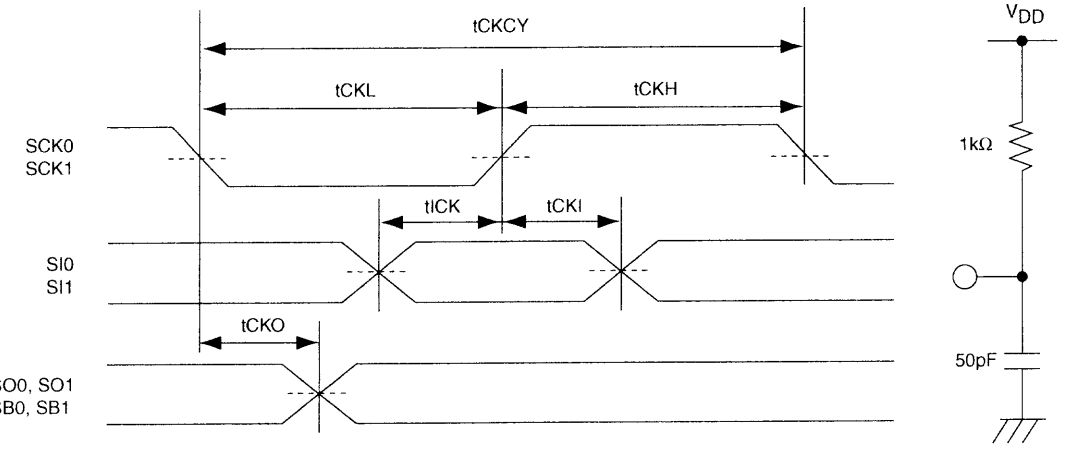
(Note) Fix the value of C_{RES}, R_{RES} that is sure to reset untill 200µs, after Power supply has been over inferior limit of supply voltage.

Figure4. Reset circuit

ILC00052



<AC timing point>



<Timing>

<Test load>

Figure5. Serial input / output test condition

ILC00073

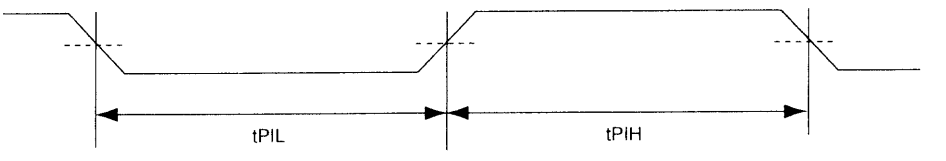


Figure6. Pulse input timing condition

ILC00074

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