

HIGH-PERFORMANCE PRODUCTS

Description

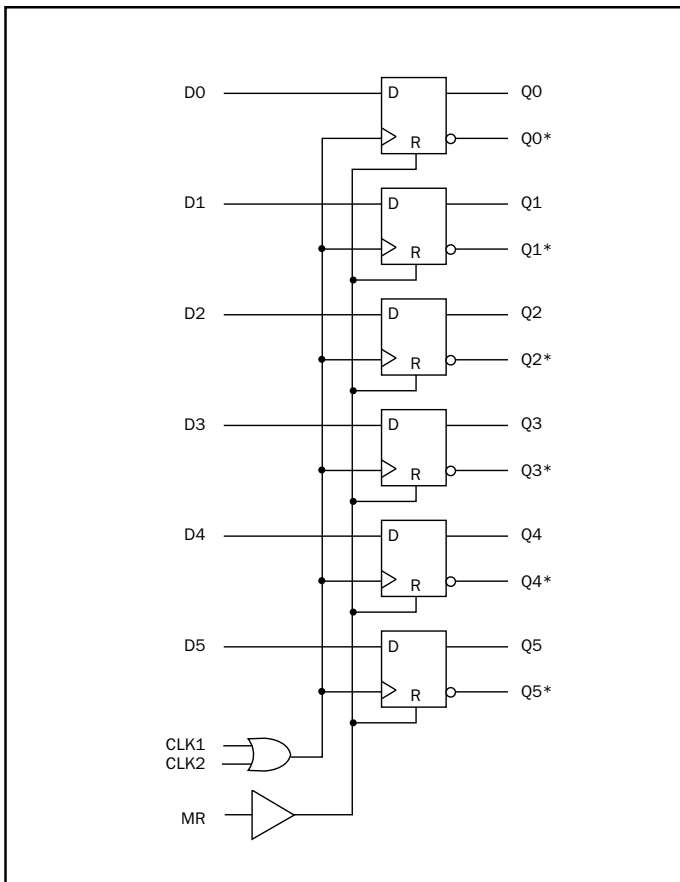
The SK10/100E151 offers 6 edge-triggered, high-speed, master-slave D-type flip-flops with differential outputs, designed for use in new high-performance ECL systems. This device is fully compatible with MC10E151 and MC100E151. The two external clock signals (CLK1, CLK2) are gated through a logical OR operation before use as clocking control for the flip-flops. Data is clocked into the flip-flops on the rising edge of either CLK1 or CLK2 (or both). When both CLK1 and CLK2 are at a logic LOW, data enters the master and is transferred to the slave when either CLK or CLK2 (or both) go HIGH.

The MR (Master Reset) signal operates asynchronously to make all Q outputs go to a logic LOW.

Features

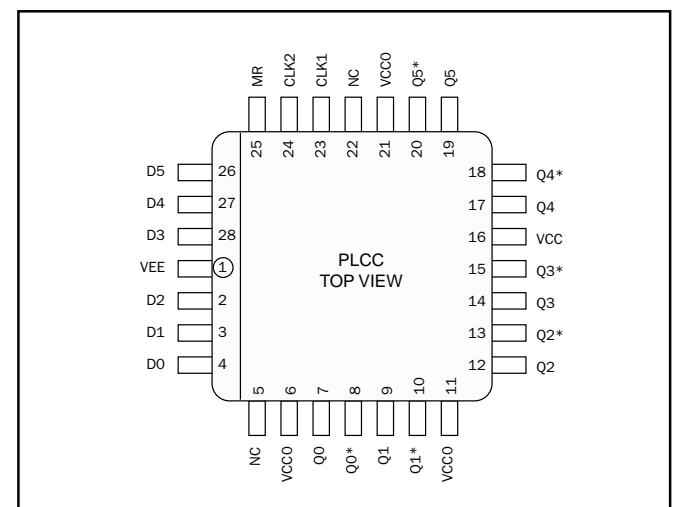
- 1100 MHz Toggle Frequency
- Extended 100E VEE Range of $-4.2V$ to $-5.46V$
- Differential Outputs
- Asynchronous Master Reset
- Dual Clocks
- Internal $75K\Omega$ Input Pull-Down Resistors
- ESD Protection of $>4000V$
- Fully Compatible with MC10E/100E151
- Specified Over Industrial Temperature Range: $-40^{\circ}C$ to $+85^{\circ}C$
- Available in 28-Pin PLCC Package

Functional Block Diagram



PIN Description

Pin	Function
D0–D5	Data Inputs
CLK1, CLK2	Clock Inputs
MR	Master Reset
Q0–Q5	True Outputs
Q0*–Q5*	Inverting Outputs
VCC0	VCC to Output



Truth Tables

Inputs				Output
Dn	CLK1	CLK2	MR	Qn(t+1)
X	X	X	H	L

Asynchronous Operation

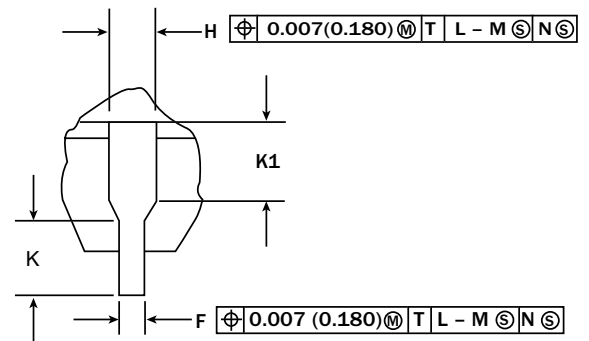
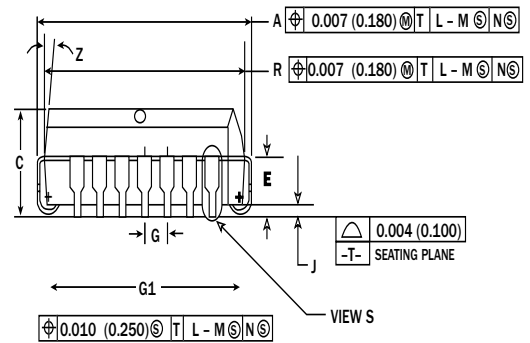
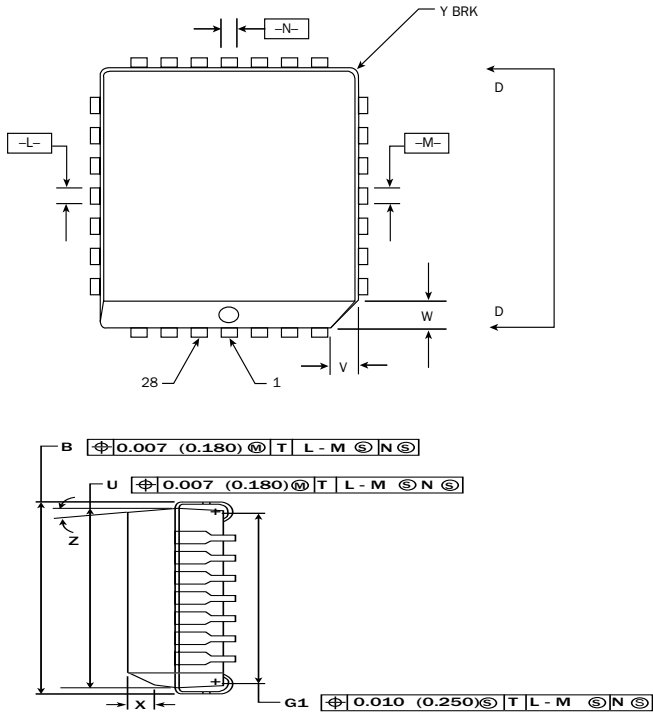
Inputs				Output
Dn	CLK1	CLK2	MR	Qn(t+1)
L	u	L	L	L
H	u	L	L	H
L	L	u	L	L
H	L	u	L	H
X	H	u	L	Qn(t)
X	u	H	L	Qn(t)
X	L	L	L	Qn(t)

Synchronous Operation

NOTES:

1. H = HIGH Voltage Level
2. L = LOW Voltage Level
3. X = Don't Care
4. t = Time Before Positive CLK Transition
5. t+1 = Time After Positive CLK Transition
6. u = LOW-to-HIGH Transition

28-Pin PLCC Package



NOTES:

1. Datums -L-, -M-, and -N - determined where top of lead shoulder exits plastic body at mold parting line.
2. DIM G1, true position to be measured at Datum -T-, Seating Plane.
3. DIM R and U do not include mold flash. Allowable mold flash is 0.010 (0.250) per side.
4. Dimensioning and tolerancing per ANSI Y14.5M, 1982.
5. Controlling Dimension: Inch.
6. The package top may be smaller than the package bottom by up to 0.012 (0.300). Dimensions R and U are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
7. Dimension H does not include Dambar protrusion or intrusion. The Dambar protrusion(s) shall not cause the H dimension to be greater than 0.037 (0.940). The Dambar intrusion(s) shall not cause the H dimension to be smaller than 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050	BSC	1.27	BSC
H	0.026	0.032	0.66	0.81
J	0.020	-	0.51	-
K	0.025	-	0.64	-
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	-	0.020	-	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	-	1.02	-

HIGH-PERFORMANCE PRODUCTS
DC Characteristics
SK10/100E151 DC Electrical Characteristics (Notes 1, 2)
 $(V_{CC} - V_{EE} = 4.2V \text{ to } 5.46V; V_{OUT} \text{ loaded } 50\Omega \text{ to } V_{CC} - 2.0V)$

Symbol	Characteristic	TA = -40°C			TA = 0°C			TA = +25°C			TA = +85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I _{IH}	Input High Current			150			150			150			150	μA
I _{EE}	Power Supply Current 10EL 100EL	44 43		78 78	44 43		78 78	44 43		78 78	44 43		78 85	mA mA
V _{CC} - V _{EE}	Power Supply Voltage	4.2		5.46	4.2		5.46	4.2		5.46	4.2		5.46	V

AC Characteristics
SK10/100E151 AC Electrical Characteristics
 $(V_{CC} - V_{EE} = 4.2V \text{ to } 5.46V; V_{OUT} \text{ loaded } 50\Omega \text{ to } V_{CC} - 2.0V)$

Symbol	Characteristic	TA = -40°C			TA = 0°C			TA = +25°C			TA = +85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f _{MAX}	Maximum Toggle Frequency	1100	1400		1100	1400		1100	1400		1100	1400		MHz
t _{PLH} t _{PHL}	Propagation Delay to Output CLK MR	436 479		534 586	471 512		575 623	494 534		602 649	553 591		670 715	ps ps
t _S	Setup Time, D	0	-175		0	-175		0	-175		0	-175		ps
t _H	Hold Time, D	350	175		350	175		350	175		350	175		ps
t _{RR}	Reset Recovery Time	750	550		750	550		750	550	750	550			ps
t _{PW}	Minimum Pulse Width CLK, MR	400			400			400			400			ps
t _{skew}	Within-Device Skew		65			65			65			65		ps
t _r , t _f	Output Rise/Fall Times (20% to 80%)	187		561	193		531	197		494	209		417	ps

Notes:

- 10EL circuits are designed to meet the DC specifications shown in the table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained. Outputs are terminated through a 50Ω resistor to V_{CC} - 2.0V.
- 100K circuits are designed to meet the DC specification shown in the table where transverse airflow greater than 500 lfpm is maintained.
- For standard ECL DC specifications, refer to the ECL Logic Family Standard DC Specification Data Sheet.
- For part ordering description, see HPP Part Ordering Information Data Sheet.

HIGH-PERFORMANCE PRODUCTS**Ordering Information**

Ordering Code	Package ID	Temperature Range
SK10E151PJ	28-PLCC	Industrial
SK10E151PJT	28-PLCC	Industrial
SK100E151PJ	28-PLCC	Industrial
SK100E151PJT	28-PLCC	Industrial

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