Preliminary Information

October 4, 1999

This document contains information on a new product. The parametric information, although not fully characterized, is the result of testing initial devices.

Features

- 100 ps Part-to-Part Skew
- 35 ps Output-to-Output Skew
- Differential Design
- VBB Output
- Low Voltage VEE Range of –2.375 to –3.8V for ECL
- Low Voltage VCC Range of +2.375 to +3.8V for PECL and HSTL
- 75 KΩ Input Pulldown Resistors
- ECL/PECL Outputs

Description

The SK100EP111 is a low skew 1-to-10 diffferential driver, designed with clock distribution in mind. It accepts two clock sources into an input multiplexer. The ECL/PECL input signals can be either differential or single-ended if the VBB output is used. HSTL inputs can be used when the EP111 is operating under PECL conditions. The selected signal is fanned out to 10 identical differential outputs.

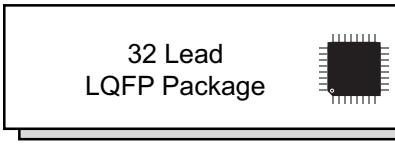
The SK100EP111 is specifically designed, modeled, and produced with low skew as the key goal. Optimal design and layout serve to minimize gate-to-gate skew within a device, and characterization is used to determine process control limits that ensure consistent tpd distributions from lot to lot. The net result is a dependable, guaranteed low skew device.

To ensure that the tight skew specification is met, it is necessary that both sides of the differential output are terminated into 50Ω, even if only one side is being used. In most applications, all ten differential pairs will be used and therefore terminated. In the case where fewer than ten pairs are used, it is necessary to terminate at least the output pairs on the same package side as the pair(s) being used on that side in order to maintain minimum skew. Failure to do this will result in small degradations of propagation delay (on the order of 10–20 ps) of the output(s) being used which, while not being catastrophic to most designs, will mean a loss of skew margin.

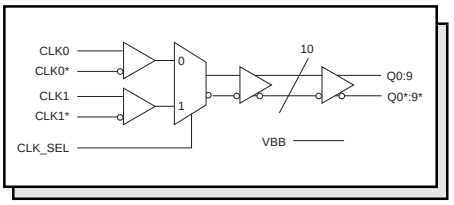
The SK100EP111, as with most other ECL devices, can be operated from a positive VCC supply in PECL mode. This allows the EP111 to be used for high performance clock distribution in +3.3V or +2.5V systems. Designers can take advantage of the EP111's performance to distribute low skew clocks across the backplane or the board. In a PECL environment, series or Thevenin line terminations are typically used as they require no additional power supplies.

Low-Voltage 1:10
Differential ECL/PECL/HSTL
Clock Driver

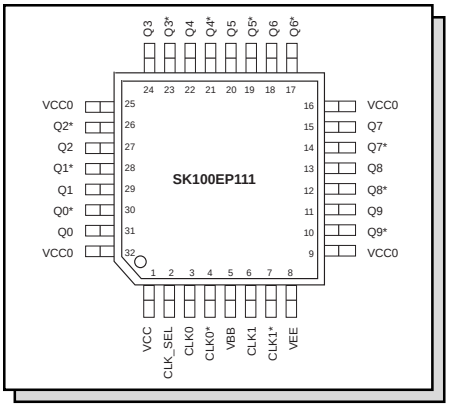
32 Lead
LQFP Package



Logic Symbol



Pinout



Pin Names

Pin	Function
CLK0, CLK0*	Differential ECL/PECL Input Pair
CLK1, CKL1*	Differential HSTL Input Pair
Q0:9, Q0*:9*	Differential PECL Outputs
CLK_SEL	Active Clock Select Input
VBB	VBB Output

Function

CLK_SEL	Active Input
0	CLK0, CLK0*
1	CLK1, CLK1*

ECL DC Characteristics

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage	-1.140	-1.005	-0.880	-1.080	-0.955	-0.880	-1.080		-0.880	-1.080	-0.955	-0.880	V
V_{OL}	Output LOW Voltage	-1.830	-1.695	-1.555	-1.810	-1.705	-1.620	-1.810		-1.620	-1.810	-1.705	-1.620	V
V_{IH}	Input HIGH Voltage	-1.165			-1.165		-0.880	-1.165		-0.880	-1.165		-0.880	V
V_{IL}	Input LOW Voltage	-1.810		-1.475	-1.810		-1.475	-1.810		-1.475	-1.810		-1.475	V
V_{BB}	Output Reference Voltage	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	V
V_{EE}	Power Supply Voltage	-2.375		-3.8	-2.375		-3.8	-2.375		-3.8	-2.375		-3.8	V
I_{IH}	Input High Current			150			150			150			150	µA
I_{EE}	Power Supply Current VEE = -2.375 to -3.8V		80	108		80	108		80	108		80	117	mA
V_{CMR}	Common Mode Range	VEE + 1.7		VCC - 0.3	VEE + 1.7		VCC - 0.3	VEE + 1.7		VCC - 0.3	VEE + 1.7		VCC - 0.3	V
V_{PP}	Minimum Input Swing	500			500			500			500			mV

HSTL DC Characteristics

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{CMR}	Common Mode Range	VEE + 0.9		VCC - 1.1	VEE + 0.9		VCC - 1.1	VEE + 0.9		VCC - 1.1	VEE + 0.9		VCC - 1.1	V
V_{PP}	Minimum Input Swing	500			500			500			500			mV

PECL DC Characteristics

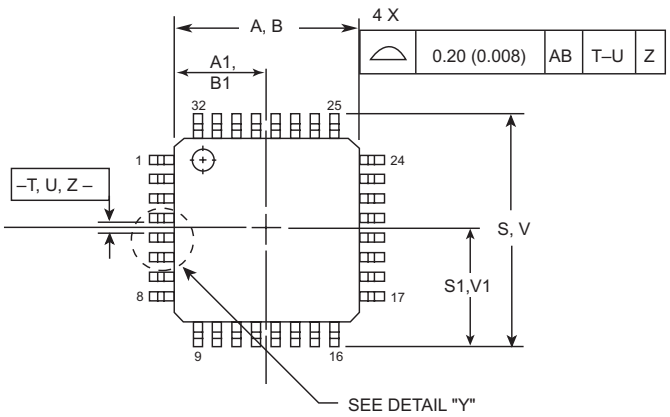
Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage (Note 1)	2.160	2.295	2.420	2.220		2.420	2.220		2.420	2.220	2.345	2.420	V
V_{OL}	Output LOW Voltage (Note 1)	1.470		1.750	1.490		1.680	1.490		1.680	1.490	1.595	1.680	V
V_{IH}	Input HIGH Voltage (Note 1)	2.135		2.420	2.135		2.420	2.135		2.420	2.135		2.420	V
V_{IL}	Input LOW Voltage (Note 1)	1.490		1.825	1.490		1.825	1.490		1.825	1.490		1.825	V
V_{BB}	Output Reference Voltage (Note 1)	1.92		2.04	1.92		2.04	1.92		2.04	1.92		2.04	V
V_{EE}	Power Supply Voltage	2.375		3.8	2.375		3.8	2.375		3.8	2.375		3.8	V
I_{IH}	Input HIGH Current			150			150			150			150	µA
I_{EE}	Power Supply Current VCC = +2.375 to +3.8V		60	70		70	80		70	80		80	117	mA
V_{CMR}	Common Mode Range	VEE + 1.7		VCC - 0.3	VEE + 1.7		VCC - 0.3	VEE + 1.7		VCC - 0.3	VEE + 1.7		VCC - 0.3	V
V_{PP}	Minimum Input Swing	500			500			500			500			mV

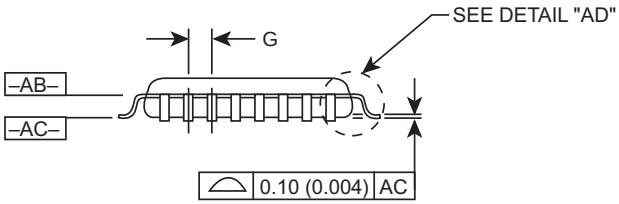
Note 1: These values are for V_{CC} = 3.3V. Level Specifications will vary 1:1 with V_{CC}.

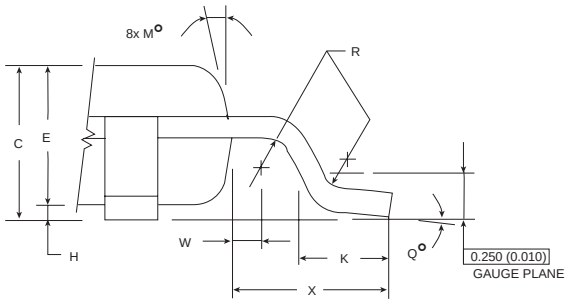
AC Characteristics (V_{EE} = –2.375V to –3.8V; V_{CC} = V_{CC0} = GND)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PLH}	ECL/PECL Prop Delay to Output	310 390	380 440	450 480	350 410	415 460	475 500	375 430	445 480	510 520	480 460	575 550	680 550	ps ps
t_{PHL}	HSTL Prop Delay to Output	340 580	415 610	485 630	380 620	450 650	510 670	410 640	480 670	545 700	520 670	615 700	720 730	ps ps
t_{skew}	Within-Device Skew		15	30		15	30		15	30		15	30	ps
	Part-to-Part Skew		100	145		100	130		100	135		100	150	ps
f_{max}	Max Input Frequency		1500			1500			1500			1500		MHz
t_r, t_f	Output Rise/Fall Time	200		600	200		600	200		600	200		600	ps

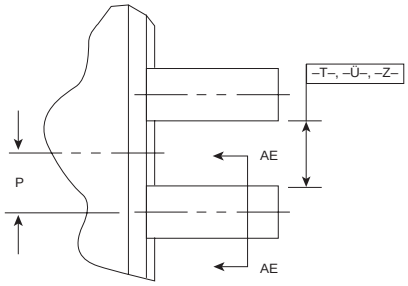
Package Information



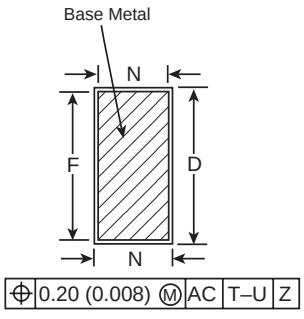




DETAIL AD



DETAIL Y



SECTION AE

NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M, 1982.
2. Controlling Dimension: Millimeter
3. Datum Plane –AB– is located at bottom of lead and is coincident with the lead where the lead exits the plastic body at the bottom of the parting line.
4. Datums –T–, –U–, and –Z– to be determined at Datum Plane –AB–.
5. Dimensions S and V to be determined at Seating Plane –AC–.
6. Dimensions A and B do not include mold protrusion. Allowable protrusion is 0.250 (0.010) per side. Dimensions A and B do not include mold mismatch and are determined at Datum Plane –AB–.
7. Dimension D does not include Dambar protrusion. Dambar protrusion shall not cause the D dimension to exceed 0.520 (0.020).
8. Minimum solder plate thickness shall be 0.0075 (0.0003).
9. Exact shape of each corner may vary from depiction.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	