

## Preliminary Information

October 4, 1999

This document contains information on a new product. The parametric information, although not fully characterized, is the result of testing initial devices.

## Features

- 100 ps Part-to-Part Skew
- 35 ps Output-to-Output Skew
- Differential Design
- VBB Output
- Low Voltage VEE Range of  $-2.375$  to  $-3.8V$  for ECL
- Low Voltage VCC Range of  $+2.375$  to  $+3.8V$  for PECL and HSTL
- 75 K $\Omega$  Input Pulldown Resistors
- ECL/PECL Outputs

## Description

The SK10EP111 is a low skew 1-to-10 differential driver, designed with clock distribution in mind. It accepts two clock sources into an input multiplexer. The ECL/PECL input signals can be either differential or single-ended if the VBB output is used. HSTL inputs can be used when the EP111 is operating under PECL conditions. The selected signal is fanned out to 10 identical differential outputs.


The SK10EP111 is specifically designed, modeled, and produced with low skew as the key goal. Optimal design and layout serve to minimize gate-to-gate skew within a device, and characterization is used to determine process control limits that ensure consistent tpd distributions from lot to lot. The net result is a dependable, guaranteed low skew device.

To ensure that the tight skew specification is met, it is necessary that both sides of the differential output are terminated into 50 $\Omega$ , even if only one side is being used. In most applications, all ten differential pairs will be used and therefore terminated. In the case where fewer than ten pairs are used, it is necessary to terminate at least the output pairs on the same package side as the pair(s) being used on that side in order to maintain minimum skew. Failure to do this will result in small degradations of propagation delay (on the order of 10–20 ps) of the output(s) being used which, while not being catastrophic to most designs, will mean a loss of skew margin.

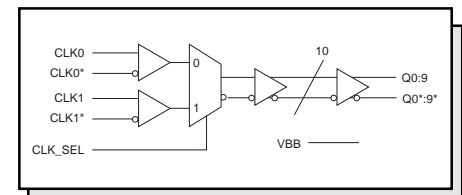
The SK10EP111, as with most other ECL devices, can be operated from a positive VCC supply in PECL mode. This allows the EP111 to be used for high performance clock distribution in +3.3V or +2.5V systems. Designers can take advantage of the EP111's performance to distribute low skew clocks across the backplane or the board. In a PECL environment, series or Thevenin line terminations are typically used as they require no additional power supplies.

Low-Voltage 1:10  
Differential ECL/PECL/HSTL  
Clock Driver

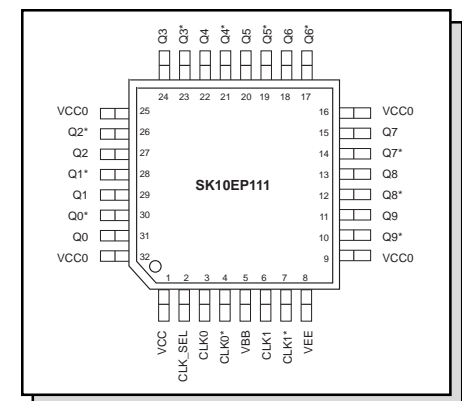
32 Lead  
LQFP Package



## Logic Symbol



## Pinout



## Pin Names

Pin	Function
CLK0, CLK0*	Differential ECL/PECL Input Pair
CLK1, CLK1*	Differential HSTL Input Pair
Q0:9, Q0*:9*	Differential PECL Outputs
CLK_SEL	Active Clock Select Input
VBB	VBB Output

## Function

CLK_SEL	Active Input
0	CLK0, CLK0*
1	CLK1, CLK1*

**ECL DC Characteristics**

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V <sub>OH</sub>	Output HIGH Voltage	-1135		-890	-1080		-840	-1020		-810	-910		-720	mV
V <sub>OL</sub>	Output LOW Voltage	-1950		-1650	-1950		-1630	-1950		-1630	-1950		-1595	mV
V <sub>IH</sub>	Input HIGH Voltage	-1230		-890	-1170		-840	-1130		-810	-1060		-720	mV
V <sub>IL</sub>	Input LOW Voltage	-1950		-1500	-1950		-1480	-1950		-1480	-1950		-1445	mV
V <sub>BB</sub>	Output Reference Voltage	-1.43		-1.30	-1.38		-1.27	-1.35		-1.25	-1.31		-1.19	V
V <sub>EE</sub>	Power Supply Voltage	-2.375		-3.8	-2.375		-3.8	-2.375		-3.8	-2.375		-3.8	V
I <sub>IH</sub>	Input HIGH Current			150			150			150			150	μA
I <sub>EE</sub>	Power Supply Current V <sub>EE</sub> = -2.375 to -3.8V		80	108		80	108		80	108		80	108	mA
V <sub>CMR</sub>	Common Mode Range	V <sub>EE</sub> + 1.7		V <sub>CC</sub> - 0.3	V <sub>EE</sub> + 1.7		V <sub>CC</sub> - 0.3	V <sub>EE</sub> + 1.7		V <sub>CC</sub> - 0.3	V <sub>EE</sub> + 1.7		V <sub>CC</sub> - 0.3	V
V <sub>PP</sub>	Minimum Input Swing	500			500			500			500			mV

**HSTL DC Characteristics**

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V <sub>CMR</sub>	Common Mode Range	V <sub>EE</sub> + 0.9		V <sub>CC</sub> - 1.1	V <sub>EE</sub> + 0.9		V <sub>CC</sub> - 1.1	V <sub>EE</sub> + 0.9		V <sub>CC</sub> - 1.1	V <sub>EE</sub> + 0.9		V <sub>CC</sub> - 1.1	V
V <sub>PP</sub>	Minimum Input Swing	500			500			500			500			mV

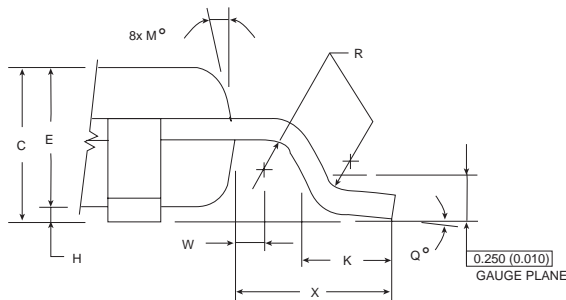
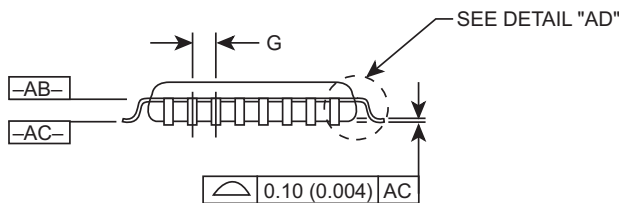
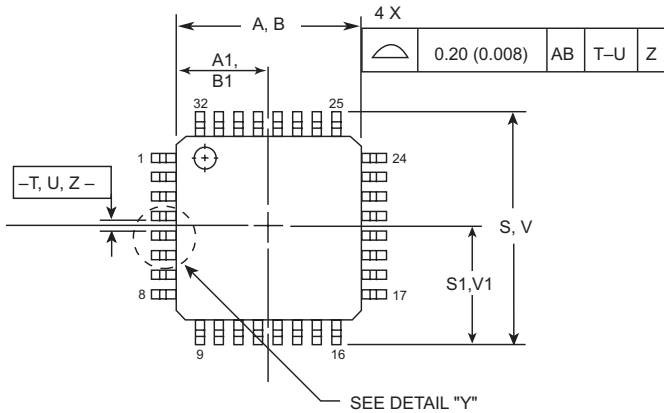
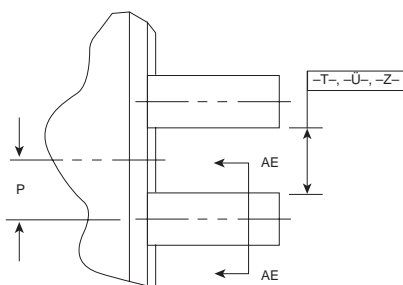
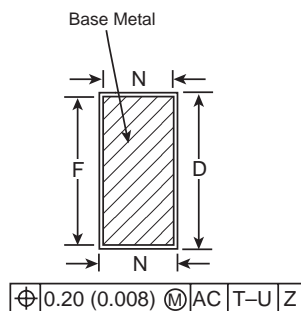
**PECL DC Characteristics**

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V <sub>OH</sub>	Output HIGH Voltage (Note 1)	2165		3210	2220		2420	2280		2490	2390		2580	mV
V <sub>OL</sub>	Output LOW Voltage (Note 1)	1350		1650	1350		1670	1350		1670	1350		1705	mV
V <sub>IH</sub>	Input HIGH Voltage (Note 1)	2670		2410	2130		2460	2170		2410	2240		2580	mV
V <sub>IL</sub>	Input LOW Voltage (Note 1)	1350		1800	1350		1820	1350		1820	1350		1855	mV
V <sub>BB</sub>	Output Reference Voltage (Note 1)	1.87		2.00	1.92		2.03	1.95		2.05	1.99		2.11	V
V <sub>EE</sub>	Power Supply Voltage	2.375		3.8	2.375		3.8	2.375		3.8	2.375		3.8	V
I <sub>IH</sub>	Input HIGH Current			150			150			150			150	μA
I <sub>EE</sub>	Power Supply Current V <sub>CC</sub> = +2.375 to +3.8V		80	108		80	108		80	108		80	108	mA
V <sub>CMR</sub>	Common Mode Range	V <sub>EE</sub> + 1.7		V <sub>CC</sub> - 0.3	V <sub>EE</sub> + 1.7		V <sub>CC</sub> - 0.3	V <sub>EE</sub> + 1.7		V <sub>CC</sub> - 0.3	V <sub>EE</sub> + 1.7		V <sub>CC</sub> - 0.3	V
V <sub>PP</sub>	Minimum Input Swing	500			500			500			500			mV

Note 1: These values are for V<sub>CC</sub> = 3.3V. Level Specifications will vary 1:1 with V<sub>CC</sub>.

**AC Characteristics** (V<sub>EE</sub> = -2.375V to -3.8V; V<sub>CC</sub> = V<sub>CC0</sub> = GND)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t <sub>PLH</sub>	ECL/PECL Prop Delay to Output	310 390	380 420	450 440	350 405	415 440	475 460	375 430	445 460	510 490	480 460	575 490	680 520	ps ps
t <sub>PHL</sub>	HSTL Prop Delay to Output	340 550	415 580	485 600	380 585	450 620	510 640	410 610	480 640	545 670	520 640	615 670	720 700	ps ps
t <sub>skew</sub>	Within-Device Skew		15	30		15	30		15	30		15	30	ps
	Part-to-Part Skew		100	145		100	130		100	135		100	150	ps
f <sub>max</sub>	Max Input Frequency		1500			1500			1500			1500		MHz
t <sub>r</sub> , t <sub>f</sub>	Output Rise/Fall Time	200		600	200		600	200		600	200		600	ps

**Package Information**

**DETAIL AD**

**DETAIL Y**

**SECTION AE**
**NOTES:**

1. Dimensioning and tolerancing per ANSI Y14.5M, 1982.
2. Controlling Dimension: Millimeter
3. Datum Plane -AB- is located at bottom of lead and is coincident with the lead where the lead exits the plastic body at the bottom of the parting line.
4. Datums -T-, -U-, and -Z- to be determined at Datum Plane -AB-.
5. Dimensions S and V to be determined at Seating Plane -AC-.
6. Dimensions A and B do not include mold protrusion. Allowable protrusion is 0.250 (0.010) per side. Dimensions A and B do not include mold mismatch and are determined at Datum Plane -AB-.
7. Dimension D does not include Dambar protrusion. Dambar protrusion shall not cause the D dimension to exceed 0.520 (0.020).
8. Minimum solder plate thickness shall be 0.0075 (0.0003).
9. Exact shape of each corner may vary from depiction.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	7.000	BSC	0.276	BSC
A1	3.500	BSC	0.138	BSC
B	7.000	BSC	0.276	BSC
B1	3.500	BSC	0.138	BSC
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800	BSC	0.031	BSC
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400	BSC	0.016	BSC
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000	BSC	0.354	BSC
S1	4.500	BSC	0.177	BSC
V	9.000	BSC	0.354	BSC
V1	4.500	BSC	0.177	BSC
W	0.200	REF	0.008	REF
X	1.000	REF	0.039	REF