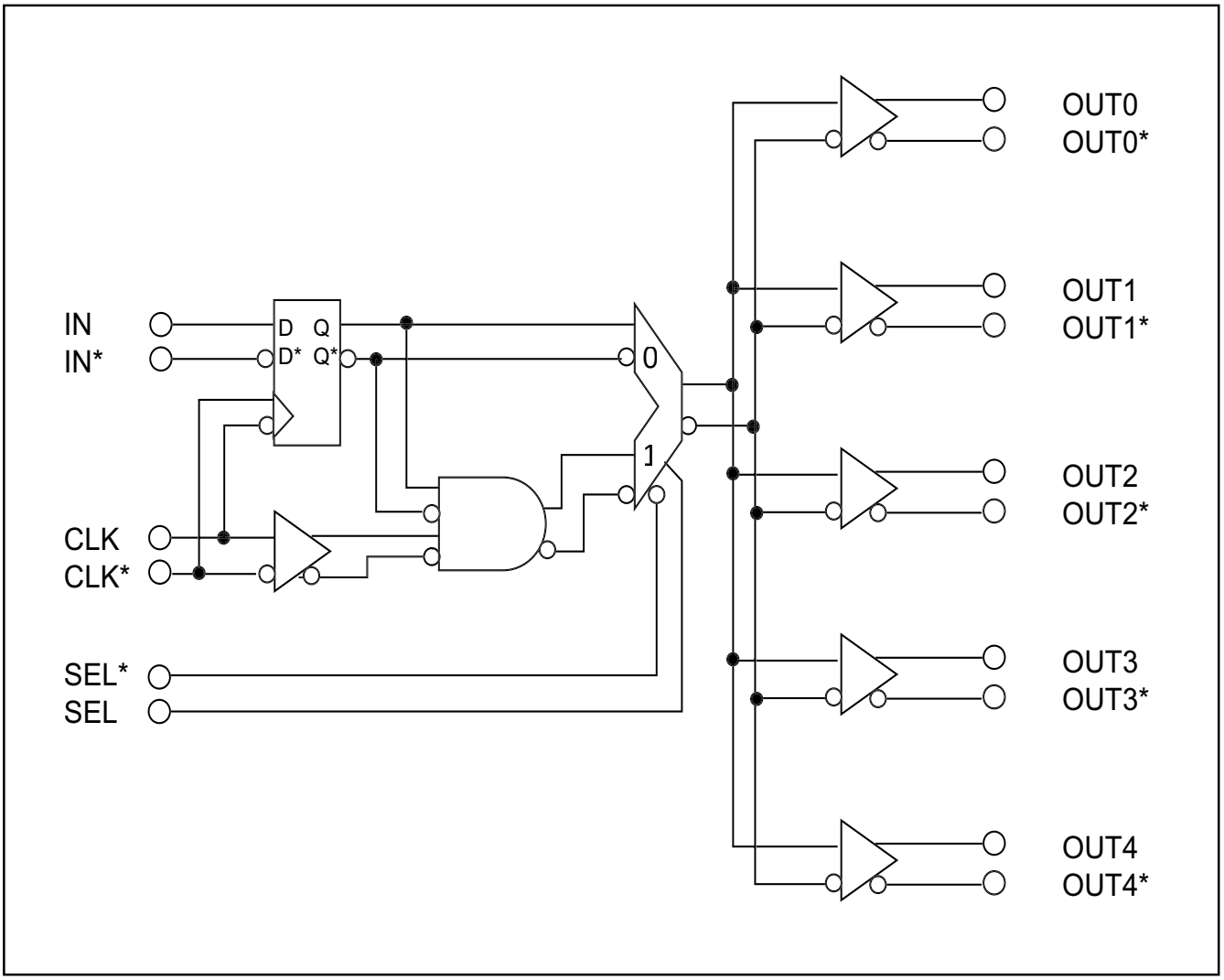
SK15XX Family
1:5 Signal Distribution

PRELIMINARY

SK15XX Family Functional Block Diagram



SK15XX Family Product Selection Guide

1:5 Signal Distribution	*3 GHz*	*Synch / Asynch Operation*

Logic Family

	Power Supply		Output Configuration				Output	Availability
Product	**3.3V**	**5.2V**	**Open Emitter**	**50Ω Double Termination**	**50Ω Source Termination**	**Internal Current Sink (Double Termination)**		
SK1500	●	●	●				ECL / PECL	Now
SK1501		●	●				Double Swing / TTL	Now
SK1502	●	●		●			ECL / PECL	Now
SK1503	●	●				●	ECL / PECL	Now
SK1504	●	●			●		ECL / PECL	Now

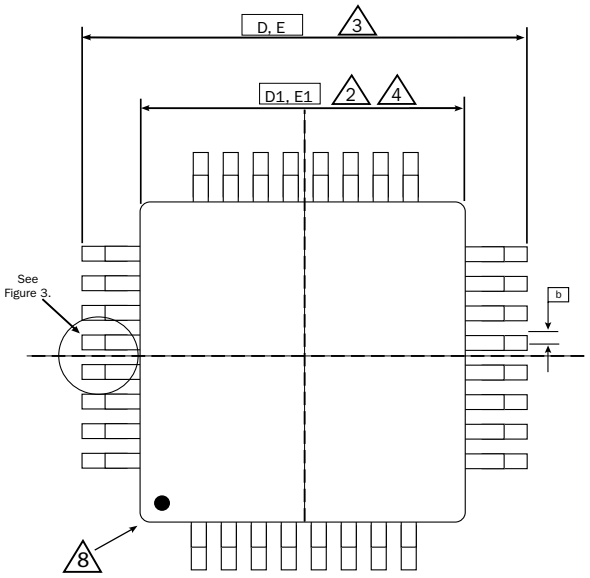
Logic / Translation Family

	Translation	Output Configuration			Availability
Product		Open Emitter	50Ω Double Termination	50Ω Source Termination	
SK1525	Anything to PECL	●			Now
SK1526	Anything to ECL	●			Now
SK1527	Anything to PECL		●		Now
SK1528	Anything to ECL		●		Now
SK1529	Anything to PECL			●	Now
SK1530	Anything to ECL			●	Now

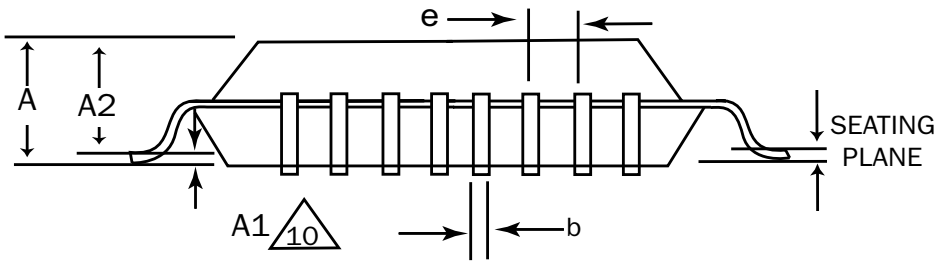
Open Collector Logic Family

	Output Configuration	Output Current	Availability
Product	**Open Collector**		
SK1599	●	12 mA	Q2 2001

SK15XX Family Package Information
5mm x 5mm TQFP



Top View



Side View

SK15XX Family Package Information (continued)
5mm x 5mm TQFP

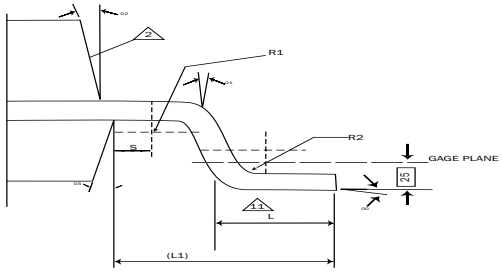


Figure 1.

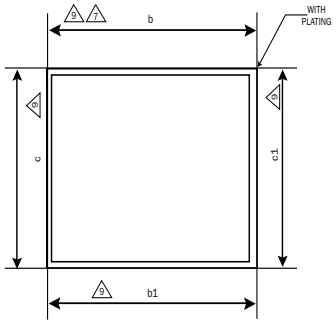


Figure 2.

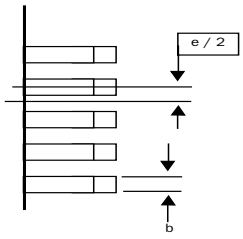


Figure 3.

1. All dimensions and tolerancing conforms to ANSI Y14.5M-1982.
2. The top package body size may be smaller than the bottom package body size by as much as 0.15 mm.
3. To be determined at seating plane.
4. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
5. Details of Pin 1 identifier optional, but must be located within the zone indicated.
6. All dimensions are in millimeters.
7. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
8. Exact shape of each corner is optional.
9. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
10. A1 is defined as the distance from the seating plane to the lowest point of the package body.

JEDEC Variation All Dimensions in Millimeters					
Symbol	**MIN**	**NOM**	**MAX**	**Note**	**Comments**
A	1.00	1.10	1.20		Package Stand Off Height
A1	0.05	0.10	0.15		Air Gap
A2	0.95	1.00	1.05		Package Body Thickness
D		7.00 BSC		3	
D1		5.00 BSC		4, 2	Package Body Length
E		7.00 BSC		3	
E1		5.00 BSC		4, 2	Package Body Width
N		32			Lead Count
e		0.50 BSC			Lead Pitch
b	0.17	0.22	0.27	7	Lead Thickness
b1	0.17	0.20	0.23		
R1	0.08	–	–		
R2	0.08	–	0.20		
00	0°	3.5°	7°		
01	0°	–	–		
02	11°	12°	13°		
03	11°	12°	13°		
S	0.20	–	–		
c	0.09	–	0.20		
c1	0.09	–	0.16		
L	0.45	0.60	0.75		
L1		1.00 REF			
aaa		0.20			
bbb		0.20			
ccc		0.08			
ddd		0.08			

Absolute Maximum Ratings*

Symbol	Parameter	Value	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	-6.0 to 0	V
V_{CC}	Power Supply (V_{EE} = 0V)	6.0 to 0	V
V_I	Input Voltage (V_{CC} = 0V, V_I not more negative than V_{EE})	-6.0 to 0	V
V_I	Input Voltage (V_E = 0V, V_I not more positive than V_{CC})	6.0 to 0	V
I_{OUT}	Output Current Continuous Surge	 50 100	 mA mA
T_A	Operating Temperature Range	0 to +70	°C
T_{stg}	Storage Temperature	-65 to +150	°C
T_{sol}	Solder Temperature (<2 to 3 seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

Description

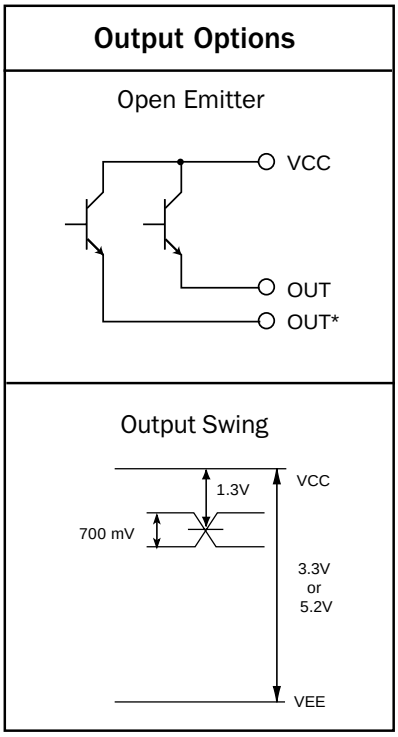
The SK1500 is an extremely fast, stable, and accurate low skew 1:5 clock / signal distributor featuring a synchronous enable, which allows the outputs to be turned off and on without the risk of an unpredictable output pulse. The D - flip-flop is triggered on the falling edge of the clock.

The SK1500 uses standard open emitter ECL outputs optimized for:

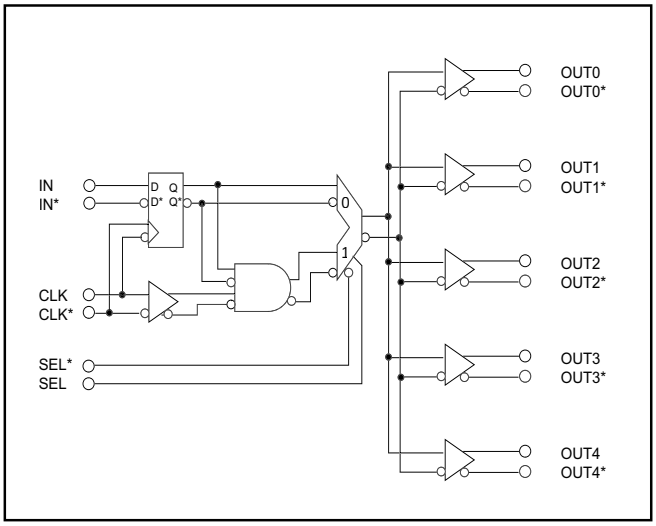
- General purpose ECL compatible applications
- Multiple destination applications (daisy chain).

Features

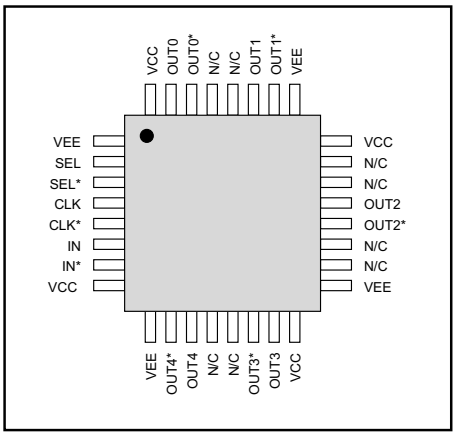
- 1:5 Clock/Data Driver
- 3 GHz Fmax
- 3.3V / 5.2V Compatible



Functional Block Diagram



Pin Description



Package Information

32 pin, 5 mm x 5 mm
TQFP Package

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High Input Low	VIH VIL	VEE + 2.0 VEE		VCC VCC - .2	V V
(IN - IN*, CLK - CLK*, SEL - SEL*) Differential Input Voltage (Note 1)	| Input - Input* |	.2		4.3	V
Timing Inputs (CLK / CLK*) Input High Current Input Low Current	 IIH IIL	 +1 -1		 +25 +1	 µA µA
Functional Inputs (IN / IN*, SEL / SEL*) Input Current	IIH, IIL	-420		+250	µA
Outputs					
Digital Output Voltage Output Common Mode Range	| OUT - OUT* | (OUT + OUT*) / 2	600 VCC - 1.5	700 VCC - 1.3	 VCC - 1.1	mV V
Power Supply					
Power Supply Current Power Supply Voltage	IEE VCC - VEE	 3.0	95	120 5.5	mA V

Test Conditions: Outputs terminated with 50Ω to VCC – 2V.
Note 1: Production tested to a maximum V_{diff} = 2.0V.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay CLK to OUT (SEL = 0) CLK to OUT (SEL = 1) SEL to OUT	 Tpd Tpd Tpd	 490 340 330	 590 440 430	 690 540 530	 ps ps ps
Channel to Channel Skew				<20	ps
Maximum Operating Frequency (Note 1)	Fmax	3.0			GHz
Minimum Pulse Width (Note 1)	PW min	160			ps
IN to CLK (Note 1) Set Up Time Hold Time	 Tsu Th	 100 100			 ps ps
Output Rise and Fall Times (20% / 80%)	Tr / Tf		125	150	ps
Temperature Coefficient	ΔTpd /ΔT		<1		ps / ^{o}C

Note 1: Guaranteed by characterization. Not production tested.

Description

The SK1501 is an extremely fast, stable, and accurate low skew 1:5 clock / signal distributor featuring a synchronous enable, which allows the outputs to be turned off and on without the risk of an unpredictable output pulse. The D - flip-flop is triggered on the falling edge of the clock.

The SK1501 uses open emitter outputs with a double amplitude swing suitable for the following applications:

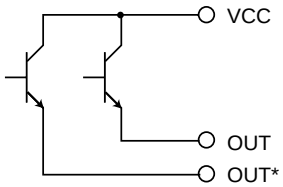
- TTL compatible destinations
- Double termination situations that require a full swing at the destination
- Long cables

Features

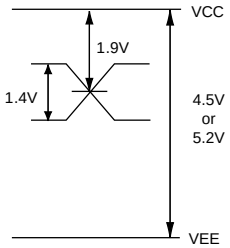
- 1:5 Clock/Data Driver
- 2 GHz Fmax
- 4.5V / 5.2V Compatible

Output Options

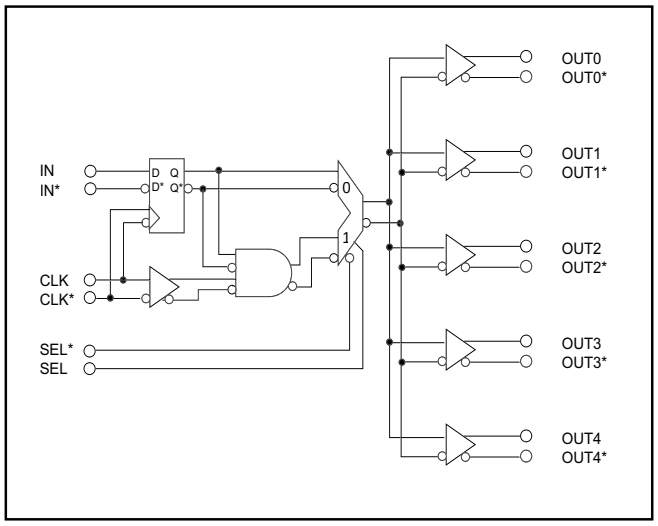
Open Emitter



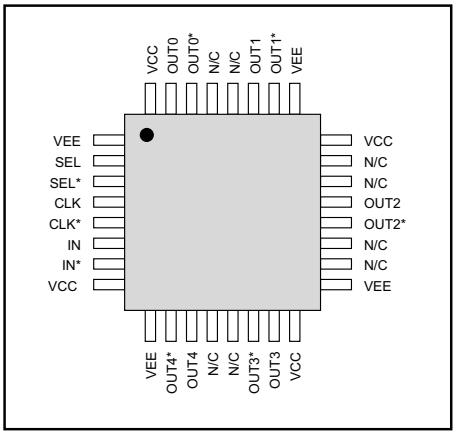
Output Swing



Functional Block Diagram



Pin Description



Package Information

32 pin, 5 mm x 5 mm
TQFP Package

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High Input Low	VIH VIL	VEE + 2.0 VEE		VCC VCC -.2	V V
(IN - IN*, CLK - CLK*, SEL -SEL*) Differential Input Voltage	| Input -Input* |	.2		4.3	V
Timing Inputs (CLK / CLK*) Input High Current Input Low Current	 IIH IIL	 +1 -1		 +25 +1	 µA µA
Functional Inputs (IN / IN*, SEL / SEL*) Input Current	IIH, IIL	-420		+250	µA
Outputs					
Digital Output Voltage Output Common Mode Range	| OUT -OUT* | (OUT + OUT*) / 2	1.2 VCC -2.1	1.4 VCC - 1.9	 VCC - 1.7	V V
Power Supply					
Power Supply Current Power Supply Voltage	IEE VCC -VEE	 4.2	95	120 5.5	mA V

Test Conditions: Outputs terminated with 50Ω to VCC – 3V.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay CLK to OUT (SEL = 0) CLK to OUT (SEL = 1) SEL to OUT	 Tpd Tpd Tpd	 490 340 330	 590 440 430	 690 540 530	 ps ps ps
Channel to Channel Skew				<20	ps
Maximum Operating Frequency (Note 1)	Fmax	2.0			GHz
Minimum Pulse Width (Note 1)	PW min	250			ps
IN to CLK (Note 1) Set Up Time Hold Time	 Tsu Th	 100 100			 ps ps
Output Rise and Fall Times (20% / 80%)	Tr / Tf		200	250	ps
Temperature Coefficient	ΔTpd /ΔT		<1		ps / °C

Note 1: Guaranteed by characterization. Not production tested.

Description

The SK1502 is an extremely fast, stable, and accurate low skew 1:5 clock / signal distributor featuring a synchronous enable, which allows the outputs to be turned off and on without the risk of an unpredictable output pulse. The D - flip-flop is triggered on the falling edge of the clock.

The SK1502 uses 50Ω outputs with source /sink capability, and is optimized for applications that require:

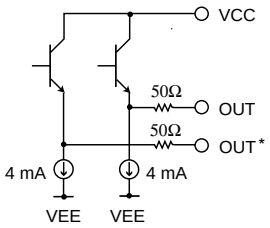
- Point to point, double terminated, timing critical lines

Features

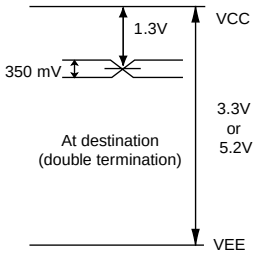
- 1:5 Clock/Data Driver
- 3 GHz Fmax
- 3.3V / 5.2V Compatible

Output Options

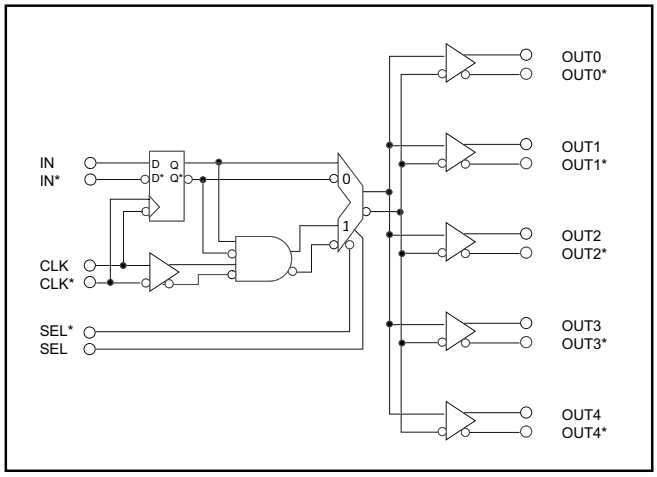
50Ω Source / Sink



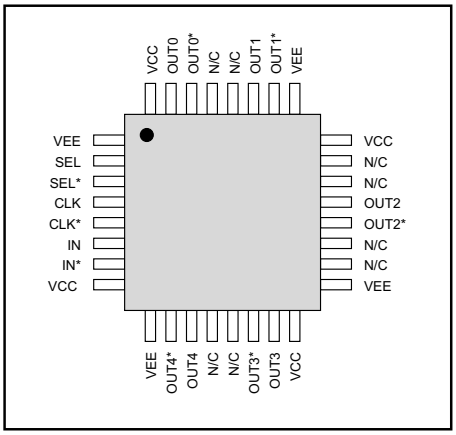
Output Swing



Functional Block Diagram



Pin Description



Package Information

32 pin, 5 mm x 5 mm
TQFP Package

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High Input Low	VIH VIL	VEE + 2.0 VEE		VCC VCC - .2	V V
(IN - IN*, CLK - CLK*, SEL - SEL*) Differential Input Voltage	| Input - Input* |	.2		4.3	V
Timing Inputs (CLK / CLK*) Input High Current Input Low Current	 IIH IIL	 +1 -1		 +25 +1	 µA µA
Functional Inputs (IN / IN*, SEL / SEL*) Input Current	IIH, IIL	-420		+250	µA
Outputs					
Digital Output Voltage Output Common Mode Range Internal Current Source Output Impedance	| OUT - OUT* | (OUT + OUT*) / 2 ISINK ROUT	600 VCC - 1.5 4 40	700 VCC -1.3 5 45	 VCC - 1.1 6 50	mV V mA Ω
Power Supply					
Power Supply Current Power Supply Voltage	IEE VCC - VEE	 3.0	135	170 5.5	mA V

Test Conditions: Outputs terminated with 50Ω to VCC – 2V.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay CLK to OUT (SEL = 0) CLK to OUT (SEL = 1) SEL to OUT	 Tpd Tpd Tpd	 490 340 330	 590 440 430	 690 540 530	 ps ps ps
Channel to Channel Skew				<20	ps
Maximum Operating Frequency (Note 1)	Fmax	3.0			GHz
Minimum Pulse Width (Note 1)	PW min	160			ps
IN to CLK (Note 1) Set Up Time Hold Time	 Tsu Th	 100 100			 ps ps
Output Rise and Fall Times (20% / 80%)	Tr / Tf		125	150	ps
Temperature Coefficient	DTpd /DT		<1		ps / ^{o}C

Note 1: Guaranteed by characterization. Not production tested.

Description

The SK1503 is an extremely fast, stable, and accurate low skew 1:5 clock / signal distributor featuring a synchronous enable, which allows the outputs to be turned off and on without the risk of an unpredictable output pulse. The D - flip-flop is triggered on the falling edge of the clock.

The SK1503 outputs are open emitter with an internal current source, optimized for applications that are:

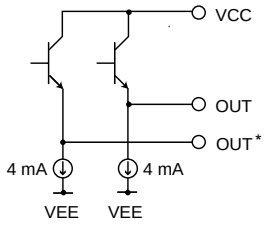
- Point to point, double terminated, timing critical lines
- Non-50Ω transmission lines

Features

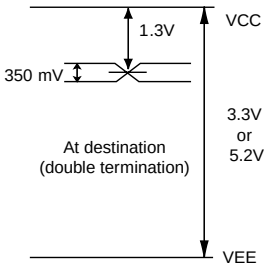
- 1:5 Clock/Data Driver
- 3 GHz Fmax
- 3.3V / 5.2V Compatible

Output Options

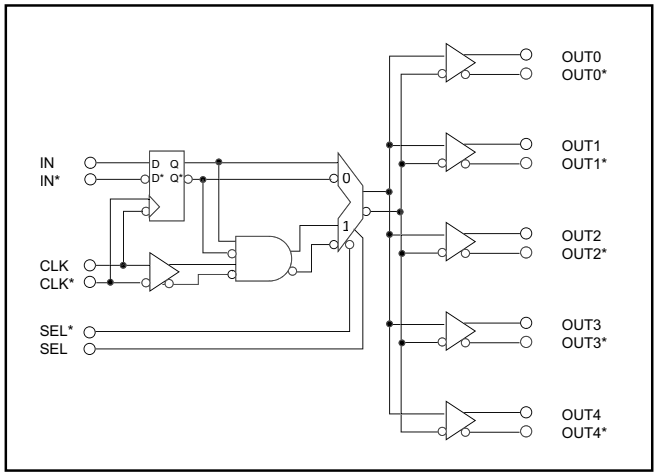
Internal Current Sink



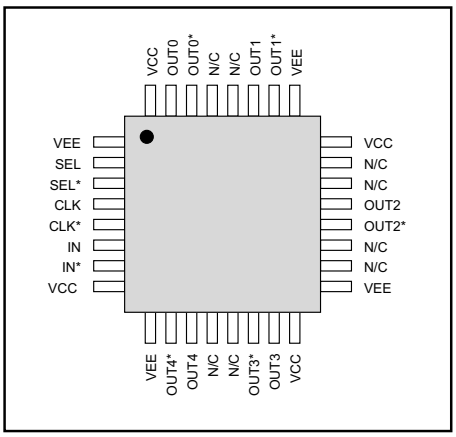
Output Swing



Functional Block Diagram



Pin Description



Package Information

32 pin, 5 mm x 5 mm
TQFP Package

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High Input Low	VIH VIL	VEE + 2.0 VEE		VCC VCC - .2	V V
(IN - IN*, CLK - CLK*, SEL - SEL*) Differential Input Voltage	| Input - Input* |	.2		4.3	V
Timing Inputs (CLK / CLK*) Input High Current Input Low Current	 IIH IIL	 +1 -1		 +25 +1	 µA µA
Functional Inputs (IN / IN*, SEL / SEL*) Input Current	IIH, IIL	-420		+250	µA
Outputs					
Digital Output Voltage Output Common Mode Range Internal Current Source	| OUT - OUT* | (OUT + OUT*) / 2 ISINK	600 VCC - 1.5 4	700 VCC -1.3 5	 VCC - 1.1 6	mV V mA
Power Supply					
Power Supply Current Power Supply Voltage	IEE VCC - VEE	 3.0	135	170 5.5	mA V

Test Conditions:

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay CLK to OUT (SEL = 0) CLK to OUT (SEL = 1) SEL to OUT	 Tpd Tpd Tpd	 490 340 330	 590 440 430	 690 540 530	 ps ps ps
Channel to Channel Skew				<20	ps
Maximum Operating Frequency (Note 1)	Fmax	3.0			GHz
Minimum Pulse Width (Note 1)	PW min	160			ps
IN to CLK (Note 1) Set Up Time Hold Time	 Tsu Th	 100 100			 ps ps
Output Rise and Fall Times (20% / 80%)	Tr / Tf		125	150	ps
Temperature Coefficient	ΔTpd /ΔT		<1		ps / ^{o}C

Note 1: Guaranteed by characterization. Not production tested.

Description

The SK1504 is an extremely fast, stable, and accurate low skew 1:5 clock / signal distributor featuring a synchronous enable, which allows the outputs to be turned off and on without the risk of an unpredictable output pulse. The D - flip-flop is triggered on the falling edge of the clock.

The SK1504 outputs are 50Ω with source and sink capability, optimized for:

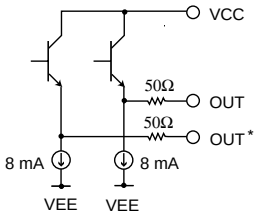
- Point to point, series terminated, timing critical lines

Features

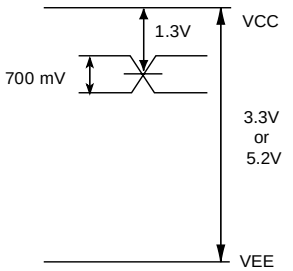
- 1:5 Clock/Data Driver
- 3 GHz Fmax
- 3.3V / 5.2V Compatible

Output Options

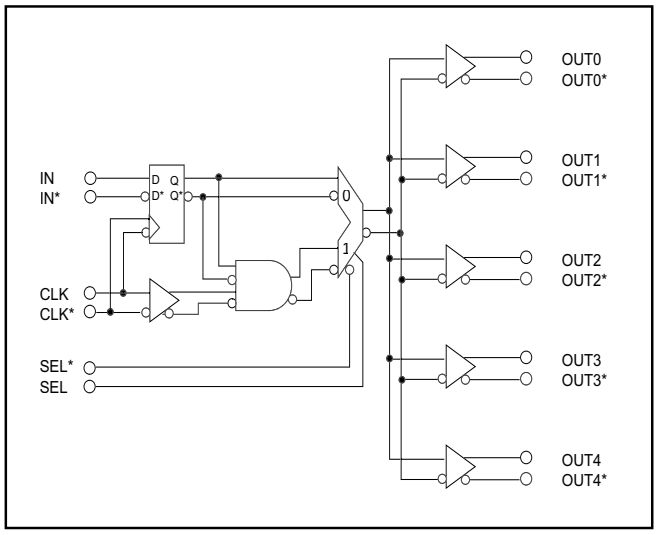
50Ω Source / Sink



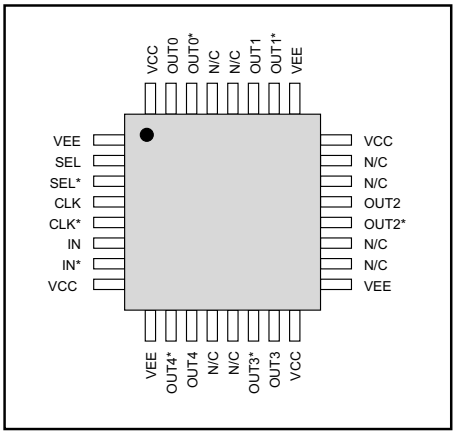
Output Swing



Functional Block Diagram



Pin Description



Package Information

32 pin, 5 mm x 5 mm TQFP Package

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High Input Low	VIH VIL	VEE + 2.0 VEE		VCC VCC - .2	V V
(IN - IN*, CLK - CLK*, SEL - SEL*) Differential Input Voltage	| Input - Input* |	.2		4.3	V
Timing Inputs (CLK / CLK*) Input High Current Input Low Current	 IIH IIL	 +1 -1		 +25 +1	 µA µA
Functional Inputs (IN / IN*, SEL / SEL*) Input Current	IIH, IIL	-420		+250	µA
Outputs					
Digital Output Voltage Output Common Mode Range Internal Current Source Output Impedance	| OUT - OUT* | (OUT + OUT*) / 2 ISINK ROUT	600 VCC - 1.5 6.5 40	700 VCC -1.3 8 45	 VCC - 1.1 10 50	mV V mA Ω
Power Supply					
Power Supply Current Power Supply Voltage	IEE VCC - VEE	 3.0	175	221 5.5	mA V

Test Conditions:

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay CLK to OUT (SEL = 0) CLK to OUT (SEL = 1) SEL to OUT	 Tpd Tpd Tpd	 490 340 330	 590 440 430	 690 540 530	 ps ps ps
Channel to Channel Skew				<20	ps
Maximum Operating Frequency (Note 1)	Fmax	3.0			GHz
Minimum Pulse Width (Note 1)	PW min	160			ps
IN to CLK (Note 1) Set Up Time Hold Time	 Tsu Th	 100 100			 ps ps
Output Rise and Fall Times (20% / 80%)	Tr / Tf		125	150	ps
Temperature Coefficient	ΔTpd /ΔT		<1		ps / ^{o}C

Note 1: Guaranteed by characterization. Not production tested.

Description

The SK1525 is an extremely fast, stable, and accurate low skew 1:5 clock / signal distributor featuring a synchronous enable, which allows the outputs to be turned off and on without the risk of an upredictable output pulse. It is also capable of receiving inputs of any technology or voltage level. The D - flip-flop is triggered on the falling edge of the clock.

The SK1525 has open emitter PECL outputs.

Target applications:

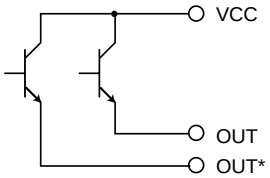
- High speed clock / data lines that require translation
- Multiple destination (daisy chain) applications

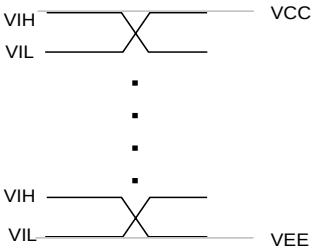
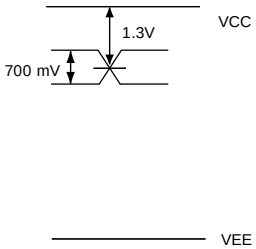
Features

- 1:5 Clock/Data Driver
- 3 GHz Fmax
- Anything to PECL Translation

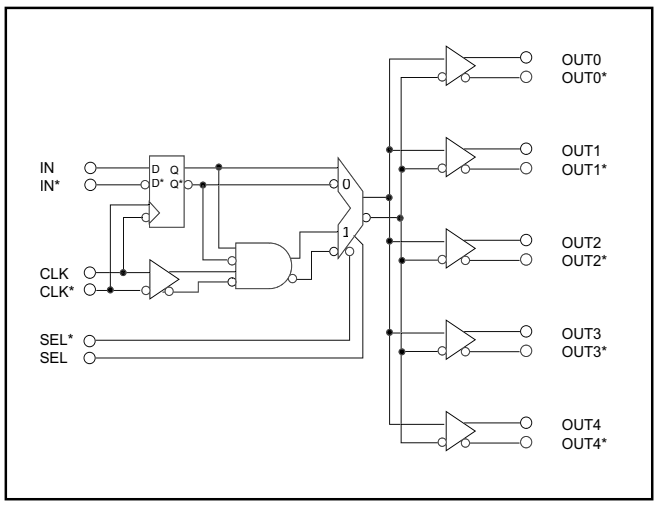
Output Options

Open Emitter

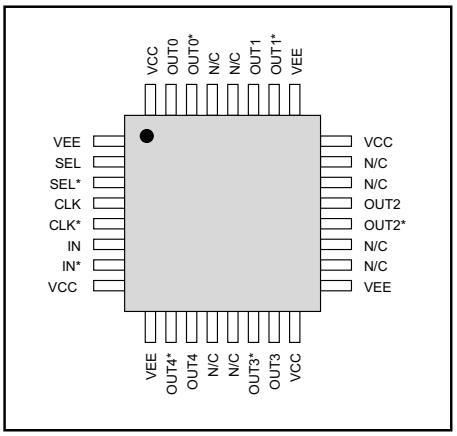


Input Swing	Output Swing
	

Functional Block Diagram



Pin Description



Package Information

32 pin, 5 mm x 5 mm
TQFP Package

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High Input Low	VIH VIL	VEE + 2.0 VEE		VCC VCC -.2	V V
(IN - IN*, CLK - CLK*, SEL -SEL*) Differential Input Voltage	| Input - Input* |	.2		4.3	V
Timing Inputs (CLK / CLK*) Input High Current Input Low Current	 IIH IIL	 +1 -1		 +25 +1	 µA µA
Functional Inputs (IN / IN*, SEL / SEL*) Input Current	 IIH, IIL	 -420		 +250	 µA
Outputs					
Digital Output Voltage Output Common Mode Range	| OUT -OUT* | (OUT + OUT*) / 2	600 VCC -1.5	700 VCC -1.3	 VCC -1.1	mV V
Power Supply					
Power Supply Current Positive Supply Voltage Negative Supply Voltage	IEE VCC VEE	 3.0 -3.6	95 3.3 -3.3	120 3.6 -3.0	mA V V

Test Conditions: Outputs terminated with 50Ω to VCC – 2V.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay CLK to OUT (SEL = 0) CLK to OUT (SEL = 1) SEL to OUT	 Tpd Tpd Tpd	 490 340 330	 590 440 430	 690 540 530	 ps ps ps
Channel to Channel Skew				<20	ps
Maximum Operating Frequency (Note 1)	Fmax	3.0			GHz
Minimum Pulse Width (Note 1)	PW min	160			ps
IN to CLK (Note 1) Set Up Time Hold Time	 Tsu Th	 100 100			 ps ps
Output Rise and Fall Times (20% / 80%)	Tr / Tf		125	150	ps
Temperature Coefficient	ΔTpd /ΔT		<1		ps / ^{o}C

Note 1: Guaranteed by characterization. Not production tested.

Description

The SK1526 is an extremely fast, stable and accurate low skew 1:5 clock / signal distributor featuring a synchronous enable, which allows the outputs to be turned off and on without the risk of an upredictable output pulse. It is also capable of receiving inputs of any technology or voltage level. The D - flip-flop is triggered on the falling edge of the clock.

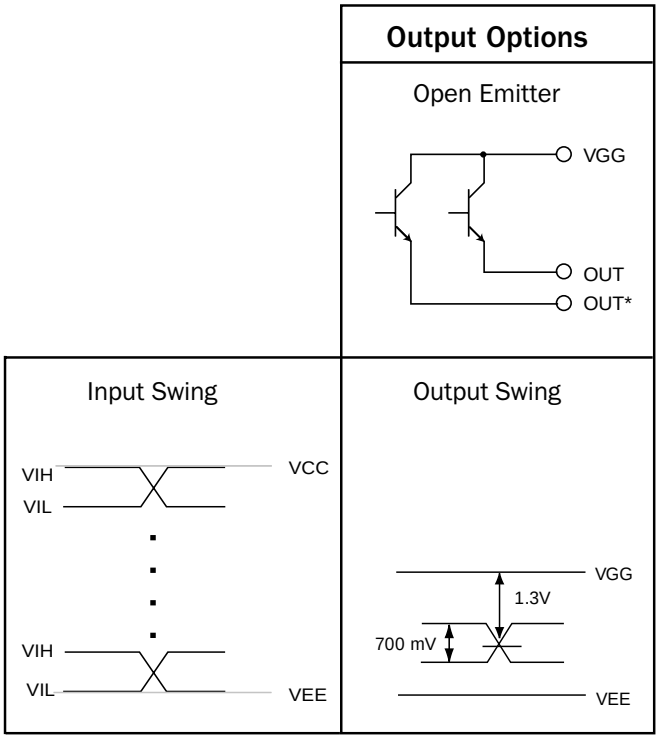
The SK1526 has standard open emitter ECL outputs.

Target applications:

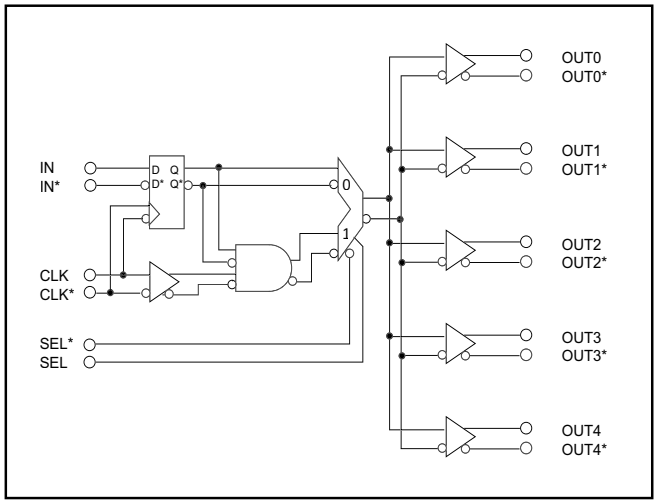
- High speed clock / data lines that require translation
- Multiple destination (daisy chain) applications

Features

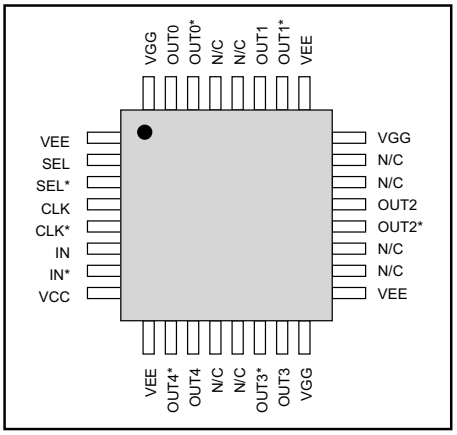
- 1:5 Clock/Data Driver
- 3 GHz Fmax
- Anything to ECL Translation



Functional Block Diagram



Pin Description



Package Information

32 pin, 5 mm x 5 mm
TQFP Package

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High Input Low	VIH VIL	VEE + 2.0 VEE		VCC VCC -.2	V V
(IN - IN*, CLK - CLK*, SEL - SEL*) Differential Input Voltage	| Input - Input* |	.2		4.3	V
Timing Inputs (CLK / CLK*) Input High Current Input Low Current	 IIH IIL	 +1 -1		 +25 +1	 µA µA
Functional Inputs (IN / IN*, SEL / SEL*) Input Current	IIH, IIL	-420		+250	µA
Outputs					
Digital Output Voltage Output Common Mode Range	| OUT - OUT* | (OUT + OUT*) / 2	600 VGG -1.5	700 VGG - 1.3	 VGG -1.1	mV V
Power Supply					
Power Supply Current Positive Supply Voltage Negative Supply Voltage	IEE ICC VCC VGG VEE VCC - VGG	 2.0 -.1 -3.6 0	95 45 3.3 0 -3.3	120 52 3.6 2.0 -3.0 3.6	mA mA V V V V

Test Conditions: Outputs terminated with 50Ω to VGG – 2V.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay CLK to OUT (SEL = 0) CLK to OUT (SEL = 1) SEL to OUT	 Tpd Tpd Tpd	 490 340 330	 590 440 430	 690 540 530	 ps ps ps
Channel to Channel Skew				<20	ps
Maximum Operating Frequency (Note 1)	Fmax	3.0			GHz
Minimum Pulse Width (Note 1)	PW min	160			ps
IN to CLK (Note 1) Set Up Time Hold Time	 Tsu Th	 100 100			 ps ps
Output Rise and Fall Times (20% / 80%)	Tr / Tf		125	150	ps
Temperature Coefficient	ΔTpd /ΔT		<1		ps / °C

Note 1: Guaranteed by characterization. Not production tested.

Description

The SK1527 is an extremely fast, stable, and accurate low skew 1:5 clock / signal distributor featuring a synchronous enable, which allows the outputs to be turned off and on without the risk of an upredictable output pulse. It is also capable of receiving inputs of any technology or voltage level. The D - flip-flop is triggered on the falling edge of the clock.

The SK1527 uses 50Ω outputs with source /sink capability, and is optimized for:

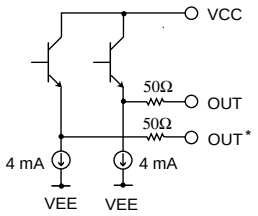
- High speed clock / data lines that require translation
- Point to point, double termination applications

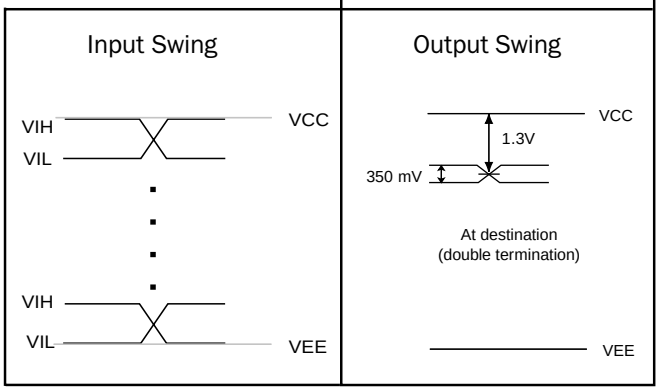
Features

- 1:5 Clock/Data Driver
- 3 GHz Fmax
- Anything to PECL Translation

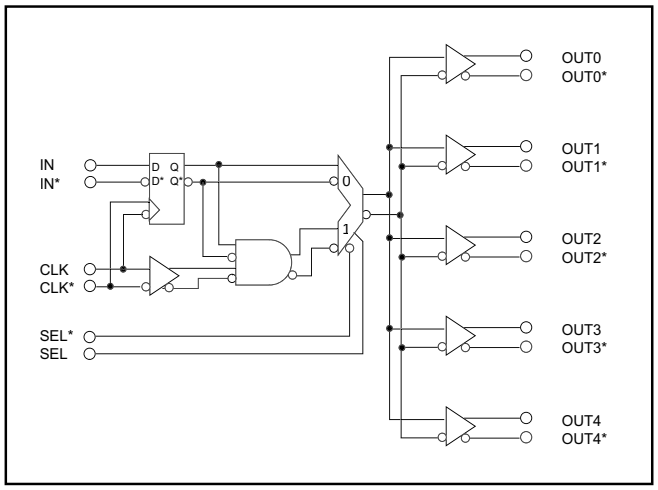
Output Options

50Ω Source / Sink

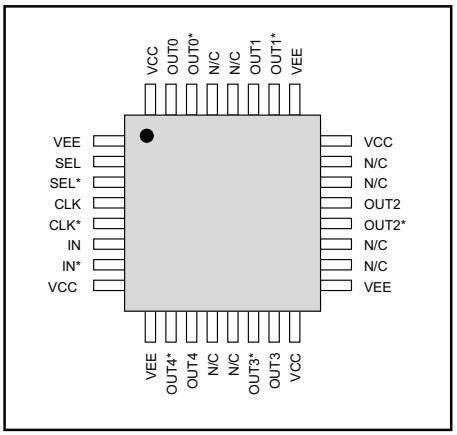




Functional Block Diagram



Pin Description



Package Information

32 pin, 5 mm x 5 mm TQFP Package

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High Input Low	VIH VIL	VEE + 2.0 VEE		VCC VCC - .2	V V
(IN - IN*, CLK - CLK*, SEL - SEL*) Differential Input Voltage	| Input - Input* |	.2		4.3	V
Timing Inputs (CLK / CLK*) Input High Current Input Low Current	IIH IIL	+1 -1		+25 +1	µA µA
Functional Inputs (IN / IN*, SEL / SEL*) Input Current	IIH, IIL	-420		+250	µA
Outputs					
Digital Output Voltage Output Common Mode Range Internal Current Source Output Impedance	| OUT - OUT* | (OUT + OUT*) / 2 ISINK ROUT	600 VCC - 1.5 4 40	700 VCC -1.3 5 45	 VCC - 1.1 6 50	mV V mA Ω
Power Supply					
Power Supply Current Positive Supply Voltage Negative Supply Voltage	IEE VCC VEE	 3.0 -3.6	135 3.3 -3.3	170 3.6 -3.0	mA V V

Test Conditions: Outputs unterminated.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay CLK to OUT (SEL = 0) CLK to OUT (SEL = 1) SEL to OUT	 Tpd Tpd Tpd	 490 340 330	 590 440 430	 690 540 530	 ps ps ps
Channel to Channel Skew				<20	ps
Maximum Operating Frequency (Note 1)	Fmax	3.0			GHz
Minimum Pulse Width (Note 1)	PW min	160			ps
IN to CLK (Note 1) Set Up Time Hold Time	 Tsu Th	 100 100			 ps ps
Output Rise and Fall Times (20% / 80%)	Tr / Tf		125	150	ps
Temperature Coefficient	ΔTpd /ΔT		<1		ps / ^{o}C

Note 1: Guaranteed by characterization. Not production tested.

Description

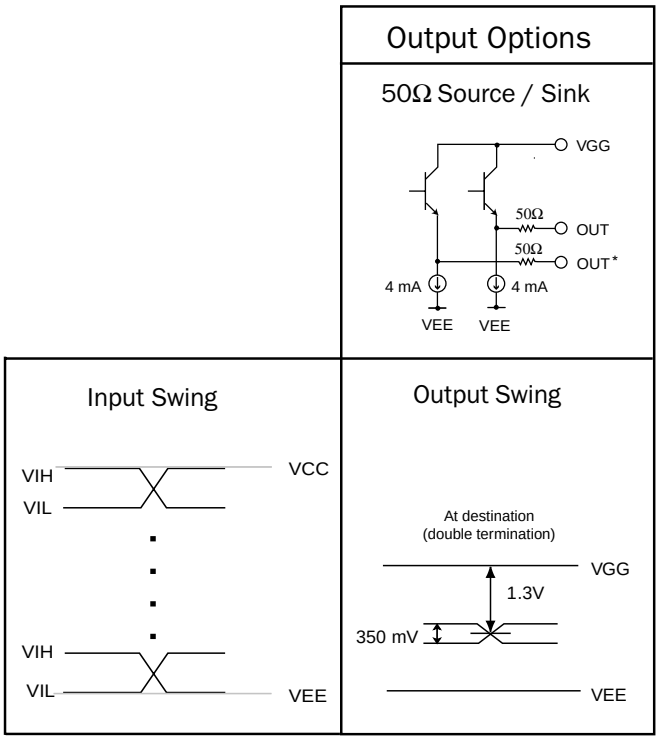
The SK1528 is an extremely fast, stable, and accurate low skew 1:5 clock / signal distributor featuring a synchronous enable, which allows the outputs to be turned off and on without the risk of an upredictable output pulse. It is also capable of receiving inputs of any technology and voltage level. The D - flip-flop is triggered on the falling edge of the clock.

The SK1528 has 50Ω outputs with source /sink capability, and is optimized for:

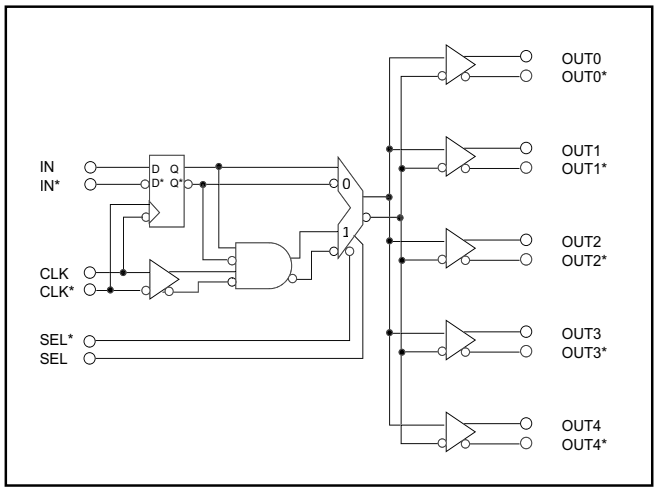
- High speed clock / data lines that require translation
- Point to point, double termination applications

Features

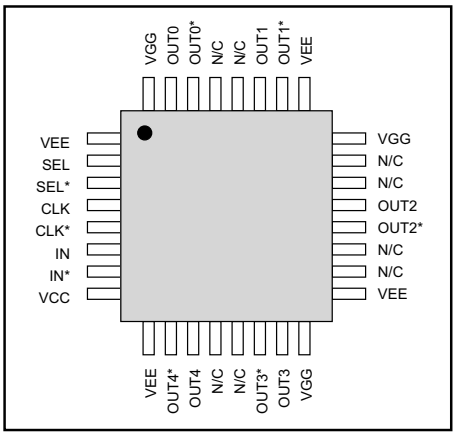
- 1:5 Clock/Data Driver
- 3 GHz Fmax
- Anything to ECL Translation



Functional Block Diagram



Pin Description



Package Information

32 pin, 5 mm x 5 mm
TQFP Package

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High Input Low	VIH VIL	VEE + 2.0 VEE		VCC VCC - .2	V V
(IN - IN*, CLK - CLK*, SEL - SEL*) Differential Input Voltage	| Input - Input* |	.2		4.3	V
Timing Inputs (CLK / CLK*) Input High Current Input Low Current	 IIH IIL	 +1 -1		 +25 +1	 µA µA
Functional Inputs (IN / IN*, SEL / SEL*) Input Current	IIH, IIL	-420		+250	µA
Outputs					
Digital Output Voltage Output Common Mode Range Internal Current Source Output Impedance	| OUT - OUT* | (OUT + OUT*) / 2 ISINK ROUT	600 VGG - 1.5 4 40	700 VGG -1.3 5 45	 VGG - 1.1 6 50	mV V mA Ω
Power Supply					
Power Supply Current Positive Supply Voltage Negative Supply Voltage	IEE ICC VCC VGG VEE VCC - VGG	 2.0 -.1 -3.6 0	135 45 3.3 0 -3.3	170 52 3.6 2.0 -3.0 3.6	mA mA V V V V

Test Conditions: Outputs unterminated.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay CLK to OUT (SEL = 0) CLK to OUT (SEL = 1) SEL to OUT	 Tpd Tpd Tpd	 490 340 330	 590 440 430	 690 540 530	 ps ps ps
Channel to Channel Skew				<20	ps
Maximum Operating Frequency (Note 1)	Fmax	3.0			GHz
Minimum Pulse Width (Note 1)	PW min	160			ps
IN to CLK (Note 1) Set Up Time Hold Time	 Tsu Th	 100 100			 ps ps
Output Rise and Fall Times (20% / 80%)	Tr / Tf		125	150	ps
Temperature Coefficient	ΔTpd /ΔT		<1		ps / ^{o}C

Note 1: Guaranteed by characterization. Not production tested.

Description

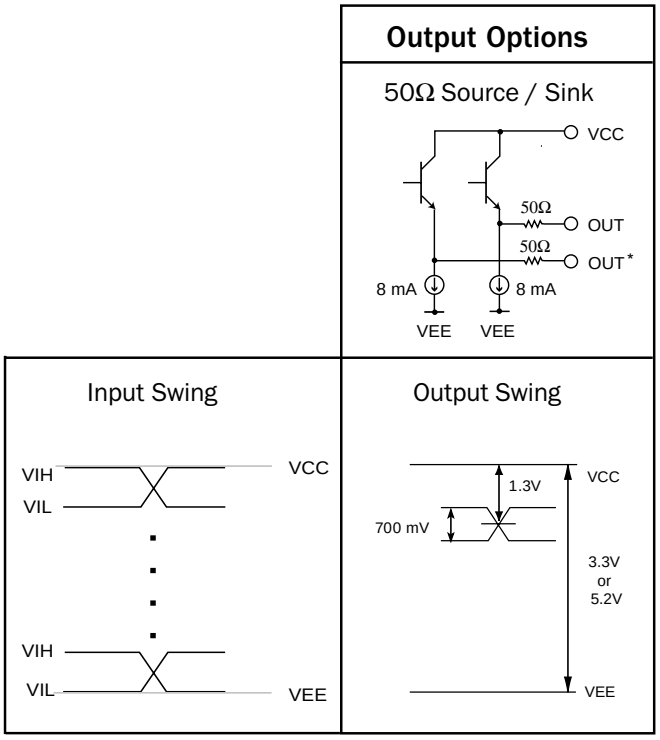
The SK1529 is an extremely fast, stable, and accurate low skew 1:5 clock / signal distributor featuring a synchronous enable, which allows the outputs to be turned off and on without the risk of an upredictable output pulse. It is also capable of receiving inputs of any technology and voltage level. The D - flip-flop is triggered on the falling edge of the clock.

The SK1529 uses 50Ω outputs with source /sink capability, and is optimized for:

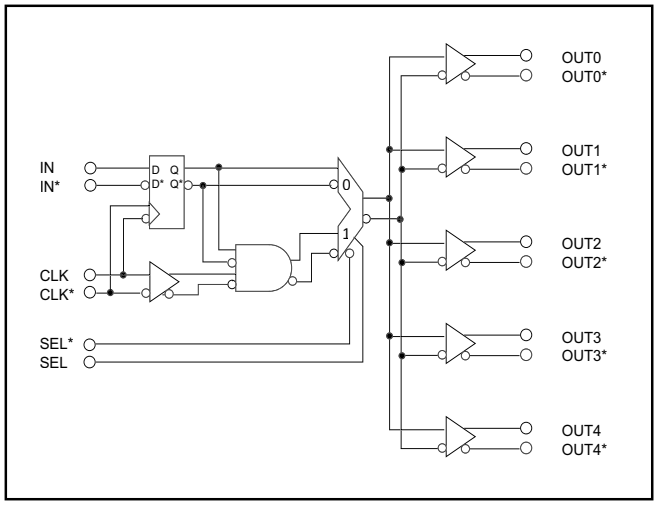
- High speed clock / data lines that require translation
- Point to point, series termination applications

Features

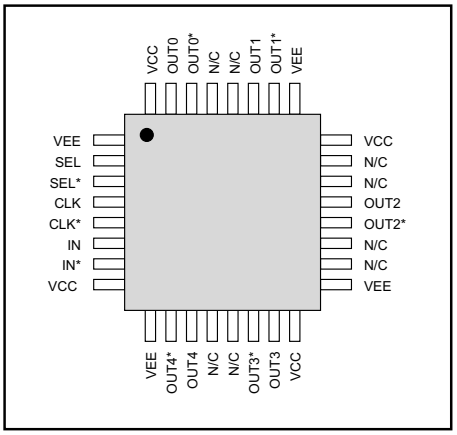
- 1:5 Clock/Data Driver
- 3 GHz Fmax
- Anything to PECL Translation



Functional Block Diagram



Pin Description



Package Information

32 pin, 5 mm x 5 mm TQFP Package

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High Input Low	VIH VIL	VEE + 2.0 VEE		VCC VCC - .2	V V
(IN - IN*, CLK - CLK*, SEL - SEL*) Differential Input Voltage	| Input - Input* |	.2		4.3	V
Timing Inputs (CLK / CLK*) Input High Current Input Low Current	 IIH IIL	 +1 -1		 +25 +1	 µA µA
Functional Inputs (IN / IN*, SEL / SEL*) Input Current	IIH, IIL	-420		+250	µA
Outputs					
Digital Output Voltage Output Common Mode Range Internal Current Source Output Impedance	| OUT - OUT* | (OUT + OUT*) / 2 ISINK ROUT	600 VCC - 1.5 6.5 40	700 VCC -1.3 8 45	 VCC - 1.1 10 50	mV V mA Ω
Power Supply					
Power Supply Current Positive Supply Voltage Negative Supply Voltage	IEE VCC VEE	 3.0 -3.6	175 3.3 -3.3	221 3.6 -3.0	mA V V

Test Conditions: Outputs unterminated.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay CLK to OUT (SEL = 0) CLK to OUT (SEL = 1) SEL to OUT	 Tpd Tpd Tpd	 490 340 330	 590 440 430	 690 540 530	 ps ps ps
Channel to Channel Skew				<20	ps
Maximum Operating Frequency (Note 1)	Fmax	3.0			GHz
Minimum Pulse Width (Note 1)	PW min	160			ps
IN to CLK (Note 1) Set Up Time Hold Time	 Tsu Th	 100 100			 ps ps
Output Rise and Fall Times (20% / 80%)	Tr / Tf		125	150	ps
Temperature Coefficient	ΔTpd /ΔT		<1		ps / ^{o}C

Note 1: Guaranteed by characterization. Not production tested.

Description

The SK1530 is an extremely fast, stable and accurate low skew 1:5 clock / signal distributor featuring a synchronous enable, which allows the outputs to be turned off and on without the risk of an upredictable output pulse. It is also capable of receiving inputs of any technology or voltage level. The D - flip-flop is triggered on the falling edge of the clock.

The SK1530 uses 50Ω outputs with source /sink capability, and is optimized for:

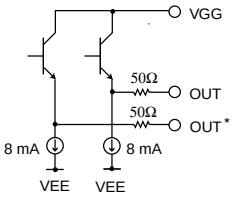
- High speed clock / data lines that require translation
- Point to point, series termination applications

Features

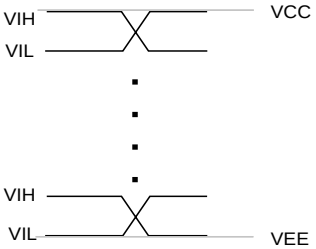
- 1:5 Clock/Data Driver
- 3 GHz Fmax
- Anything to ECL Translation

Output Options

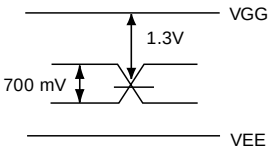
50Ω Source / Sink



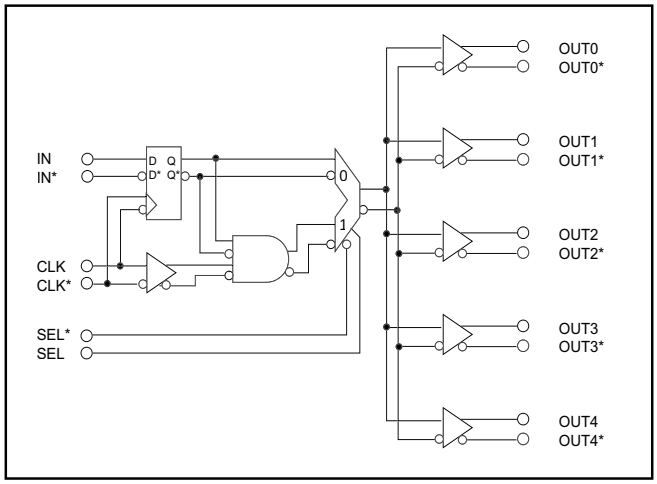
Input Swing



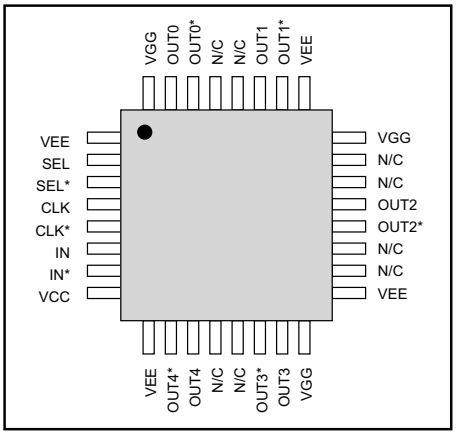
Output Swing



Functional Block Diagram



Pin Description



Package Information

32 pin, 5 mm x 5 mm
TQFP Package

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High Input Low	VIH VIL	VEE + 2.0 VEE		VCC VCC - .2	V V
(IN - IN*, CLK - CLK*, SEL - SEL*) Differential Input Voltage	| Input - Input* |	.2		4.3	V
Timing Inputs (CLK / CLK*) Input High Current Input Low Current	 IIH IIL	 +1 -1		 +25 +1	 µA µA
Functional Inputs (IN / IN*, SEL / SEL*) Input Current	IIH, IIL	-420		+250	µA
Outputs					
Digital Output Voltage Output Common Mode Range Internal Current Source Output Impedance	| OUT - OUT* | (OUT + OUT*) / 2 ISINK ROUT	600 VGG - 1.5 6.5 40	700 VGG -1.3 8 45	 VGG - 1.1 10 50	mV V mA Ω
Power Supply					
Power Supply Current Positive Supply Voltage Negative Supply Voltage	IEE ICC VCC VGG VEE VCC - VGG	 2.0 -.1 -3.6 0	175 45 3.3 0 -3.3	221 52 3.6 2.0 -3.0 3.6	mA mA V V V V

Test Conditions: Outputs unterminated.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay CLK to OUT (SEL = 0) CLK to OUT (SEL = 1) SEL to OUT	 Tpd Tpd Tpd	 490 340 330	 590 440 430	 690 540 530	 ps ps ps
Channel to Channel Skew				<20	ps
Maximum Operating Frequency (Note 1)	Fmax	3.0			GHz
Minimum Pulse Width (Note 1)	PW min	160			ps
IN to CLK (Note 1) Set Up Time Hold Time	 Tsu Th	 100 100			 ps ps
Output Rise and Fall Times (20% / 80%)	Tr / Tf		125	150	ps
Temperature Coefficient	ΔTpd /ΔT		<1		ps / ^{o}C

Note 1: Guaranteed by characterization. Not production tested.

Description

The SK1599 is an extremely fast, stable, and accurate low skew 1:5 clock / signal distributor featuring a synchronous enable, which allows the outputs to be turned off and on without the risk of an unpredictable output pulse. The D - flip-flop is triggered on the falling edge of the clock.

The SK1599 has open collector (CML) outputs, targeted for:

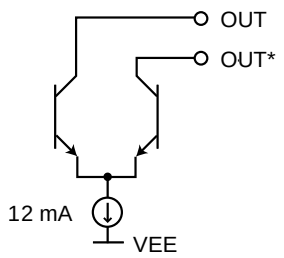
- Ultra high speed applications
- Adjustable common mode levels at the destination.

Features

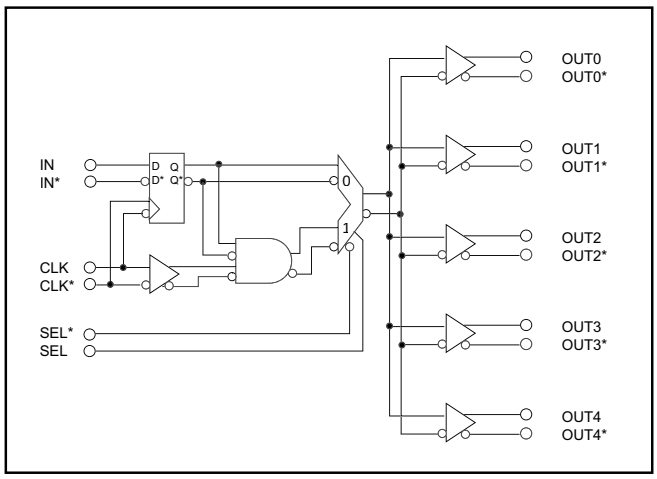
- 1:5 Clock/Data Driver
- 3 GHz Fmax
- 3.3V / 5.2V Compatible

Output Options

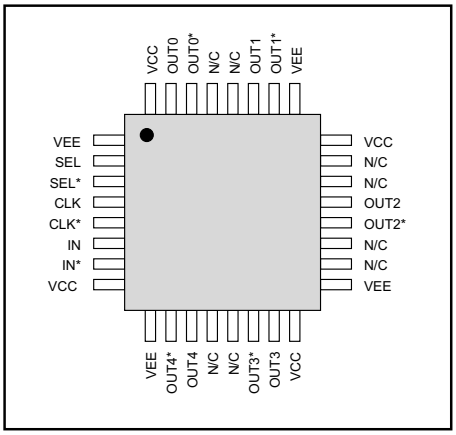
Open Collector



Functional Block Diagram



Pin Description



Package Information

32 pin, 5 mm x 5 mm
TQFP Package

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High Input Low	VIH VIL	VEE + 2.0 VEE		VCC VCC -.2	V V
(IN - IN*, CLK - CLK*, SEL - SEL*) Differential Input Voltage	| Input - Input* |	.2		4.3	V
Timing Inputs (CLK / CLK*) Input High Current Input Low Current	 IIH IIL	 +1 -1		 +25 +1	 µA µA
Functional Inputs (IN / IN*, SEL / SEL*) Input Current	IIH, IIL	-420		+250	µA
Outputs					
Output Current High Output Current Low	IOH IOL		0 12		mA mA
Power Supply					
Power Supply Current Power Supply Voltage	IEE VCC - VEE	 3.0	145	183 5.5	mA V

Test Conditions: Outputs terminated with 50Ω to VCC.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay CLK to OUT (SEL = 0) CLK to OUT (SEL = 1) SEL to OUT	 Tpd Tpd Tpd	 490 340 330	 590 440 430	 690 540 530	 ps ps ps
Channel to Channel Skew				<20	ps
Maximum Operating Frequency (Note 1)	Fmax	3.0			GHz
Minimum Pulse Width (Note 1)	PW min	160			ps
IN to CLK (Note 1) Set Up Time Hold Time	 Tsu Th	 100 100			 ps ps
Output Rise and Fall Times (20% / 80%)	Tr / Tf		125	150	ps
Temperature Coefficient	ΔTpd /ΔT		<1		ps / ^{o}C

Note 1: Guaranteed by characterization. Not production tested.

Ordering Information

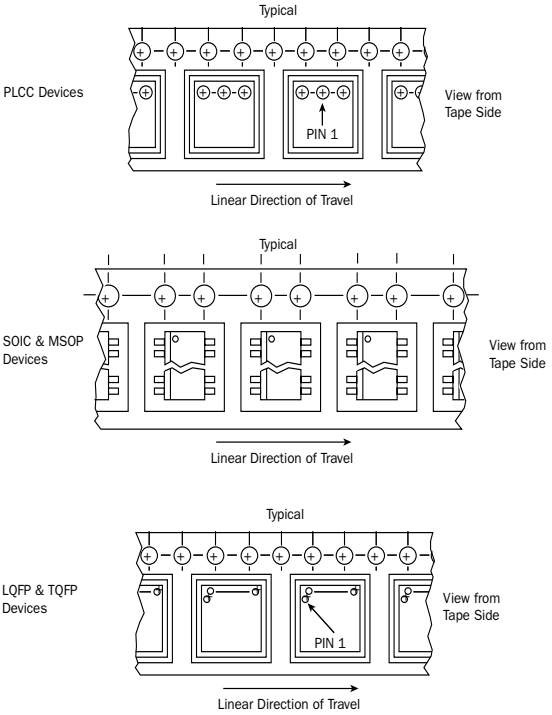
Ordering Code	Package ID	Temperature Range
SK1500	32 - TQFP 5 X 5 mm	Commercial
SK1501	32 - TQFP 5 X 5 mm	Commercial
SK1502	32 - TQFP 5 X 5 mm	Commercial
SK1503	32 - TQFP 5 X 5 mm	Commercial
SK1504	32 - TQFP 5 X 5 mm	Commercial
SK1525	32 - TQFP 5 X 5 mm	Commercial
SK1526	32 - TQFP 5 X 5 mm	Commercial
SK1527	32 - TQFP 5 X 5 mm	Commercial
SK1528	32 - TQFP 5 X 5 mm	Commercial
SK1529	32 - TQFP 5 X 5 mm	Commercial
SK1530	32 - TQFP 5 X 5 mm	Commercial
SK1599	32 - TQFP 5 X 5 mm	Commercial

Note: For tape and reel, add the letter “T” at the end of Ordering Code.

Device Type	Tape Width (mm)	Max Device/Reel	Reel Size (inch)	Max Device/Tube
PLCC-28	24	750	13	37
SOIC-8	12	2,500	13	98
SOIC-16	16	2,500	13	49
SOIC-20	24	1,000	13	38
MSOP-8	12	2,500	13	50
MSOP-10	12	2,500	13	50
LQFP-32 (7 x 7 mm)	16	1,000	13	250 (tray)
TQFP-32 (7 x 7 mm)	16	1,000	13	250 (tray)
TQFP-32 (5 x 5 mm)	16	1,000	13	360 (tray)

Tape and Reel

Semtech's tape and reel packaging fully conforms to the latest EIA-481-1A and EIA-481-2A specifications. The antistatic embossed tape provides a secure cavity sealed with a peel-back cover tape.



Ordering Information

To order devices which are to be delivered in Tape and Reel, add the suffix T to the device number being ordered.

Contact Information

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