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TEL:805-498-2111 FAX:805-498-3804 WEB:http://www.semtech.com

DESCRIPTION

The SC1102 is a low-cost, full featured, synchronous voltage-mode controller designed for use in single ended power supply applications where efficiency is of primary concern. Synchronous operation allows for the elimination of heat sinks in many applications. The SC1102 is ideal for implementing DC/DC converters needed to power advanced microprocessors in low cost systems, or in distributed power applications where efficiency is important. Internal level-shift, high-side drive circuitry, and preset shoot-thru control, allows the use of inexpensive N-channel power switches.

SC1102 features include temperature compensated voltage reference, triangle wave oscillator and current sense comparator circuitry. Power good signaling, shutdown, and over voltage protection are also provided.

The SC1102 operates at a fixed 200kHz, providing an optimum compromise between efficiency, external component size, and cost.

FEATURES

- 1.265V Reference available
- Synchronous operation
- Over current fault monitor
- On-chip power good and OVP functions
- Small size with minimum external components
- Soft Start
- $R_{DS(ON)}$ Current sensing

APPLICATIONS

- Microprocessor core supply
- Low cost synchronous applications
- Voltage Regulator Modules (VRM)

ORDERING INFORMATION

DEVICE(1)	PACKAGE	TEMP. RANGE (T_J)
SC1102CSTR	SO-14	0 - 125°C
SC1102EVB	Evaluation Board	

Note:
(1) Only available in tape and reel packaging. A reel contains 2500 devices.

APPLICATION CIRCUIT

Typical Distributed Power Supply

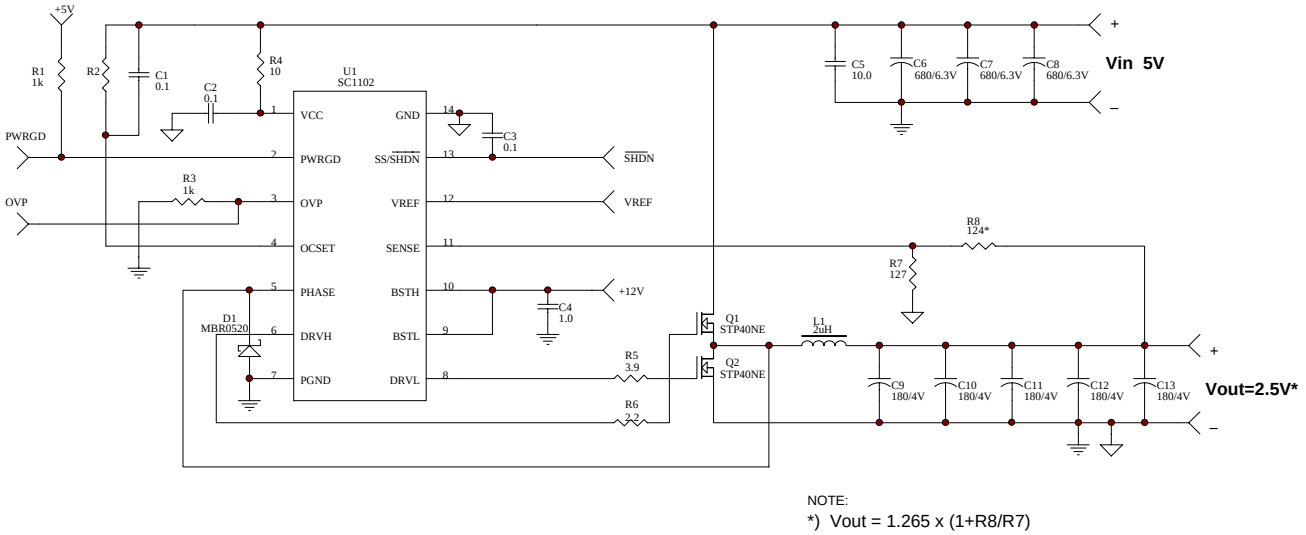

Figure 1.

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Maximum	Units
V_{CC}, BSTL to GND	V_{IN}	-0.3 to 14	V
PGND to GND		± 0.5	V
PHASE to GND		-0.3 to 18	V
BSTH to PHASE		14	V
Thermal Resistance Junction to Case	θ_{JC}	45	°C/W
Thermal Resistance Junction to Ambient	θ_{JA}	115	°C/W
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature (Soldering) 10 sec	T_{LEAD}	300	°C
ESD Rating (Human Body Model)	ESD	2	kV

ELECTRICAL CHARACTERISTICS

Unless specified: V_{CC} = 4.75V to 12.6V; GND = PGND = 0V; FB = V_O; V_{BSTL} = 12V; $V_{BSTH-PHASE}$ = 12V; T_J = 25°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY					
Supply Voltage	V_{CC}	4.2		12.6	V
Supply Current	EN = V_{CC}		6	10	mA
Line Regulation	V_O = 2.5V		0.5		%
ERROR AMPLIFIER					
Gain (AOL)			35		dB
Input Bias			5	8	µA
OSCILLATOR					
Oscillator Frequency		180	200	220	kHz
Oscillator Max Duty Cycle		90	95		%
MOSFET DRIVERS					
DH Source/Sink Current	BST_H - DH = 4.5V / DH - PHASE = 2V	1			A
DL Source/Sink Current	BST_L - DL = 4.5V / DL - $PGND_L$ = 2V	1			A
PROTECTION					
OVP Threshold Voltage			20		%
OVP Source Current	V_{OVP} = 3V	10			mA
Power Good Threshold		88		112	%
Dead Time		45		100	ns
Over Current Set Isource	2.0V ≤ V_{OCSET} ≤ 12V	180	200	220	µA

NOTE:

(1) Specification refers to application circuit (Figure 1).

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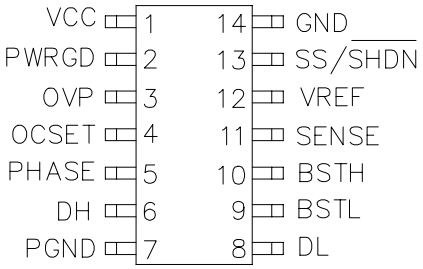
ELECTRICAL CHARACTERISTICS (CONT)

Unless specified: V_{CC} = 4.75V to 12.6V; GND = PGND = 0V; FB = V_O; V_{BSTL} = 12V; $V_{BSTH-PHASE}$ = 12V; T_J = 25°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE					
Reference Voltage		1.252	1.265	1.278	V
Accuracy		-1		+1	%
SOFT START					
Charge Current	V_{SS} = 1.5V	8.0	10	12	µA
Discharge Current	V_{SS} = 1.5V	1.3	2	2.4	µA

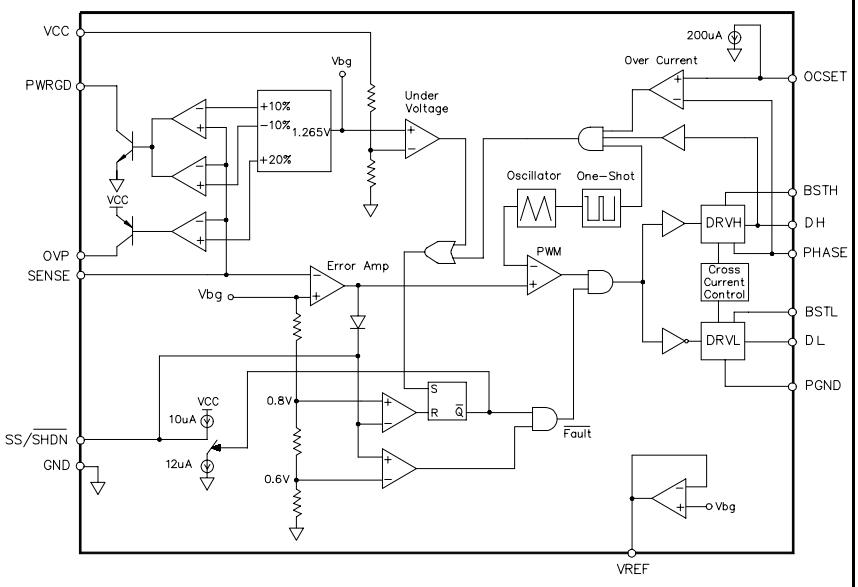
PIN CONFIGURATION

Top View



(14-Pin SOIC)

BLOCK DIAGRAM



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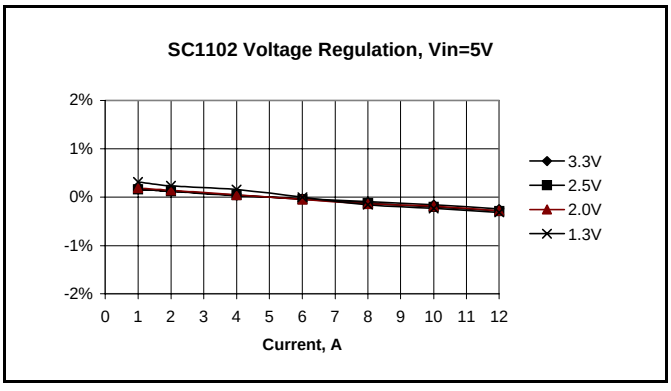
PIN DESCRIPTION

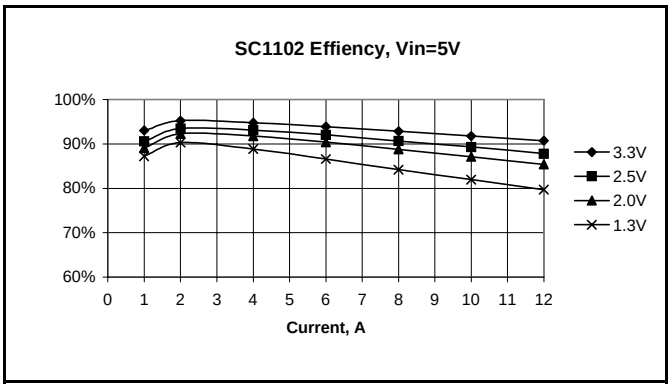
Pin #	Pin Name	Pin Function
1	VCC	Chip supply voltage
2	PWRGD	Logic high indicates correct output voltage
3	OVP	Over voltage protection.
4	OCSET	Sets the converter overcurrent trip point
5	PHASE	Input from the phase node between the MOSFET'S
6	DH	High side driver output
7	PGND	Power ground
8	DL	Low side driver output
9	BSTL	Bootstrap, low side driver.
10	BSTH	Bootstrap, high side driver.
11	SENSE	Voltage sense input
12	VREF	Buffered band gap voltage reference.
13	SS/$\overline{\text{SHDN}}$	Soft start. A capacitor to ground sets the slow start time.
14	GND	Signal ground

NOTE:

(1) All logic level inputs and outputs are open collector TTL compatible.

CHARACTERISTIC CURVES





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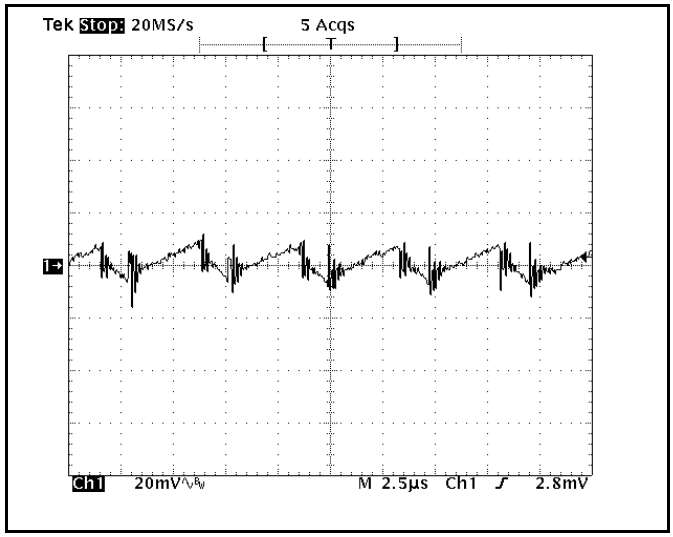
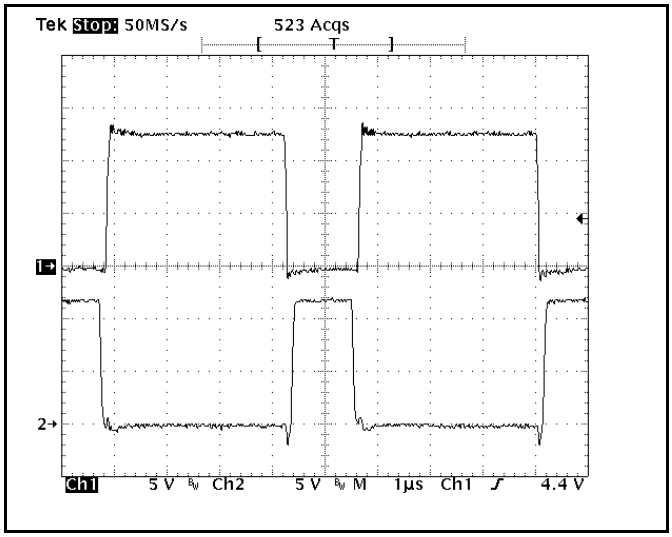
Output Ripple Voltage

1. V_{IN} = 5V; V_O = 3.3V; I_{OUT} = 12A



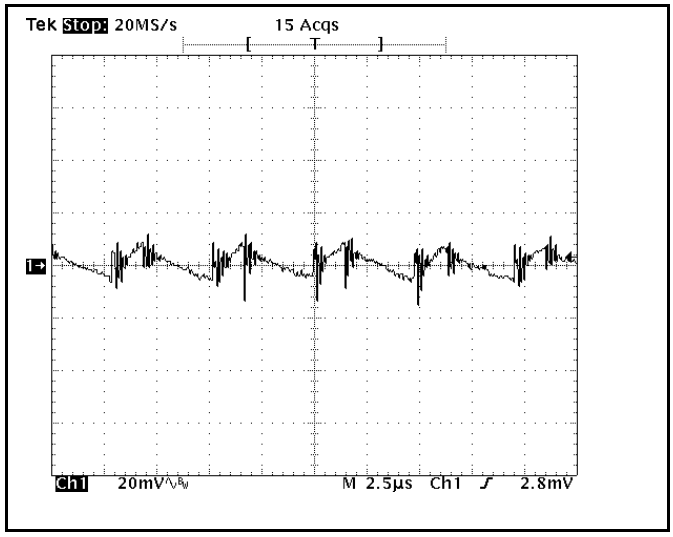
Ch1: Vo_rpl

Gate Drive Waveforms

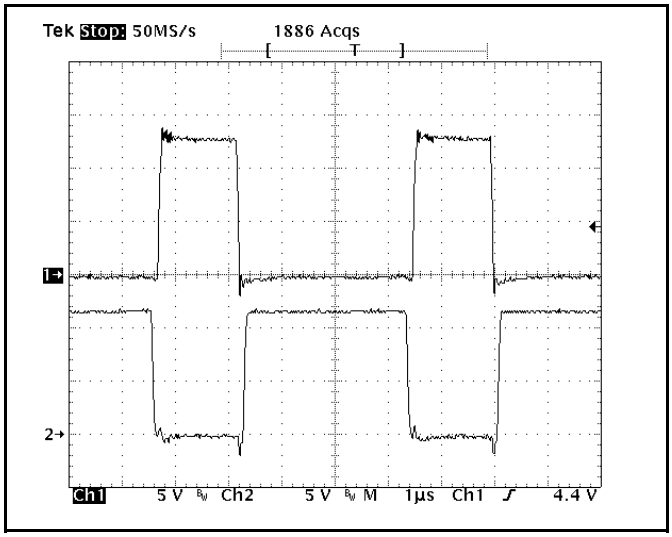


Ch1: Top FET
Ch2: Bottom FET

2. V_{IN} = 5V; V_{OUT} = 1.3V; I_{OUT} = 12A



Ch1: Vo_rpl



Ch1: Top FET
Ch2: Bottom FET

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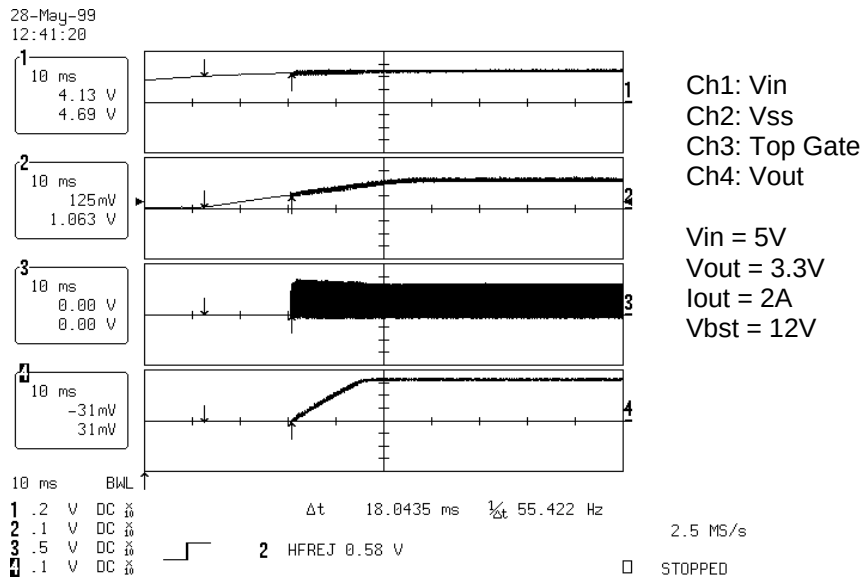
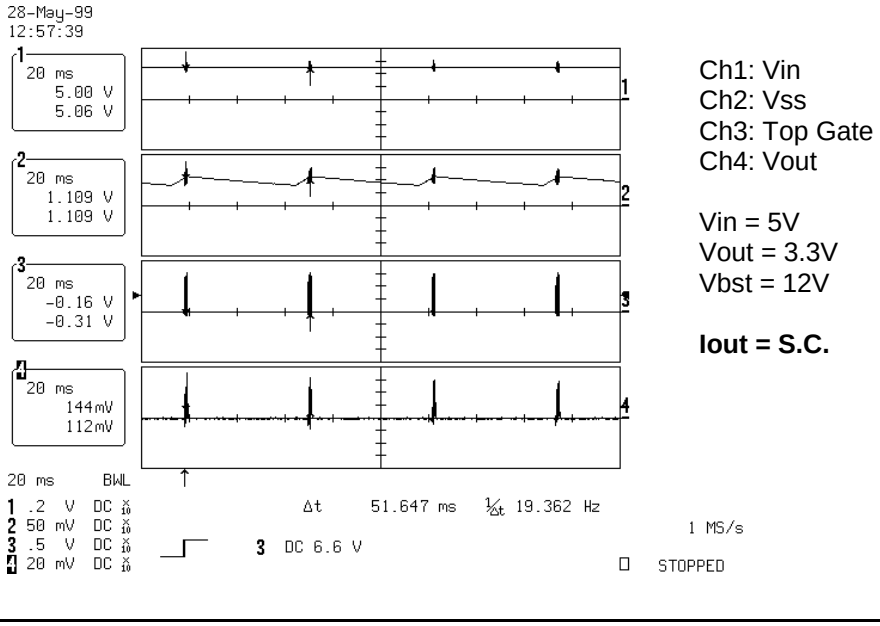
Start Up



Ch1: Vin
Ch2: Vss
Ch3: Top Gate
Ch4: Vout

Vin = 5V
Vout = 3.3V
Iout = 2A
Vbst = 12V

Hiccup Mode



Ch1: Vin
Ch2: Vss
Ch3: Top Gate
Ch4: Vout

Vin = 5V
Vout = 3.3V
Vbst = 12V

Iout = S.C.

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THEORY OF OPERATION

Synchronous Buck Converter

Primary V_{CORE} power is provided by a synchronous, voltage-mode pulse width modulated (PWM) controller. This section has all the features required to build a high efficiency synchronous buck converter, including "Power Good" flag, shut-down, and cycle-by-cycle current limit.

The output voltage of the synchronous converter is set and controlled by the output of the error amplifier. The external resistive divider reference voltage is derived from an internal trimmed-bandgap voltage reference (See Fig. 1). The inverting input of the error amplifier receives its voltage from the SENSE pin.

The internal oscillator uses an on-chip capacitor and trimmed precision current sources to set the oscillation frequency to 200kHz. The triangular output of the oscillator sets the reference voltage at the inverting input of the comparator. The non-inverting input of the comparator receives it's input voltage from the error amplifier. When the oscillator output voltage drops below the error amplifier output voltage, the comparator output goes high. This pulls DL low, turning off the low-side FET, and DH is pulled high, turning on the high-side FET (once the cross-current control allows it). When the oscillator voltage rises back above the error amplifier output voltage, the comparator output goes low. This pulls DH low, turning off the high-side FET, and DL is pulled high, turning on the low-side FET (once the cross-current control allows it).

As SENSE increases, the output voltage of the error amplifier decreases. This causes a reduction in the on-time of the high-side MOSFET connected to DH, hence lowering the output voltage.

Under Voltage Lockout

The under voltage lockout circuit of the SC1102 assures that the high-side MOSFET driver outputs remain in the off state whenever the supply voltage drops below set parameters. Lockout occurs if V_{CC} falls below 4.1V. Normal operation resumes once V_{CC} rises above 4.2V.

Over-Voltage Protection

The over-voltage protection pin (OVP) is high only when the voltage at SENSE is 20% higher than the target value programmed by the external resistor divider. The OVP pin is internally connected to a PNP's collector.

Power Good

The power good function is to confirm that the regulator outputs are within +/-10% of the programmed level. PWRGD remains high as long as this condition is met. PWRGD is connected to an internal open collector NPN transistor.

Soft Start

Initially, SS/$\overline{SHDN}$ sources 10µA of current to charge an external capacitor. The outputs of the error amplifiers are clamped to a voltage proportional to the voltage on SS/$\overline{SHDN}$. This limits the on-time of the high-side MOSFETs, thus leading to a controlled ramp-up of the output voltages.

$R_{DS(ON)}$ Current Limiting

The current limit threshold is set by connecting an external resistor from the V_{CC} supply to OCSET. The voltage drop across this resistor is due to the 200µA internal sink sets the voltage at the pin. This voltage is compared to the voltage at the PHASE node. This comparison is made only when the high-side drive is high to avoid false current limit triggering due to uncontributing measurements from the MOSFET's off-voltage. When the voltage at PHASE is less than the voltage at OCSET, an overcurrent condition occurs and the soft start cycle is initiated. The synchronous switcher turns off and SS/$\overline{SHDN}$ starts to sink 2µA. When SS/$\overline{SHDN}$ reaches 0.8V, it then starts to source 10µA and a new cycle begins.

Hiccup Mode

During power up, the SS/$\overline{SHDN}$ pin is internally pulled low until VCC reaches the undervoltage lockout level of 4.2V. Once V_{CC} has reached 4.2V, the SS/$\overline{SHDN}$ pin is released and begins to source 10µA of current to the external soft-start capacitor. As the soft-start voltage rises, the output of the internal error amplifier is clamped to this voltage. When the error signal reaches the level of the internal triangular oscillator, which swings from 1V to 2V at a fixed frequency of 200 kHz, switching occurs. As the error signal crosses over the oscillator signal, the duty cycle of the PWM signal continues to increase until the output comes into regulation. If an over-current condition has not occurred the soft-start voltage will continue to rise and level off at about 2.2V.

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THEORY OF OPERATION (CON'T)

An over-current condition occurs when the high-side drive is turned on, but the PHASE node does not reach the voltage level set at the OCSET pin. The PHASE node is sampled only once per cycle during the valley of the triangular oscillator. Once an over-current occurs, the high-side drive is turned off and the low-side drive turns on and the SS/$\overline{\text{SHDN}}$ pin begins to sink 2uA. The soft-start voltage will begin to decrease as the 2uA of current discharges the external capacitor. When the soft-start voltage reaches 0.8V, the SS/$\overline{\text{SHDN}}$ pin will begin to source 10uA and begin to charge the external capacitor causing the soft-start voltage to rise again. Again, when the soft-start voltage reaches the level of the internal oscillator, switching will occur.

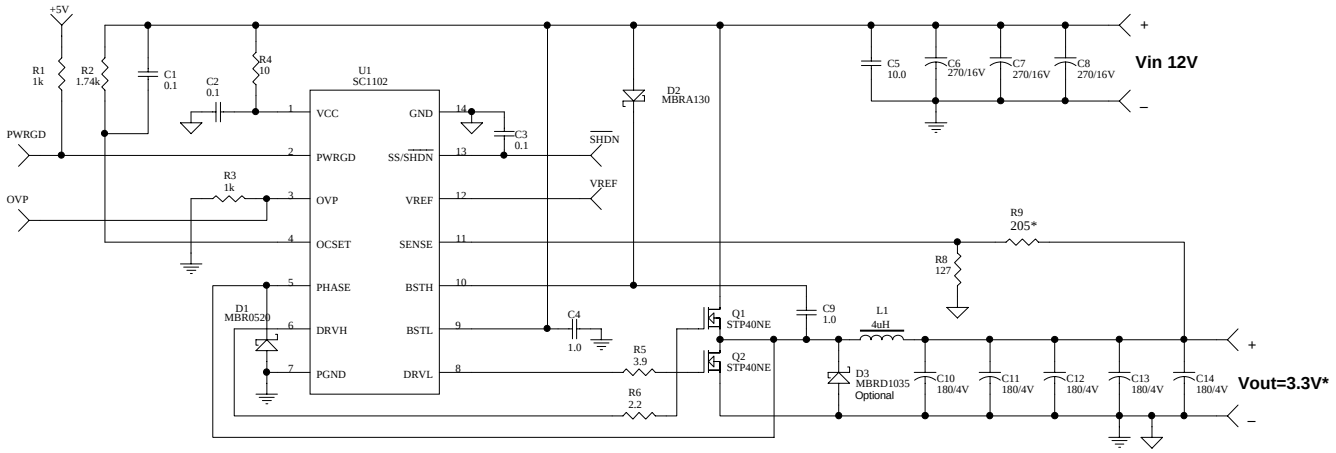
If the over-current condition is no longer present, normal operation will continue. If the over-current condition is still present, the SS/$\overline{\text{SHDN}}$ pin will again begin to sink 2uA. This cycle will continue indefinitely until the over-current condition is removed.

In conclusion, below is shown a typical "12V Application Circuit" which has a BSTH voltage derived by bootstrapping input voltage to the PHASE node through diode D1. This circuit is very useful in cases where only input power of 12V is available.

In order to prevent substrate glitching, a small-signal diode should be placed in close proximity to the chip with cathode connected to PHASE and anode connected to PGND.

APPLICATION CIRCUIT

Typical 12V Application Circuit with Bootstrapped BSTH



NOTE:
*) Vout = 1.265 x (1+R9/R8)

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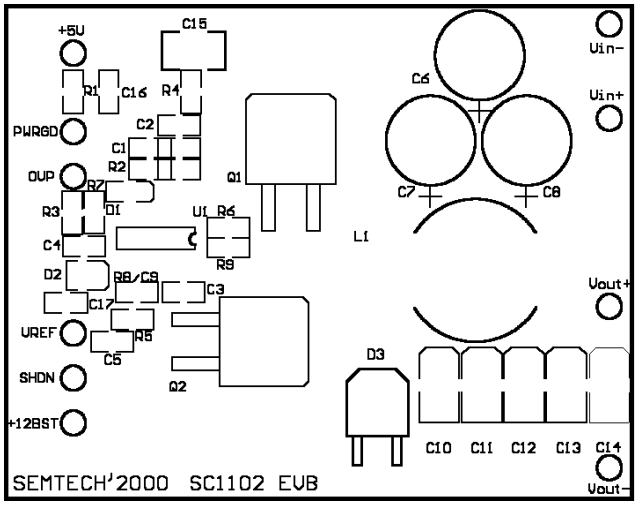
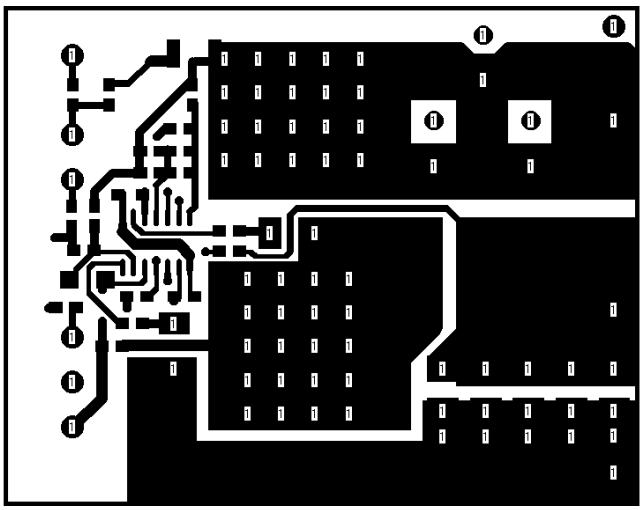
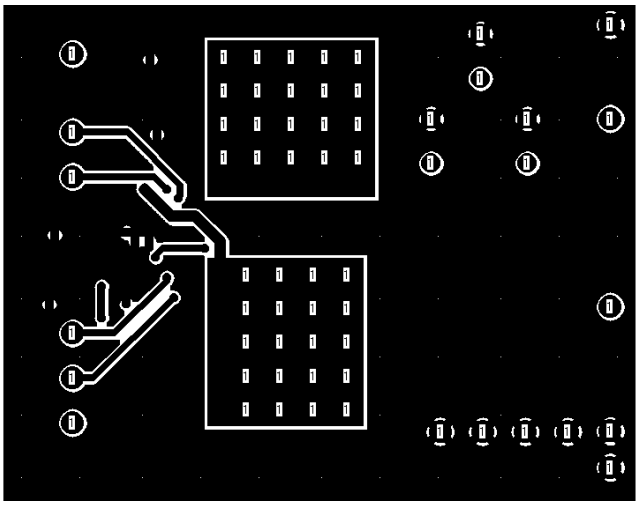
Top component side view



Top copper view



Bottom copper view



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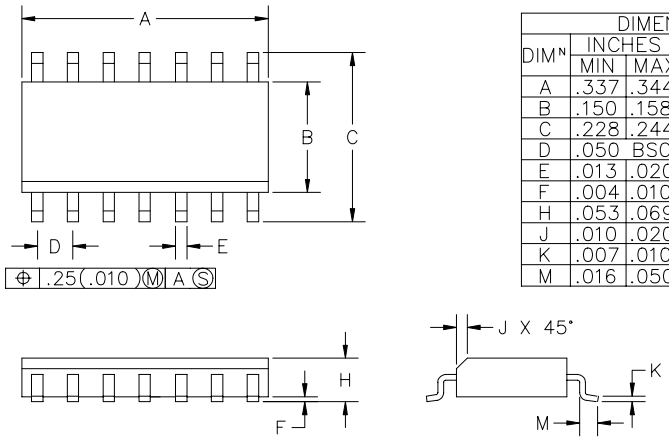
OUTLINE DRAWING SO-14



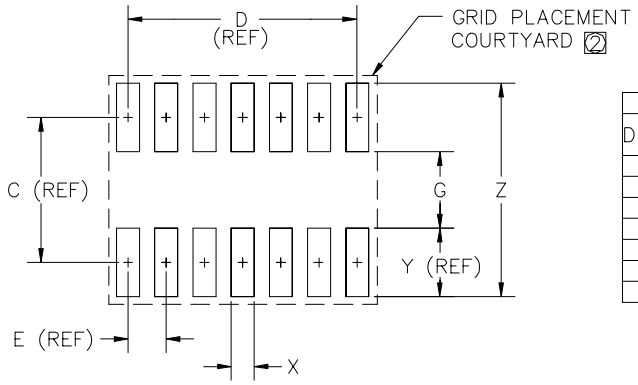
DIMENSIONS					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.337	.344	8.55	8.75	2
B	.150	.158	3.80	4.00	3
C	.228	.244	5.80	6.20	
D	.050 BSC		1.27 BSC		
E	.013	.020	0.33	0.51	
F	.004	.010	0.10	0.25	
H	.053	.069	1.35	1.75	
J	.010	.020	0.25	0.50	
K	.007	.010	.19	.25	
M	.016	.050	0.40	1.27	

[3] DIMENSION "B" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25 mm (.010") PER SIDE.

[2] DIMENSION "A" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15 mm (.010") PER SIDE.

[1] CONTROLLING DIMENSION : MILLIMETER

LAND PATTERN SO-14



DIMENSIONS 1					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
C	–	.19	–	5.00	–
D	–	.30	–	7.62	–
E	–	.05	–	1.27	–
G	.10	.11	2.60	2.80	–
X	.02	.03	.60	.80	–
Y	–	.09	–	2.40	–
Z	–	.29	7.20	7.40	–

2 GRID PLACEMENT COURTYARD IS 20x16 ELEMENTS (10mm X 8mm) IN ACCORDANCE WITH THE INTERNATIONAL GRID DETAILED IN IEC PUBLICATION 97.

1 CONTROLLING DIMENSION: MILLIMETERS

ECN00-1311