PRELIMINARY - February 29, 2000

TEL:805-498-2111 FAX:805-498-3804 WEB:http://www.semtech.com

DESCRIPTION

The SC1103 is a versatile, low-cost, voltage-mode PWM controller designed for use in single ended DC/DC power supply applications. A simple, fixed-voltage buck regulator can be implemented using the SC1103 with a minimum of external components. Internal level shift and drive circuitry eliminates the need for an expensive p-channel, high-side switch. The small device footprint allows for compact circuit design.

SC1103 features include a temperature compensated voltage reference, triangle wave oscillator, current limit comparator, frequency shift overcurrent protection, and an internally compensated error amplifier. Pulse by pulse current limiting is implemented by sensing the differential voltage across an external resistor, or an appropriately sized PC board trace.

The SC1103 operates at a fixed frequency of 200kHz, providing an optimum compromise between efficiency, external component size, and cost.

FEATURES

- Low cost / small size
- Switch mode efficiency (90%)
- 1% reference voltage accuracy
- Over current protection
- 500mA output drive
- 5V to 12V Input power source

APPLICATIONS

- Pentium® P55 Core Supply
- Low Cost Microprocessor Supplies
- Peripheral Card Supplies
- Industrial Power Supplies
- High Density DC/DC Conversion

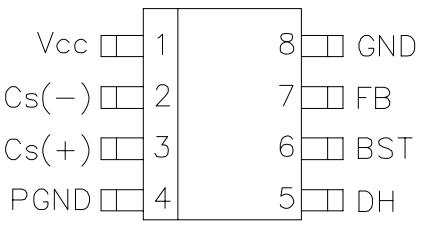
ORDERING INFORMATION

DEVICE(1)	PACKAGE	TEMP RANGE (T_J)
SC1103CS	SO-8	0° to 125°C

Note:
(1) Add suffix 'TR' for tape and reel.

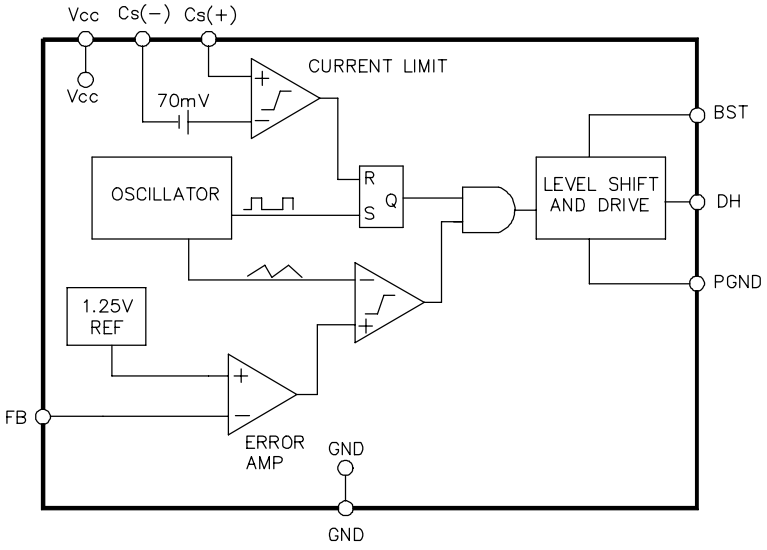
PIN CONFIGURATION

Top View



(SO-8)

BLOCK DIAGRAM



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PIN DESCRIPTION

Pin #	Pin Name	Pin Function
1	V_{CC}	Device Input Voltage
2	$C_{s(-)}$	Current Sense Input (Negative)
3	$C_{s(+)}$	Current Sense Input (Positive)
4	P_{GND}	Device Power Ground
5	DH	High Side Driver Output
6	BST	High Side Driver V_{BST} (Boost)
7	FB	Error Amplifier Input (-)
8	GND	Small Signal Ground

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Maximum	Units
Input Voltage	V_{CC} to GND	-0.3 to 14	V
Ground Differential	P_{GND} to GND	± 1	V
Boost Input Voltage	BST to GND	-0.3 to +26	V
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_S	-45 to +125	°C
Lead Temperature (Soldering) 10 seconds	T_L	300	°C
Thermal Resistance, Junction to Ambient	θ_{JA}	165	°C/W
Thermal Resistance, Junction to Case	θ_{JC}	40	°C/W

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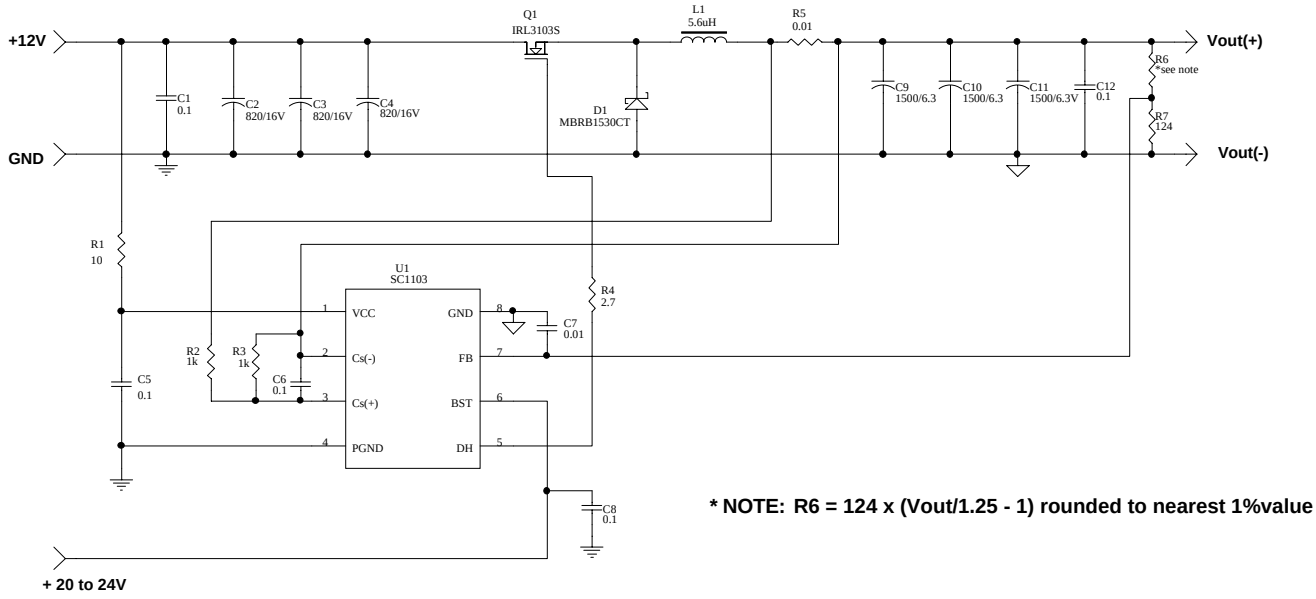
ELECTRICAL CHARACTERISTICS

V_{CC} = 11.50V to 12.50V; GND = P_{GND} = 0V; V_O = 3.3V; T_A = 25°C; BST = 24±1V; Output current = 2A.
Per test circuit, unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Reference	V_{REF}		1.238	1.250	1.263	V
		Over Temp	1.225	1.250	1.275	V
Feedback Bias Current	I_{FB}			2.0	8.0	uA
Quiescent Current	I_Q	Current into V_{CC} pin		5.0	8.0	mA
Regulation Load	REG_{LOAD}	I_O = 1A to 10A		0.5	1.0	%
Regulation Line	REG_{LINE}	I_O = 10A			0.5	%
Current Limit Threshold	CLT	CS(+) to CS(-)	60	70	80	mV
Oscillator Frequency	OSC		180	200	220	kHz
Oscillator Frequency Shift	OFS	$V_{FB} < V_{REF}/2$		50		kHz
Max Duty Cycle	d.c.		90	95		%
DH Sink/Source Current	I_O	$V_{BST} - V_{DH}$ = 4.5V ($V_{DH} - V_{PGND}$ = 2V)	500			mA
UVLO Threshold	V_{UVLO}			3.8		V

TEST CIRCUIT



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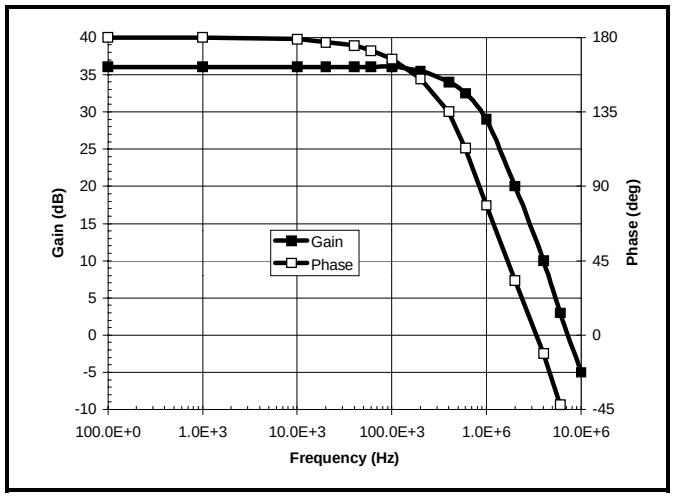

Fig.1: Error Amplifier, Gain and Phase

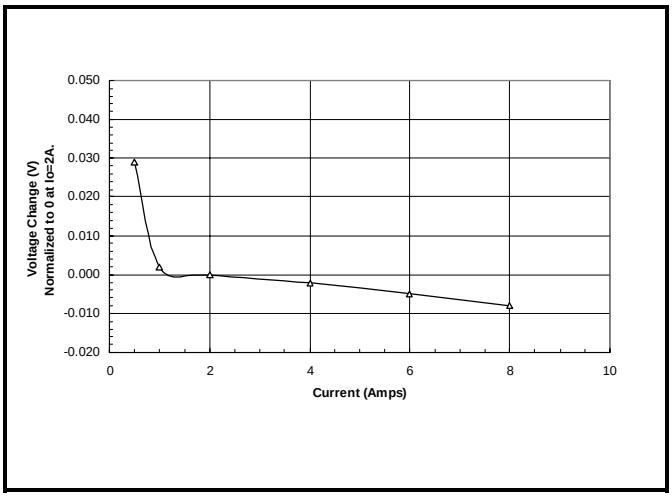

Fig. 2: Load Regulation @ V_O = 3.3V, V_{IN} = 12V

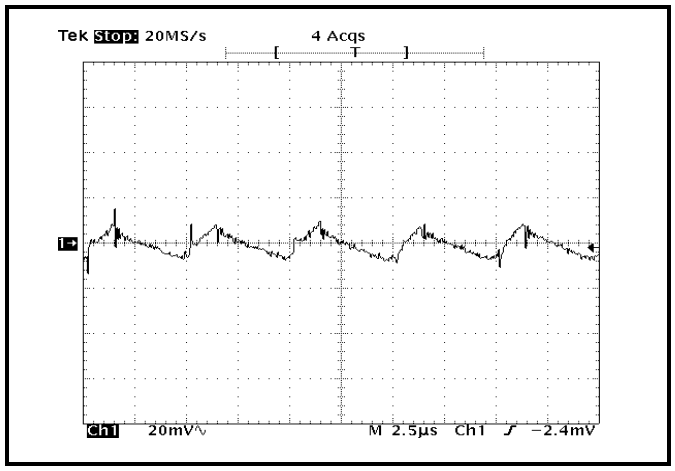

Fig. 3: V_{RIPPLE} @ V_{IN} = 12V, V_O = 3.3V, I_O = 10A

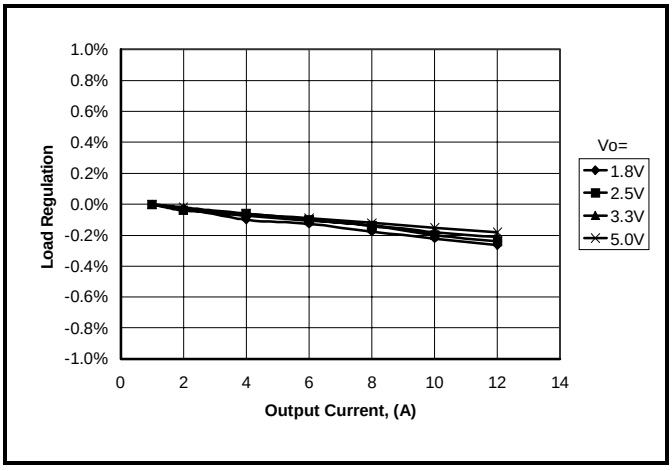

Fig. 4: Load Regulation @ V_{IN} = 12V

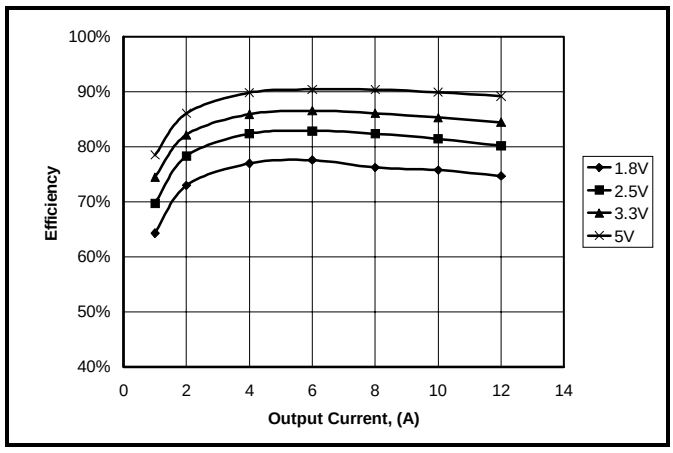

Fig. 5: Efficiency @ V_{IN} = 12V

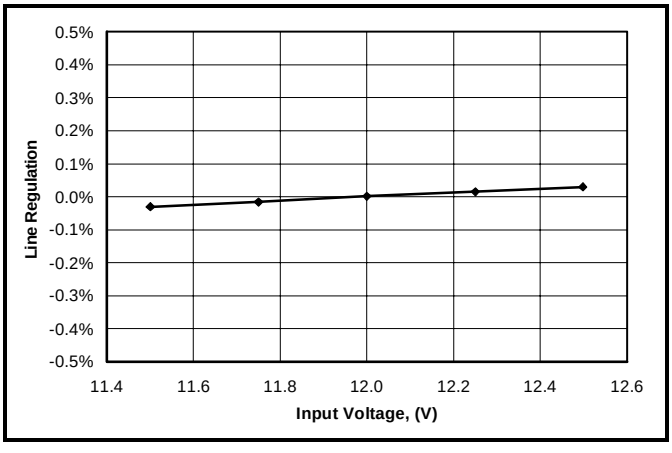

Fig. 6: Line Regulation @ V_O = 3.3V, I_O = 10A

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LAYOUT GUIDELINES

Careful attention to layout requirements are necessary for successful implementation of the SC1103 PWM controller. High currents switching at 200kHz are present in the application and their effect on ground plane voltage differentials must be understood and minimized.

1). The high power parts of the circuit should be laid out first. A ground plane should be used, the number and position of ground plane interruptions should be such as to not unnecessarily compromise ground plane integrity. Isolated or semi-isolated areas of the ground plane may be deliberately introduced to constrain ground currents to particular areas, for example the input capacitor and bottom Schottky ground.

2). The loop formed by the Input Capacitor(s) (Cin), the Top FET (Q1) and the Schottky (D1) must be kept as small as possible. This loop contains all the high current, fast transition switching. Connections should be as wide and as short as possible to minimize loop inductance. Minimizing this loop area will reduce EMI, lower ground injection currents, resulting in electrically "cleaner" grounds for the rest of the system and minimize source ringing, resulting in more reliable gate switching signals.

3). The connection between the junction of Q1, D1 and the output inductor should be a wide trace or copper region. It should be as short as practical. Since this connection has fast voltage transitions, keeping this connection short will minimize EMI. The connection between the output inductor and the sense resistor should be a wide trace or copper area, there are no fast voltage or current transitions in this connection and length is not so important, however adding unnecessary impedance will reduce efficiency.

4) The Output Capacitor(s) (Cout) should be located as close to the load as possible, fast transient load currents are supplied by Cout only, and connections between Cout and the load must be short, wide copper areas to minimize inductance and resistance.

5) The SC1103 is best placed over an isolated ground plane area. GND and PGND should be returned to this isolated ground. This isolated ground area should be connected to the main ground by a trace that runs from the GND pin to the ground side of (one of) the output capacitor(s). If this is not possible, the GND pin may be connected to the ground path between the Output Capacitor(s) and the Cin, Q1, D1 loop. Under no circumstances should GND be returned to a ground inside the Cin, Q1, D1 loop.

6) Vcc for the SC1103 should be supplied from the VIN supply through a 10Ω resistor, the Vcc pin should

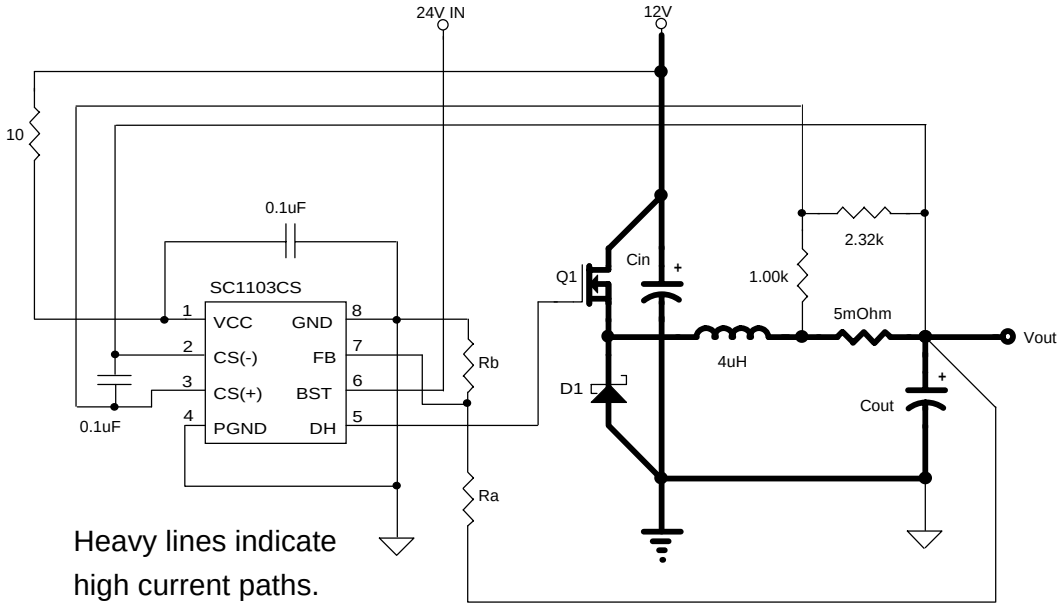

Fig. 7 Layout diagram for the SC1103

be decoupled directly to GND by a 0.1µF ceramic capacitor, trace lengths should be as short as possible.

7) The Current Sense resistor and the divider across it should form as small a loop as possible, the traces running back to CS(+) and CS(-) on the SC1103 should run parallel and close to each other. The 0.1µF capacitor should be mounted as close to the CS(+) and CS(-) pins as possible.

8) To minimize noise pickup at the sensitive FB pin, the feedback resistors should both be close to the SC1103 with the bottom resistor (Rb) returned to ground at the GND pin.

Under Voltage Lockout

The under voltage lockout circuit of the SC1103 assures that the high-side MOSFET driver outputs remain in the off state whenever the supply voltage drops below set parameters. Lockout occurs if V_{CC} falls below 3.8V. Normal operation resumes once V_{CC} rises above 3.8V.

TYPICAL APPLICATIONS

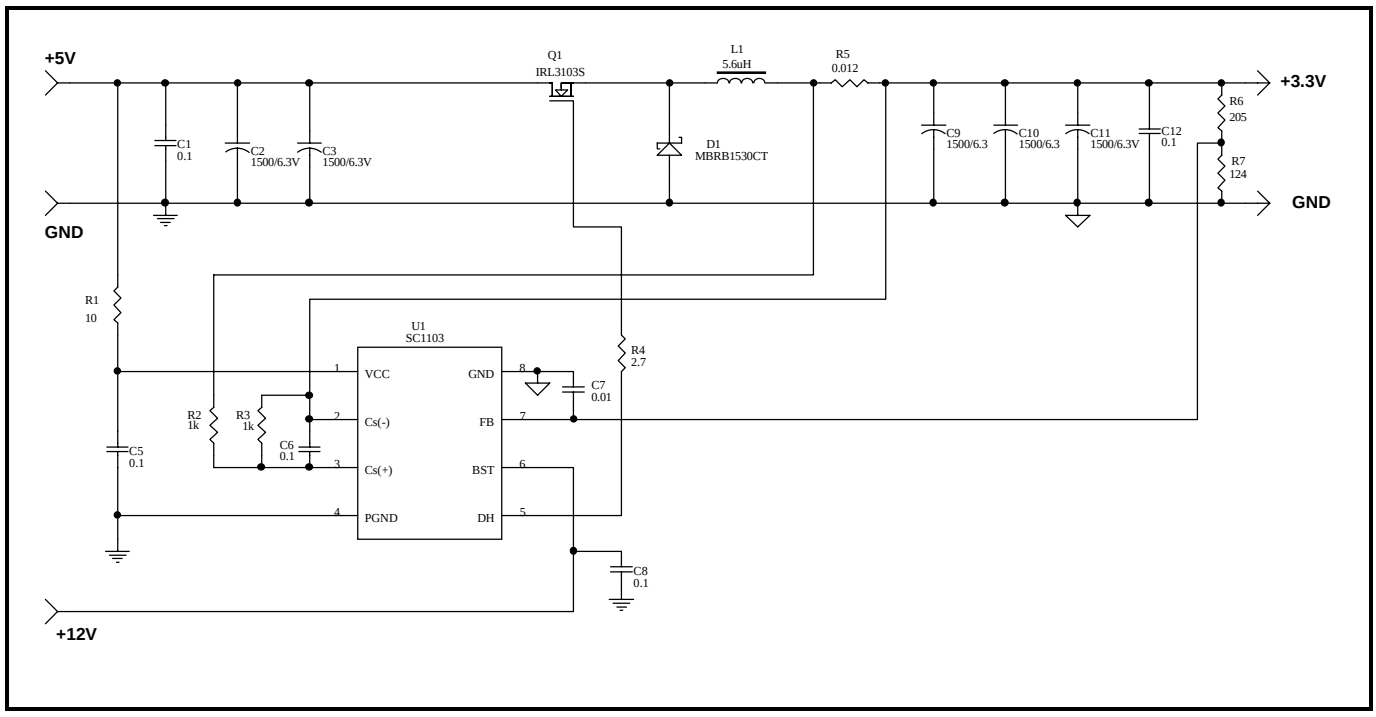

Fig. 8: 5V to 3.3V @ 8A

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TYPICAL APPLICATIONS (cont.)

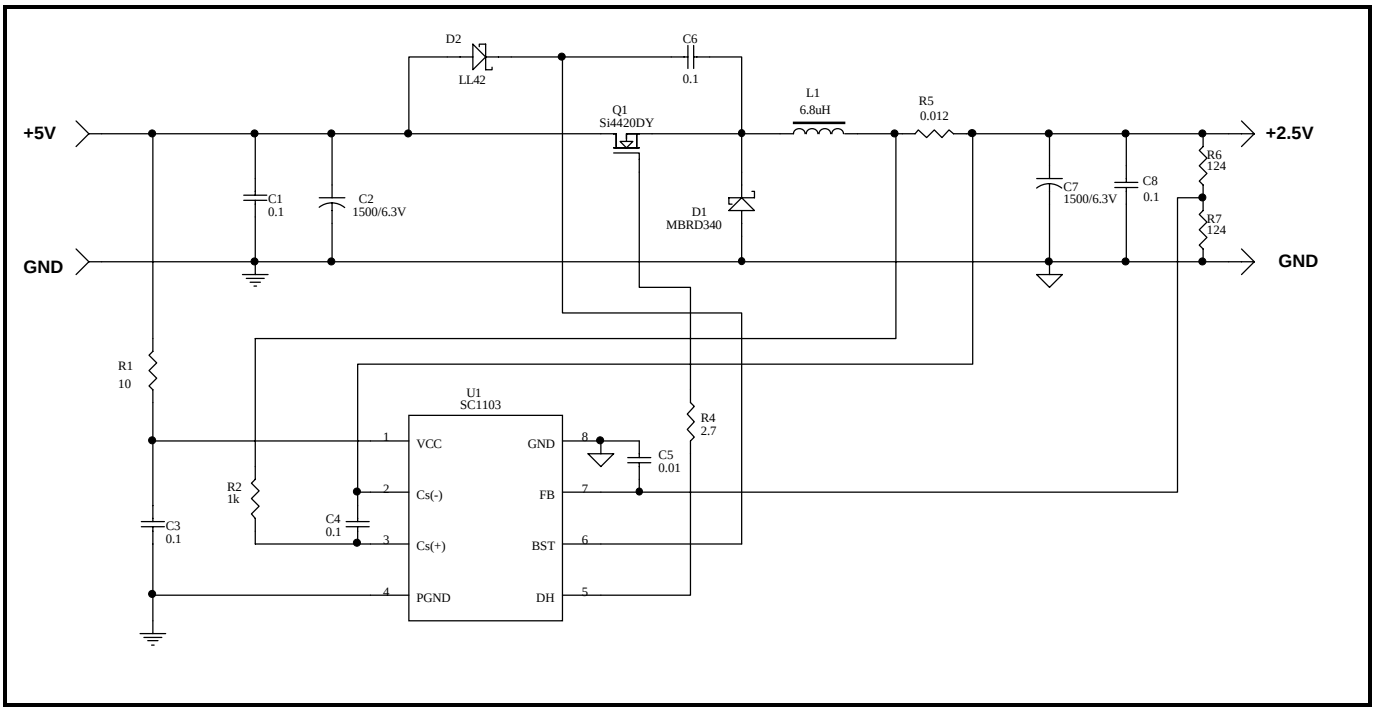

Fig. 9: 5V to 2.5V @ 4A with “flying capacitor” boost voltage.

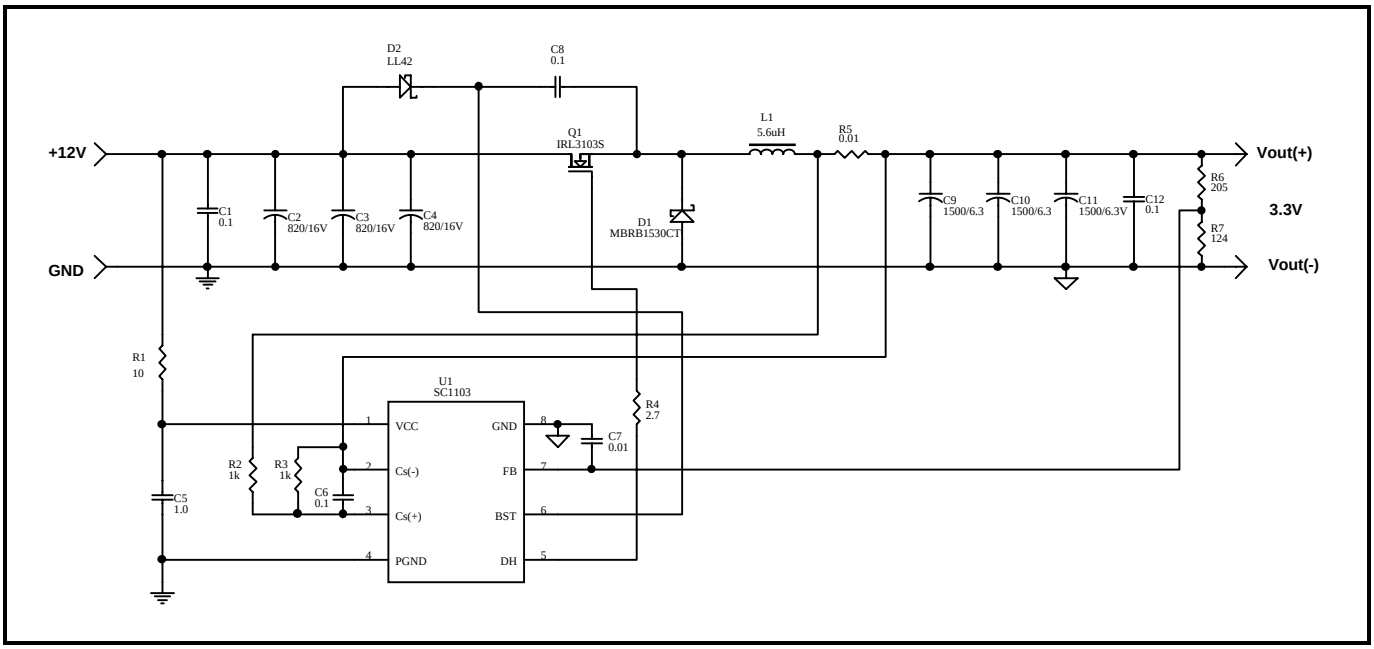

Fig. 10: 12V to 3.3V @ 10A with “flying capacitor” boost voltage.

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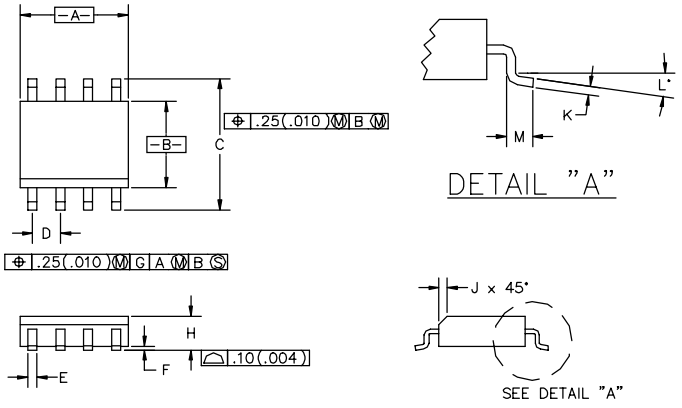
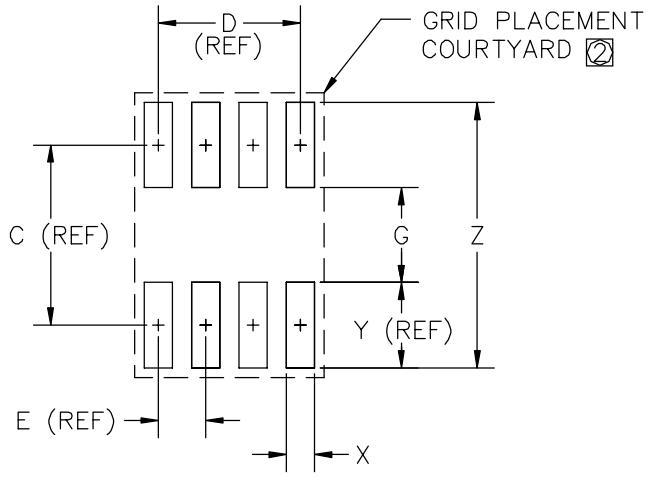
OUTLINE DRAWING

JEDEC
REF: MS-012AA



DIMENSIONS					
DIM N	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.188	.197	4.80	5.00	
B	.149	.158	3.80	4.00	
C	.228	.244	5.80	6.20	
D	.050	BSC	1.27	BSC	
E	.013	.020	0.33	0.51	
F	.004	.010	0.10	0.25	
H	.053	.069	1.35	1.75	
J	.011	.019	0.28	0.48	
K	.007	.010	.19	.25	
L	0°	8°	0°	8°	
M	.016	.050	0.40	1.27	

LAND PATTERN SO-8



DIMENSIONS (1)					
DIM N	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
C	–	.19	–	5.00	–
D	–	.15	–	3.81	–
E	–	.05	–	1.27	–
G	.10	.11	2.60	2.80	–
X	.02	.03	.60	.80	–
Y	–	.09	–	2.40	–
Z	–	.29	7.20	7.40	–

(2) GRID PLACEMENT COURTYARD IS 12x16 ELEMENTS (6 mm X 8mm) IN ACCORDANCE WITH THE INTERNATIONAL GRID DETAILED IN IEC PUBLICATION 97.

(1) CONTROLLING DIMENSION: MILLIMETERS

ECN00-899

