

### PROTECTION PRODUCTS

#### Description

The SDC15 transient voltage suppressor (TVS) is designed to protect components which are connected to data and transmission lines from voltage surges caused by ESD (electrostatic discharge), EFT (electrical fast transients), and lightning.

TVS diodes are characterized by their high surge capability, low operating and clamping voltages, and fast response time. This makes them ideal for use as board level protection of sensitive semiconductor components. The dual-junction common-cathode design allows the user to protect one data or power line operating at +/-12 volts. The low profile SOT23 package allows flexibility in the design of "crowded" circuit boards.

The SDC15 TVS will meet the surge requirements of IEC 61000-4-2 (Formerly IEC 801-2), Level 4, "Human Body Model" for air and contact discharge.

#### Features

- ◆ 300 watts peak pulse power ( $t_p = 8/20\mu s$ )
- ◆ 40 watts peak pulse power ( $t_p = 10/1000\mu s$ )
- ◆ Transient protection for data & power lines to **IEC 61000-4-2 (ESD) 15kV (air), 8kV (contact)**  
**IEC 61000-4-4 (EFT) 40A (5/50ns)**  
**IEC 61000-4-5 (Lightning) 12A (1.2/50 $\mu s$ )**
- ◆ Protects one bidirectional line
- ◆ Low clamping voltage
- ◆ Low leakage current
- ◆ High surge capability
- ◆ Solid-state silicon avalanche technology

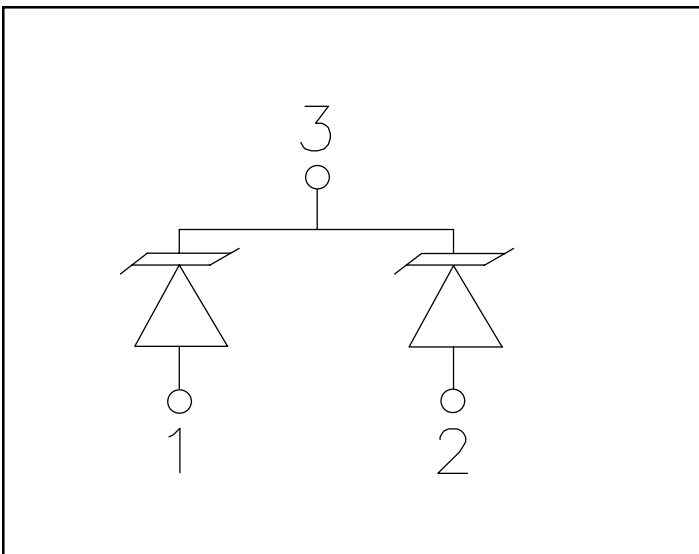
#### Mechanical Characteristics

- ◆ JEDEC SOT23 package
- ◆ Molding compound flammability rating: UL 94V-0
- ◆ Marking : DC15
- ◆ Packaging : Tape and Reel per EIA 481

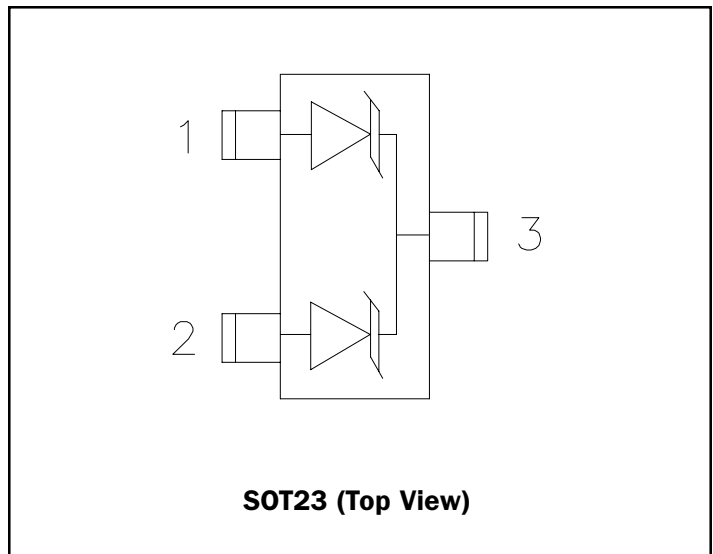
#### Applications

- ◆ RS-232 Data Lines
- ◆ Portable Electronics
- ◆ Industrial Controls
- ◆ Set-Top Box
- ◆ Servers, Notebook, and Desktop PC
- ◆ 12V DC Supply Protection

#### Circuit Diagram



#### Schematic & PIN Configuration



**PROTECTION PRODUCTS**
**Absolute Maximum Rating**

Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20μs)	$P_{pk}$	300	Watts
Peak Pulse Current (tp = 8/20μs)	$I_{pp}$	10	A
Non-Repetitive Peak Forward Current (tp=100us)	$I_{FSMAX}$	4	A
Thermal Resistance, Junction to Ambient	$\theta_{JA}$	556	°C/W
Lead Soldering Temperature	$T_L$	260 (10 sec.)	°C
Operating Temperature	$T_J$	-55 to +125	°C
Storage Temperature	$T_{STG}$	-55 to +150	°C

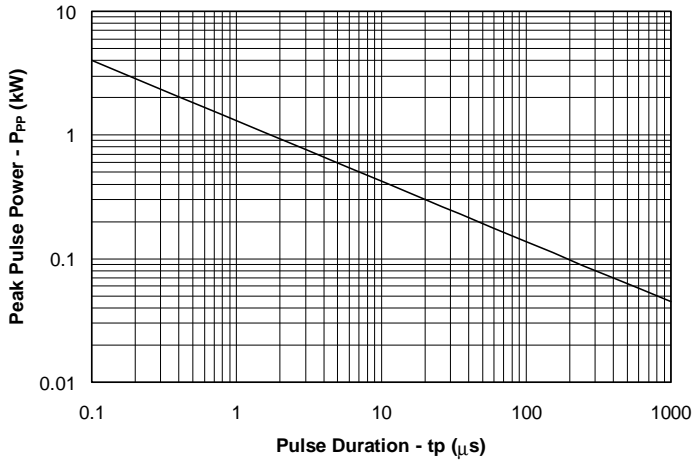
**Electrical Characteristics**

<b>SDC15</b>						
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	$V_{RWM}$				12.8	V
Reverse Breakdown Voltage	$V_{BR}$	$I_f = 1mA$ , Between Pin 1 & 2 (each direction)	14.3		16.4	V
Reverse Leakage Current	$I_R$	$V_{RWM} = 12.8V$ , $T=25^\circ C$ Between Pin 1 & 2 (each direction)			100	nA
Forward Voltage	$V_F$	$I_f = 100mA$ , Pin 1 to 3 and Pin 2 to 3			1.3	V
Temperature Coefficient of VBR	$\alpha VBR$				12	mV/°C
Clamping Voltage	$V_C$	$I_{pp} = 1.9A$ , tp = 10/10000μs Between Pin 1 & 2 (each direction)			21.2	V
Junction Capacitance	$C_J$	$V_R = 0V$ , f = 1MHz Pin 1 to 2			120	pF

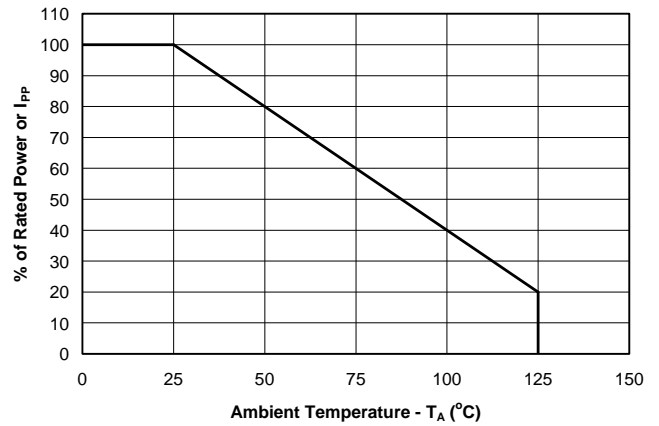
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Typical Characteristics

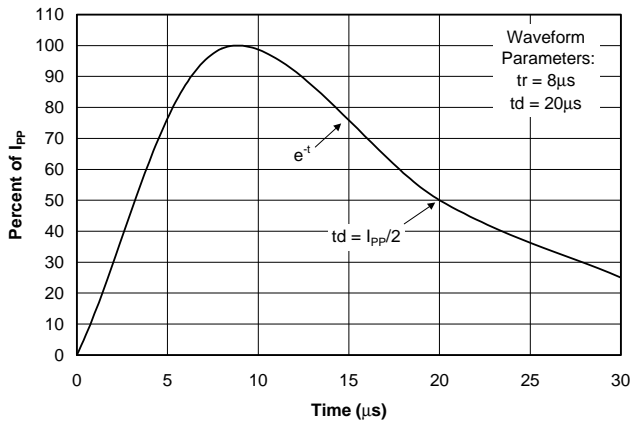
Non-Repetitive Peak Pulse Power vs. Pulse Time



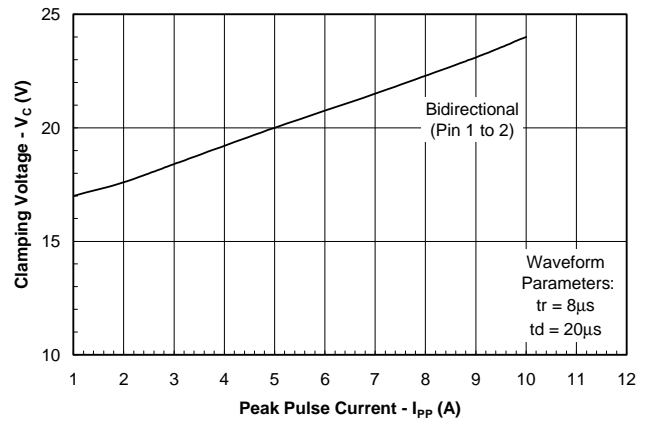
Power Derating Curve



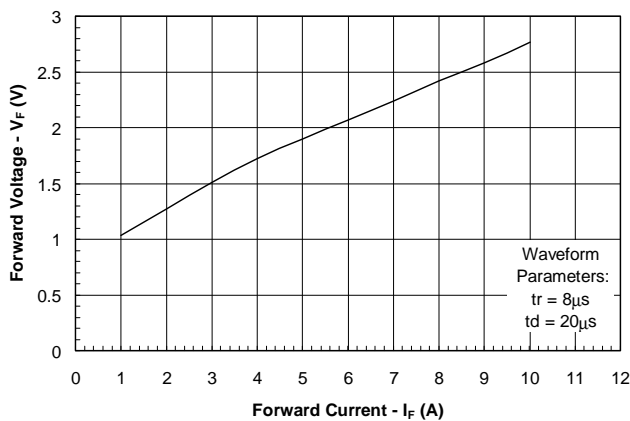
Pulse Waveform



Clamping Voltage vs. Peak Pulse Current



Forward Voltage vs. Forward Current



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**Applications Information**

**Device Connection for Protection of One Data Line**

The SDC15 is designed to protect one data or I/O line operating at +/- 12 volts. Connection options are as follows:

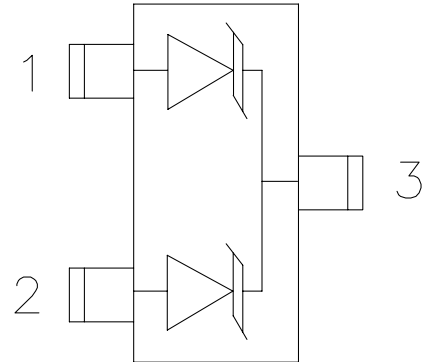
- Common mode protection: Pin 1 is connected to the data line and pin 2 is connected to ground. For best results, this pin should be connected directly to a ground plane on the board. The path length should be kept as short as possible to minimize parasitic inductance. Pin 3 is not connected.
- Differential protection: Pin 1 is connected to one line and pin 2 is connected to the second line. Pin 3 is not connected.

**Circuit Board Layout Recommendations for Suppression of ESD.**

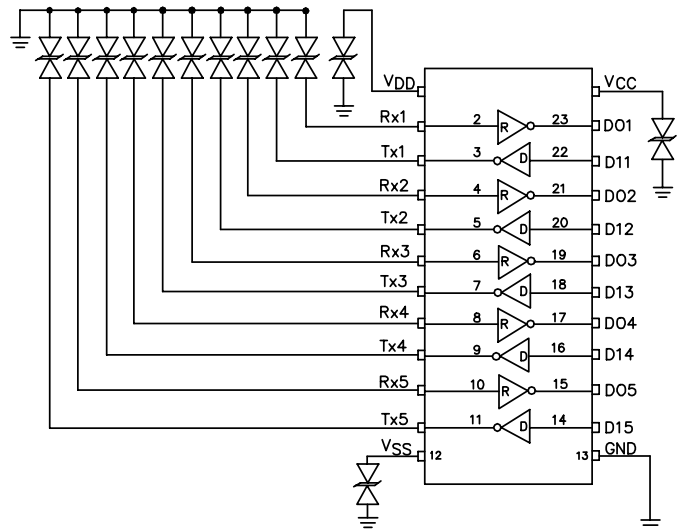
Good circuit board layout is critical for the suppression of fast rise-time transients such as ESD. The following guidelines are recommended:

- Place the SDC15 near the input terminals or connectors to restrict transient coupling.
- Minimize the path length between the SDC15 and the protected line.
- Minimize all conductive loops including power and ground loops.
- The ESD transient return path to ground should be kept as short as possible.
- Never run critical signals near board edges.
- Use ground planes whenever possible.

**Device Schematic & Pin Configuration**

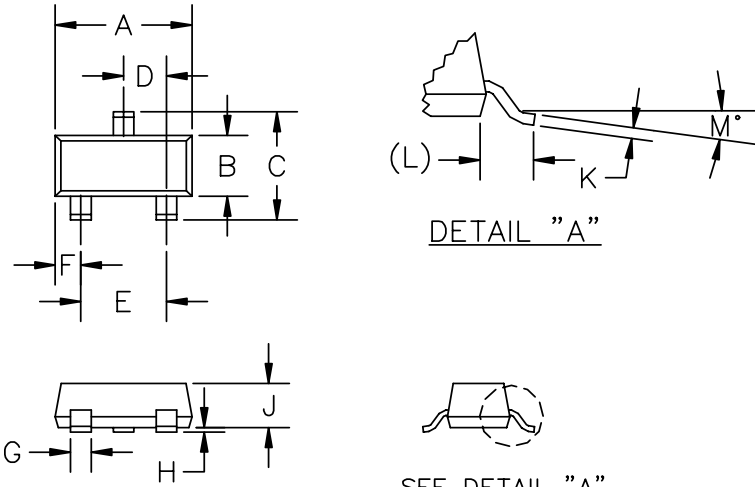


**RS-232 Transceiver Protection Example**



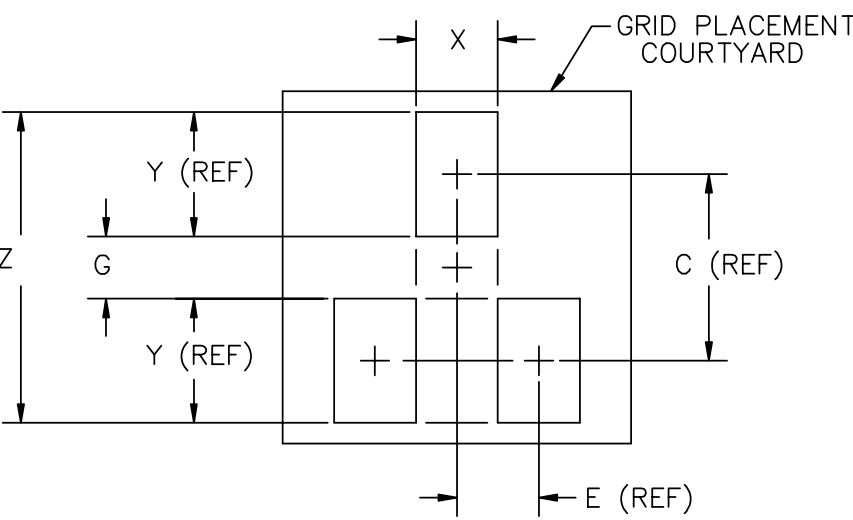
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Outline Drawing - SOT23



DIM <sup>N</sup>	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.110	.119	2.8	3.04	—
B	.047	.055	1.20	1.40	—
C	.083	.104	2.10	2.64	—
D	.035	.040	0.88	1.02	—
E	.070	.081	1.78	2.05	—
F	.017	.024	.44	.60	—
G	.014	.020	.37	.51	—
H	.0005	.004	.013	0.10	—
J	.034	.040	.87	1.02	—
K	.003	.007	.085	.180	—
L	—	.022	—	0.55	REF
M	0	8°	0	8°	—

Land Pattern - SOT23



DIM <sup>N</sup>	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
C	—	.09	—	2.20	—
E	—	.04	—	.95	—
G	.03	.04	.80	1.00	—
X	.03	.04	.80	1.00	—
Y	—	.06	—	1.40	—
Z	.14	.15	3.40	3.60	—

Note 1 : Grid placement courtyard is 8 x 8 elements (4mm x 4mm) in accordance with the international grid detailed in IEC Publication 97.

**PROTECTION PRODUCTS****Ordering Information**

<b>Part Number</b>	<b>Working Voltage</b>	<b>Qty per Reel</b>	<b>Reel Size</b>
SDC15.TC	12.8V	3,000	7 Inch
SDC15.TG	12.8V	10,000	13 Inch

**Contact Information**

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