Edge647
Pin Electronics Driver, Window Comparator, and Switch Matrix

EDGE HIGH-PERFORMANCE PRODUCTS

Description

The Edge647 is an integrated trinary driver, window comparator, and switch matrix pin electronics solution manufactured in a wide voltage CMOS process. It is designed for automatic test equipment and instrumentation where cost, functional density, and power are all at a premium.

The tristatable driver is capable of generating 3 levels - one for a logic high, one for a logic low, and one for either a termination voltage or a special programming voltage.

The on-board window comparator effectively determines whether the DUT is in a high, low, or intermediate state.

The switches are included to allow such functions as PMU, pull up, and pull down connections.

The Edge647 is intended to offer an extremely low leakage, low cost, low power, small footprint, per pin solution for 100 MHz and below pin electronics applications. It is a higher performance, pin and functionally compatible version of the Edge646.

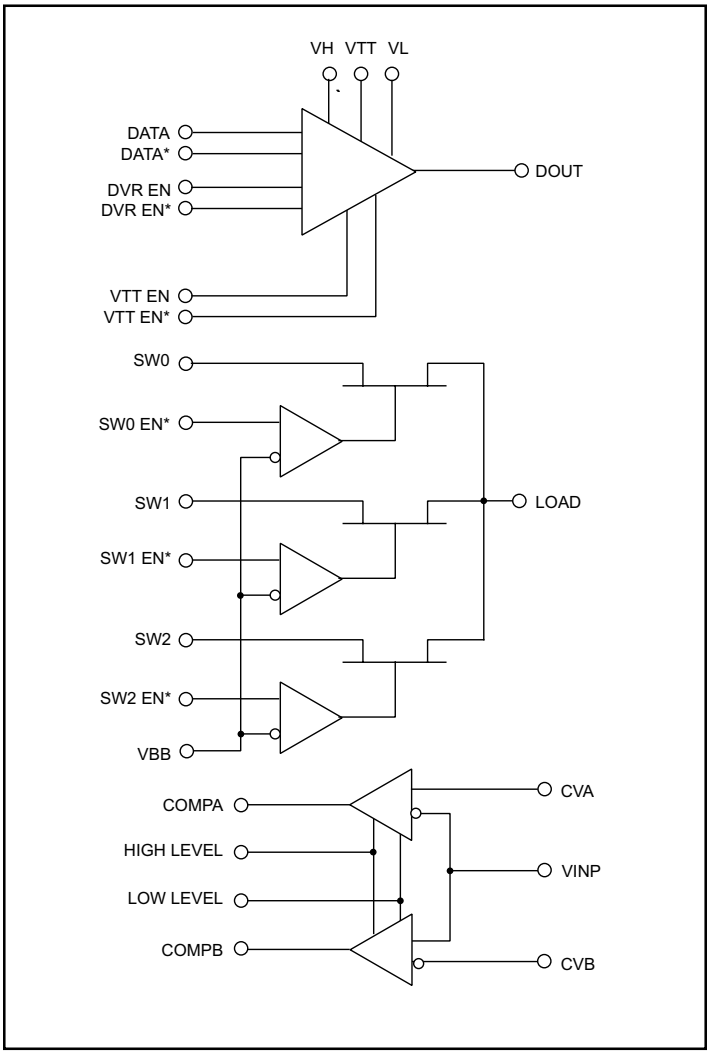
Features

- Pin Compatible with the Edge646
- 100 MHz Operation
- 12V I/O Range
- Programmable Output Levels
- Flex In digital Inputs (Technology Independent)
- Three Level Driver
- Extremely Low Leakage Currents (~0 nA)
- Small Footprint (32 Pin, 7 mm X 7 mm, TQFP Package)

Applications

- Low Cost Automatic Test Equipment

Functional Block Diagram

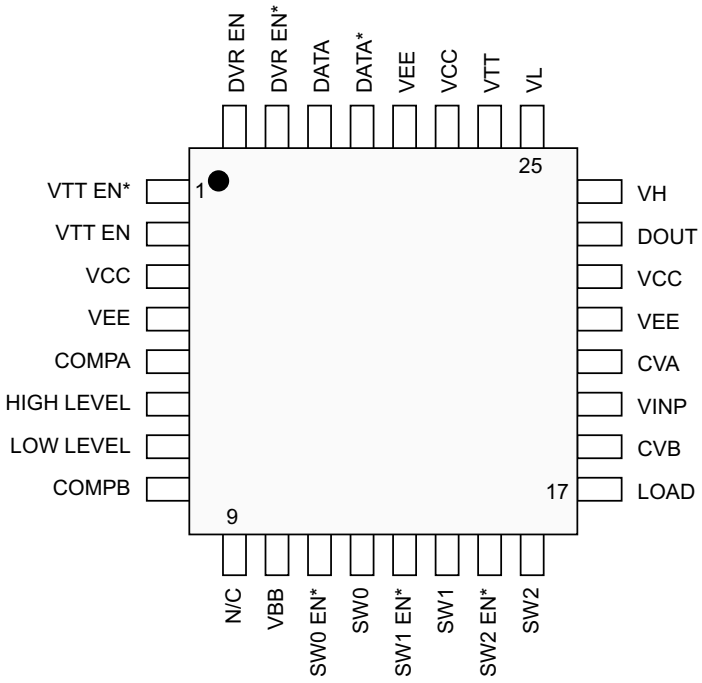


PIN Description

Pin Name	Pin #	Description
Driver		
DATA / DATA*	30, 29	Digital input that determines the high/low status of the driver when it is enabled.
DVR EN / DVR EN*	32, 31	Digital input that enables and disables the driver, or places the driver in the VTT state.
VTT EN / VTT EN*	2, 1	Digital input that determines whether DVR EN* places the driver in a high impedance state or actively drives to the VTT level.
DOUT	23	Driver Output.
VH, VL, VTT	24, 25, 26	Unbuffered analog inputs that set the voltage level of a logical 1, 0, or VTT at the driver output.
VBB	10	Analog input pin which establishes the threshold for all single-ended digital input signals.
Comparator		
VINP	19	Analog window comparator input.
CVA, CVB	20, 18	Analog DC comparator inputs that set the threshold levels for teh window comparator.
COMPA, COMPB	5, 8	Digital comparator outputs.
LOW LEVEL HIGH LEVEL	7 6	Voltage inputs that establish the digital low and high levels of the comparator outputs.
Switch Matrix		
SW0 EN*, SW! EN* SW2 EN*	11, 13 15	TTL compatible inputs that activate switches 0, 1, 2, and 3.
SW0 SW1 SW2	12 14 16	Switch 0 Switch 1 Switch 2
LOAD	17	Input pin that connects the DUT to the analog switches.
Power Supplies		
VCC	3, 22, 27	Positive analog power supply.
VEE	4, 21, 28	Negative analog power supply.
N/C	9	No Connect pin (leave floating).

PIN Description *(continued)*

32-Pin, 7mm x 7mm TQFP



Circuit Description

Driver Description

The Edge647 driver supports three distinct programmable driver levels; high, low, and termination, and high impedance. There are no restrictions between any of these three levels in that all three may vary independently over the entire operating voltage range between VCC and VEE.

The DVR EN*, DATA, and VTT EN pins are digital inputs that control the driver (see Table 1). With DVR EN* low, DATA determines whether the driver will force VH or VL at DOUT. With DVR EN* high, VTT EN* controls whether the driver goes into high impedance or drives VTT.

DVR EN*	VTT EN	DATA	DOUT
1	0	X	HiZ
1	1	X	VTT
0	X	0	VL
0	X	1	VH

Table 1. Driver Truth Table

VH, VL, and VTT

VH, VL, and VTT define the logical “1”, “0”, and “termination” levels of the driver and can be adjusted anywhere over the range spanned by VCC to VEE. There is no restriction between VH, VL, and VTT, in that they can all vary independently over the entire voltage range determined by the power supply levels.

The VH, VL, and VTT inputs are unbuffered in that they also provide the driver output current, so the sources of these voltages must have ample current drive capability.

While VTT is referred to as the termination voltage, it may also be used as a very high “programming” level on many memory devices.

Driver Output Protection

The Edge647 is designed to operate in a functional testing environment where a controlled impedance (typically 50 Ω) is maintained between the pin electronics and the DUT. In general, there will be an external resistor at the driver output which series terminates the transmission line to the DUT. In this environment, the driver can withstand a short to any legal DUT voltage for an indefinite period.

In a low impedance application with no additional output series resistance, care must be exercised and systems should be designed to check for this condition and tristate the driver if a short is detected.

The driver does NOT have on-chip short circuit protection or limitation circuitry.

VBB

VBB is an analog input which establishes the threshold for all single ended digital input signals. If SW0 EN*, SW1 EN*, or SW2 EN* are more positive than VBB, these inputs are a digital “1". Conversely, if they are more negative than VBB, they are a “0".

All digital inputs are wide voltage comparator inputs, so they are technology independent. By establishing the appropriate VBB level for the switch control inputs, and the appropriate differential input levels for the driver digital control inputs, the Edge647 may be driven by TTL, ECL, CMOS, or any custom level circuitry.

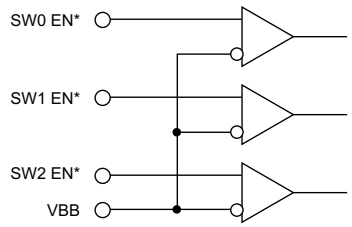


Figure 1. Driver Digital Inputs

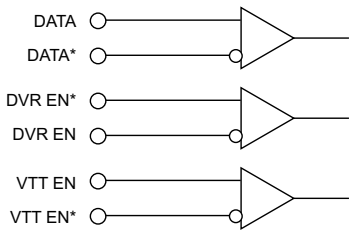


Figure 2. Driver Differential Digital Inputs

Circuit Description *(continued)*

Receiver Functionality

The Edge647 supports an on-board window comparator. CVB and CVA are high impedance analog inputs which establish the threshold voltages. COMPA and COMPB are the digital outputs which reflect the real time status of VINP. Table 2 summarizes the relationship between the threshold levels, VINP, and the output signals.

VINP	COMPA	COMPB
VINP < CVA VINP > CVA	1 0	X X
VINP < CVB VINP > CVB	X X	0 1

Table 2. Comparator Truth Table

Comparator Outputs

The comparator outputs are 50 Ω output impedance non-tristatable drivers designed to cleanly drive 50 Ω transmission lines without requiring any external series termination resistors. Input pins LOW LEVEL and HIGH LEVEL establish the logic 0 and 1 levels respectively. In normal operation, LOW LEVEL would be connected to ground and HIGH LEVEL would be connected to a system VDD supply, producing CMOS digital swings at the output.

However, the comparator outputs are technology independent in that they can drive PECL, 3V CMOS, ECL, LV CMOS, GTL, and custom levels by varying LOW LEVEL and HIGH LEVEL. For example, should a 3V swing be desired, HIGH LEVEL could be connected to a 3.0V power supply.

Notice that HIGH LEVEL and LOW LEVEL provide both the voltage level and the current for the comparator outputs. HIGH LEVEL and LOW LEVEL may be varied between +5V and -2V.

Load

The Edge647 provides a total of 3 analog switches. Individual switches vary in both their on resistance and their on/off time (see Table 4).

Like the driver digital inputs, the switch matrix control inputs SW0-3 EN* are technology independent as VBB determines their threshold level. The switch control is documented in Table 3.

Control Inputs	Status
SW0 EN* = 1 SW0 EN* = 0	SW0 disconnected SW0 connected
SW1 EN* = 1 SW1 EN* = 0	SW1 disconnected SW1 connected
SW EN* = 1 SW2 EN* = 0	SW2 disconnected SW2 connected

Table 3. Switch Matrix Truth Table

Switch	Rout	On/Off Time
SW0	50 Ω	100 ns
SW1	50 Ω	100 ns
SW2	50 Ω	100 ns

Table 4. Switch Matrix Characteristics

Do NOT leave any digital input pins floating.

Power Supplies Decoupling

A .1 µF capacitor is recommended between VCC and VEE.

In addition, solid VCC and VEE planes are recommended to provide a low inductance path for the power supply currents. These planes will reduce any inductive supply drops associated with switching currents on the power supply pins. If solid planes are not possible, then wide power busses are preferable.

VH, VL, and VTT Decoupling

As the VH, VL, and VTT inputs are unbuffered and must supply the driver output current, decoupling capacitors for these inputs are recommended in proportion to the amount of output current the application requires. In general, a surge current of 50 mA (5V swings series terminated with 50 Ω into a 50Ω transmission line) are the maximum dynamic output currents the driver should see. The decoupling capacitors should be able to provide this current for the duration of the round trip time between the pin electronics and the DUT, and then recharge themselves before the next such transition would occur. Once this condition is satisfied, the VH, VL, and VTT supply voltages are more responsible for establishing the DC levels associated with each function and recharging the capacitors, rather than providing the actual dynamic currents required to drive the DUT transmission line.

Ideally, VH, VL, and VTT would each have a dedicated power layer on the PC board for the lowest possible inductance power supply distribution.

Power Supply Rules

1) VEE ≤ All I/O Pins ≤ VCC
2) VCC ≥ 0V
3) VEE ≤ 0V

Power Up Sequencing

1) VCC (all other inputs @ ground)
2) VEE (all other inputs @ ground)
3) Digital Inputs
   Analog Inputs
   VH, VL, VTT

Latchup Protection

The Edge647 has several power supply requirements to protect the part in power supply fault situations, as well as during power up and power down sequences. VCC must remain greater than or equal to VDD (external supply for the digital logic) at all times. Both VCC and VDD must always be positive (above ground), and VEE must always be negative (at or below ground).

The three diode configuration shown in Figure 3 should be used on a once-per-board basis.

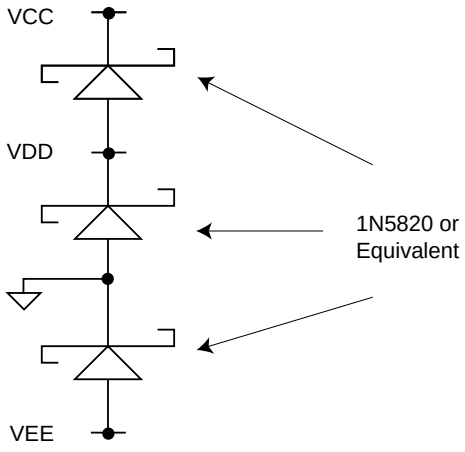
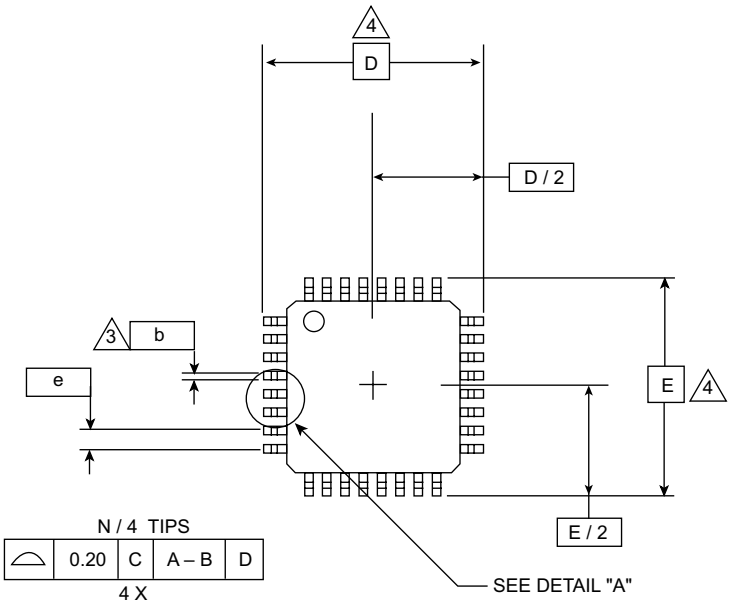


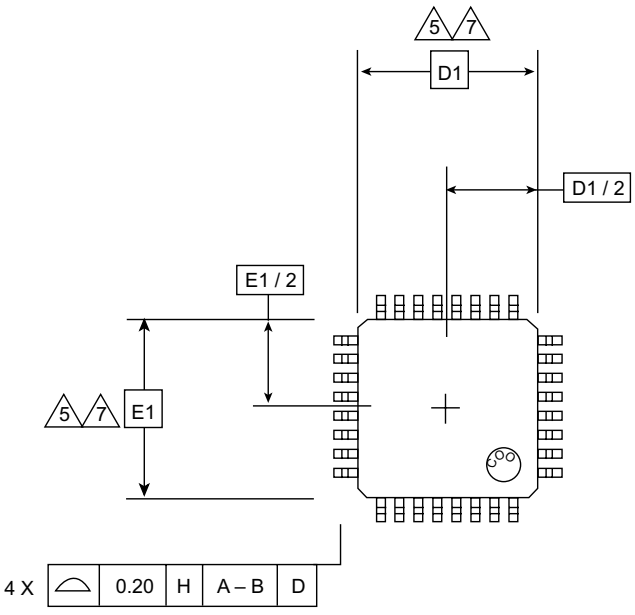
Figure 3.
Power Supply Protection Scheme

Warning: It is extremely important that the voltage on any device pin does not exceed the range of VEE –0.5V to VCC +0.5V at any time, either during power up, normal operation, or during power down. Failure to adhere to this requirement could result in latchup of the device, which could be destructive if the system power supplies are capable of supplying large amounts of current. Even if the device is not immediately destroyed, the cumulative damage caused by the stress of repeated latchup may affect device reliability.

TOP VIEW

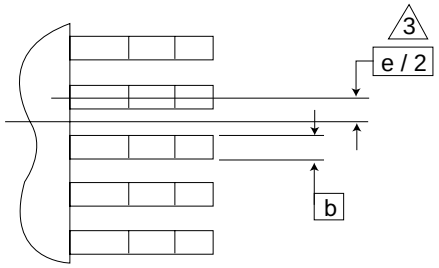


BOTTOM VIEW

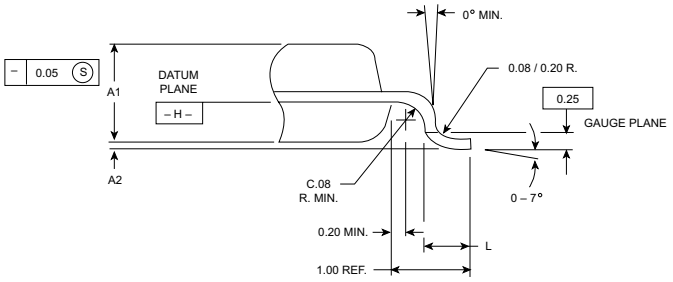


Package Information *(continued)*

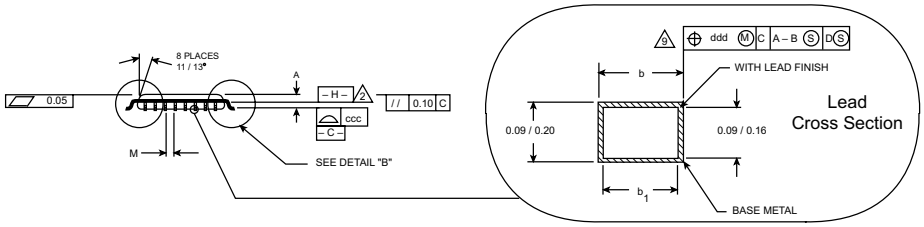
DETAIL "A"



DETAIL "B"



SECTION C–C



Notes:

1. All dimensions and tolerances conform to ANSI Y14.5-1982.
2. Datum plane -H- located at mold parting line and coincident with lead, where lead exits plastic body at bottom of parting line.
3. Datums A-B and -D- to be determined at centerline between leads where leads exit plastic body at datum plane -H-.
4. To be determined at seating plane -C-.
5. Dimensions D1 and E1 do not include mold protrusion.
6. "N" is the total # of terminals.
7. These dimensions to be determined at the datum plane -H-.
8. Package top dimensions are smaller than bottom dimensions and top of package will not overhang bottom of package.
9. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot.
10. Controlling dimension: millimeter.
11. Maximum allowable die thickness to be assembled in this package family is 0.30 millimeters.
12. This outline conforms to JEDEC publication 95, registration MO-136, variations AC, AE, and AF.

	JEDEC VARIATION All Dimensions in Millimeters			
	AC			
	Min.	Nom.	Max.	Note
A			1.60	
A1	0.05	0.10	0.15	
A2	1.35	1.40	1.45	
D		9.00 BSC.		4
D1		7.00 BSC.		7,8
E		9.00 BSC.		4
E1		7.00 BSC.		7,8
L	0.45	0.60	0.75	
M	0.15			
N	32			
e		0.80 BSC.		
b	0.30	0.37	0.45	9
b1	0.30	0.35	0.40	
ccc			0.10	
ddd			0.20	

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Positive Analog Power Supply	VCC	6	8	12	V
Negative Analog Power Supply	VEE	-5	-4	-3	V
Total Analog Power Supply	VCC - VEE	9		12	V
Comparator Output High Level	HIGH LEVEL	-2		+5	V
Comparator Output Low Level	LOW LEVEL	-2		+5	V
Junction Temperature	TJ			+125	^{o}C

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
Total Analog Power Supply	VCC - VEE	0		13	V
Positive Analog Power Supply	VCC	0		13	V
Negative Analog Power Supply	VEE	-6		0	V
Analog Input Voltages		VEE - .5		VCC + .5	V
Digital Inputs		VEE - .5		VCC + .5	V
Ambient Operating Temperature	TA	-55		+125	^{o}C
Storage Temperature		-65		+150	^{o}C
Junction Temperature	TJ			+150	^{o}C
Soldering Temperature				260	^{o}C

Stresses above listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Driver/Receiver Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Driver					
Programmable Driver Output Voltages	VH, VL, VTT	VEE		VCC	V
Driver Output Swing	VH - VL	VEE - VCC		VCC - VEE	V
	VH - VTT	VEE - VCC		VCC - VEE	V
	VTT - VLL	VEE - VCC		VCC - VEE	V
DC Driver Output Current	Iout DC	-50		+50	mA
Output Impedance	Rout	21	25	31	Ω
DUT Pin Capacitance	Cout		13		pF
HiZ Leakage Current (Note 1)	Ileak		0	4	nA
Comparator					
Input Voltage	VINP	VEE		VCC	V
Input Leakage Current (Note 4)	IBIAS		0	2	nA
Input Capacitance	Cin		4		pF
Offset Voltage (Note 2)	VOS	-75		+75	mV
Receiver Threshold (Note 2)		VEE + 2.0		VCC - 1.0	V
Threshold Bias current (Note 1)	CVA, CVB		0	10	nA
Digital Output High Level	HIGH LEVEL	-2		5	V
Digital Output Low Level	LOW LEVEL	-2		5	V
Digital Output Impedance (Note 3)	Rout	40	47	56	Ω
Digital Output Current Drive	Imax	-50		+50	mA
Analog Switches (SW0, SW1, SW2)					
On Resistance	Ron	40	47	54	Ω
Voltage Range		VEE		VCC	V
LOAD HiZ Leakage Current (Note1)			0	4	nA
DC Current Rating		-30		+30	mA
SW Capacitance			10		pF
Total Power Supply					
Quiescent Positive Supply Current	ICC_DC	75	95	105	mA
Quiescent Negative Supply Current	IEE_DC	-105	-95	-75	mA
Total Leakage (Note 4) (DOUT + VINP + LOAD)			0	10	nA
Total Capacitance (Note 1) (DOUT + VINP + LOAD)			27		pF

DC Characteristics *(continued)*

Digital Inputs
DATA / DATA*, DVR EN* / DVR EN, VTT EN / VTT EN*
SW0 EN*, SW1 EN*, SW2 EN*, SW3 EN*

Parameter	Symbol	Min	Typ	Max	Units
Input High Voltage	Input - Input*	.8		5	V
Input Low Voltage	Input* - Input	.8		5	V
Input Current	IIN		0	1.0	µA
Input Capacitance	DATA DRV EN VTT EN			8 8 8	pF pF pF
Digital Input Voltage Range	INPUT, INPUT*	-2.0*		+5.0	V
Digital Input Threshold	VBB	-1.4		4.4	V

*-2V or (VEE + 2.0V), whichever is more positive.

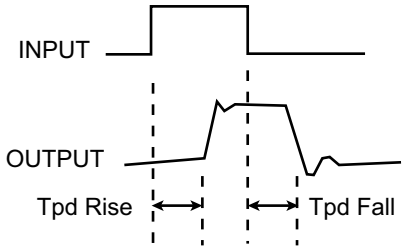
Note 1: This parameter is guaranteed by design and characterization. Production testing is performed against a ± 250 nA limit.
Note 2: Measured at 0V.
Note 3: Measured at HIGH LEVEL = +3.3V, LOW LEVEL = 0V.
Note 4: Production tested at +5V and 0V against ± 10 nA limits. Also tested at VCC and VEE against ± 250 nA limits.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Driver					
Propagation Delay (Note 3)					
DATA IN to DOUT		4	6	10	ns
VTT EN to DOUT		5	7	11	ns
DVR EN* to DOUT (Active to HiZ) (Note 5)		5	7	11	ns
DVR EN* to DOUT (HiZ to Active) (Note 5)		5	7	11	ns
DATA to VTT Prop Delay Matching (Note 4)		-2		+2	ns
Minimum Pulse Width (3V Swing)			4	5	ns
Toggle Rate (Note 6)	Fmax	100			MHz
DOUT Output Rise/Fall Times (Notes 1, 4)					
1V Swing (20% - 80%)			1.2	1.6	ns
3V Swing (10% - 90%)		1.0	1.5	2.0	ns
5V Swing (10% - 90%)			2.0	3.5	ns
DOUT Output Overshoot/Undershoot (Notes 1, 4)					
(3V Swing (Swing 2% + 50 mV))				110	mV
ΔTpd vs. Overdrive (1.8V) (Note 4)				100	ps
ΔTpd vs. ΔTr/ΔTf @ Digital Inputs (Note 4)				50	ps
ΔTpd vs. Frequency (<=100 MHz) (Note 4)				200	ps
Tpd Rise, Tpd Fall Errors (Note 4)				2.0	ns
Comparator					
Comparator Digital Outputs (Notes 2, 4)					
Rise Time (10% - 90%)	tr		1.5	2.5	ns
Fall time (10% - 90%)	tf		1.5	2.5	ns
VINP to COMPA, COMPB	Tpd	5	7	11	ns
ΔTpd vs. Frequency (<= 100 MHz) (Note 4)				200	ps
Minimum Pulse Width			4	5	ns
Toggle Rate (Note 6)	Fmax	100			MHz
Comparator Uncertainty Region (Notes 4, 7)		-25		+25	mV
ΔTpd vs. Overdrive					
400 mV Overdrive				1.0	ns
200 mV Overdrive				2.0	ns
Tpd Rise, Tpd Fall Errors				2.0	ns
Switch Matrix					
SW0, 1, 2 EN* to Switch On/Off		8	25	60	ns

Note 1: Into 1M of 50Ω transmission line terminated with 1KΩ and 5 pF with the proper series termination resistor.
Note 2: LOW LEVEL = 0V, HIGH LEVEL = 3.3V.
Note 3: Measured at 2.5V with VH = +5V, VL = 0V.
Note 4: Guaranteed by design and characterization. This parameter is not tested in production.
Note 5: Tested with a 30 mA load.
Note 6: Guaranteed by characterization. This parameter is tested in production against 40 MHz limits.
Note 7: The region around the threshold where the comparator may have difficulty resolving the input state.

AC Characteristics *(continued)*



| Tpd Rise – Tpd Fall | ≤ 2.0 ns

Figure 4. Tpd Rise, Tpd Fall Errors

Ordering Information

Model Number	Package
E647ATF	32-Pin TQFP
EVM647ATF	Edge647 Evaluation Module

Contact Information

Semtech Corporation
Edge High-Performance Division
10021 Willow Creek Rd., San Diego, CA 92131
Phone: (858)695-1801 FAX (858)695-2633