Edge692
200 MHz Monolithic Dual Pin Electronics Driver

EDGE HIGH-PERFORMANCE PRODUCTS

Description

The Edge692 is a dual pin electronics driver manufactured in a high-performance, complementary bipolar process. In Automatic Test Equipment (ATE) applications, the Edge692 offers two pin drivers suitable for drive-only channels in memory testers, as well as for bidirectional channels in memory, VLSI, and mixed- signal test systems.

The Edge692 is designed to produce excellent waveforms (low overshoot), especially at low swings (<500 mV), and have extremely low leakage currents in HiZ mode. In addition, the Edge692 is pin and functionally compatible with both the Edge693 and the Bt692.

Each driver is capable of forcing 9V signals over a 12V range, in addition to going into a high impedance state. The driver slew rate is adjustable between 2 V/ns and 1 V/ns.

Each driver is completely isolated from the other. There are separate data, enable, slew rate adjust, high and low levels, as well as power supply inputs for each driver.

Combining two independent drivers into a 28 pin PLCC package offers a highly integrated solution where speed and density are at a premium.

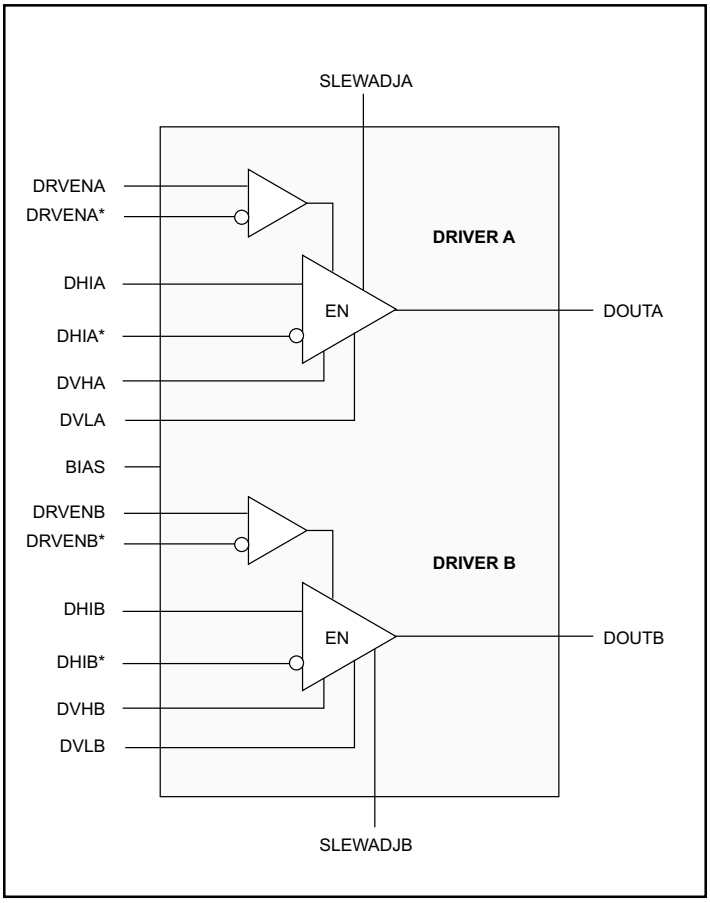
Features

- 2 V/ns Driver Slew Rates
- Adjustable Driver Slew Rates
- Three Statable
- Low HiZ Leakage
- Low Voltage Driver Swings
- Low Overshoot Waveforms
- 12 V Output Range
- 9 V Output Swings
- 28-Pin PLCC with an Internal Heat Spreader
- Edge693 Compatible
- Bt692 Compatible

Applications

- Memory Test Equipment
- Instrumentation

Functional Block Diagram

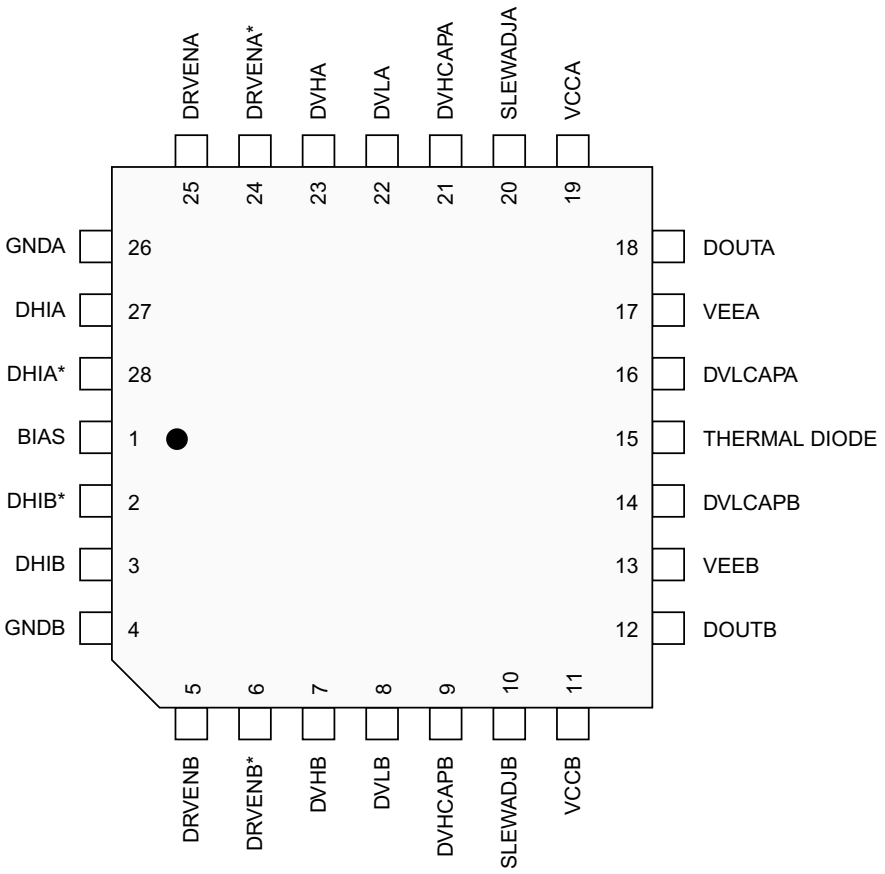


PIN Description

Pin Name	Pin #	Description
Driver		
DRVENA, DRVENA* DRVENB, DRVENB*	25, 24 5, 6	Wide voltage differential input pins that determine whether the driver (A and B respectively) is forcing a voltage or placed in a high impedance state.
DHIA, DHIA* DHIB, DHIB*	27, 28 3, 2	Wide voltage differential input pins that force one of two programmable levels (DVH or DVL) at the driver (A and B respectively) output.
DOUTA DOUTB	18 12	Driver A and driver B outputs.
DVLA, DVHA DVLB, DVHB	22, 23 8, 7	Buffereed analog inputs that program the low and high output levels for driver A and driver B.
DVLCAPA, DVHCAPA DVLCAPB, DVHCAPB	16, 21 14, 9	Analog pins. 0.01 µF capacitor to ground should be connected to each pin.
SLEWADJA SLEWADJB	20 10	Analog current inputs that adjust the rise and fall slew rates of driver A and driver B.
BIAS	1	Analog input. A positive current into this node sets the internal bias level for driver A and driver B.
Power		
VEEA, VEEB	17, 13	Negative power supply for driver A and driver B.
VCCA, VCCB	19, 11	Positive power supply for driver A and driver B.
GNDA, GNDB	26, 4	Device ground for driver A and driver B.
Test Pins		
THERMAL DIODE	15	Thermal monitor output used to track the die junction temperature.

PIN Description *(continued)*

28-Pin PLCC



Circuit Description

Introduction

The driver circuit will force the DOUT output to one of three states:

1. DVH (driver high voltage level)
2. DVL (driver low voltage level)
3. High Impedance (Hi Z).

Both driver digital control inputs (DHI/DHI*, DRVEN/DRVEN*) are wide-voltage differential inputs capable of receiving ECL, TTL, and CMOS signals. Single-ended operation is achievable by generating the proper threshold levels for the inverting inputs.

Drive Enable

The drive enable (DRVEN/DRVEN*) inputs control whether the driver is forcing a voltage or is placed in a high-impedance state. If DRVEN is more positive than DRVEN*, the output will force either DVL or DVH, depending on the driver data inputs. When DRVEN is more negative than DRVEN*, the output is set to high-impedance, independent of the driver data inputs.

Driver Data

The driver data inputs (DHI/DHI*) determine whether the driver output is high or low. If DHI is more positive than DHI*, the output will force DVH when the driver is enabled. If DHI is more negative than DHI*, the output will force DVL when the driver is enabled.

Table 1 summarizes the functionality of the driver enable and driver data pins.

DRVEN, DRVEN*	DHI, DHI*	DOUT
DRVEN > DRVEN*	DHI > DHI*	DVH
DRVEN > DRVEN*	DHI < DHI*	DVL
DRVEN < DRVEN*	X	HiZ

Table 1. DRVEN and DHI Pin Functionality

Driver Levels

DVH and DVL are high input impedance voltage controlled inputs that establish the driver logical high and low levels respectively.

DVLCAP / DVHCAP

These two analog nodes are brought out to better stabilize the high and low driver levels. Much like placing decoupling capacitors on the DVL and DVH input pins, the DVLCAP and DVHCAP pins require a fixed .01 µF chip capacitor (with good high frequency characteristics) to ground. A tight layout with minimum etch is recommended.

Driver Bias

The BIAS pin is an analog current input that establishes a reference current for the driver and influences the overall speed and power consumption of the chip. The BIAS input current may be varied from 1.0 mA to 2.0 mA. Ideally, a current source would supply this current. However, a resistor to a voltage source, typically VCC, is acceptable.

The BIAS input structure is shown in Figure 1.

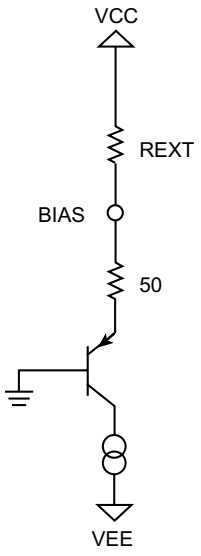


Figure 1. BIAS Input Structure

Circuit Description *(continued)*

The desired value for the external resistor can be determined from the relationship:

IBIAS = (VCC - .7) / (Rext + 50).

The actual IBIAS level is determined by selecting the desired performance and power level. The charts listed in the Application Information section enable the user to quickly determine the appropriate bias level.

Thermal Monitor

The Edge692 includes an on-chip thermal monitor accessible through the THERMAL DIODE pin. This node connects to 5 diodes in series to VEE (see Figure 2) and may be used to accurately measure the junction temperature at any time.

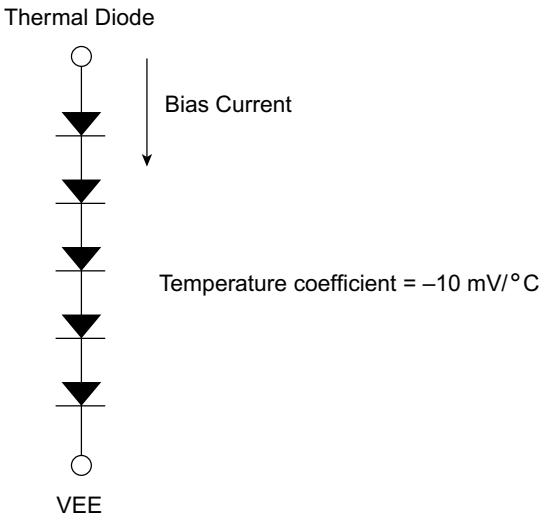


Figure 2. Thermal Diode String

A bias current of 100 µA is injected into this node, and the measured voltage corresponds to a specific junction temperature with the following equation:

TJ(°C) = {[(VTHERMAL DIODE – VEE) / 5] – .7} / (–.00208).

Slew Rate Adjustment

The driver rising and falling slew rates are adjustable from 2 V/ns to 1 V/ns. The actual slew rate realized is a function of the chip bias and slew rate adjust input currents.

The SLEWADJ input is determined by selecting the desired performance and power level (after the BIAS current is first chosen.) The charts listed in the Application Information section enable the user to quickly determine the appropriate SLEWADJ level.

SLEWADJ is a current controlled input that varies the rising and falling edge slew rates. Ideally, a current DAC would be used to establish this current. However, a resistor to a positive voltage, typically VCC, is acceptable.

Figure 3 shows a simplified schematic of the SLEWADJ input stage. Once a desired input current is selected, the external resistor value is determined by the following relationship:

(VCC - .7) / (Rext + 860) = Islewadj.

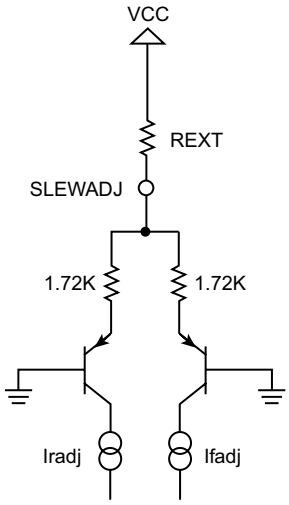
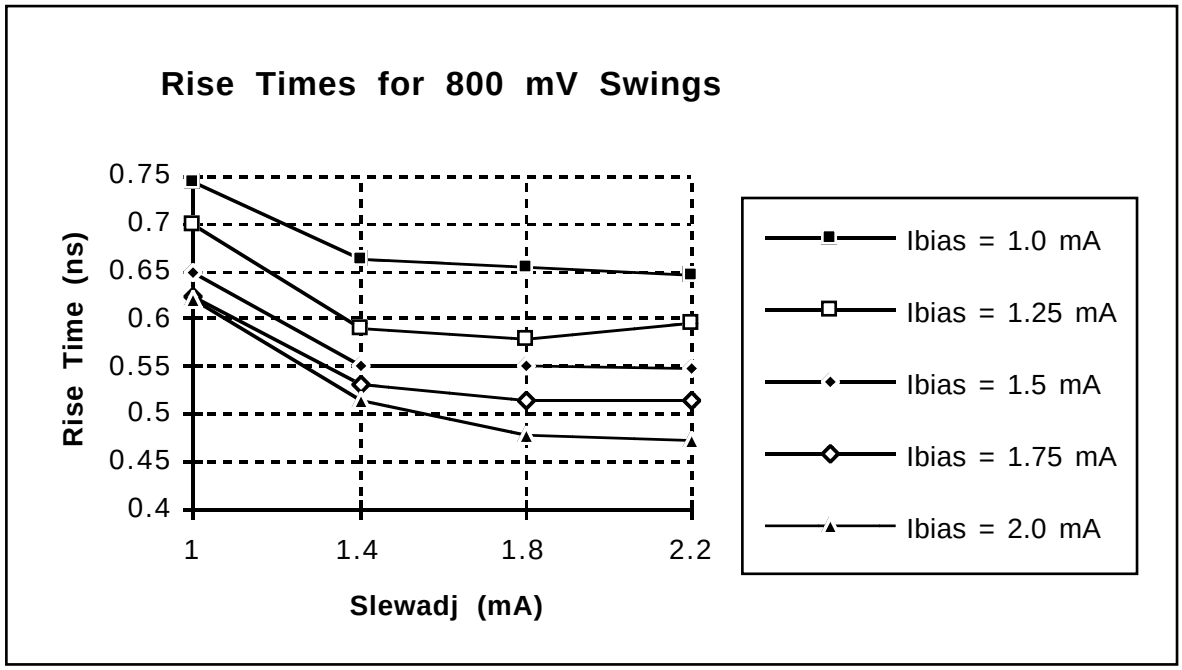
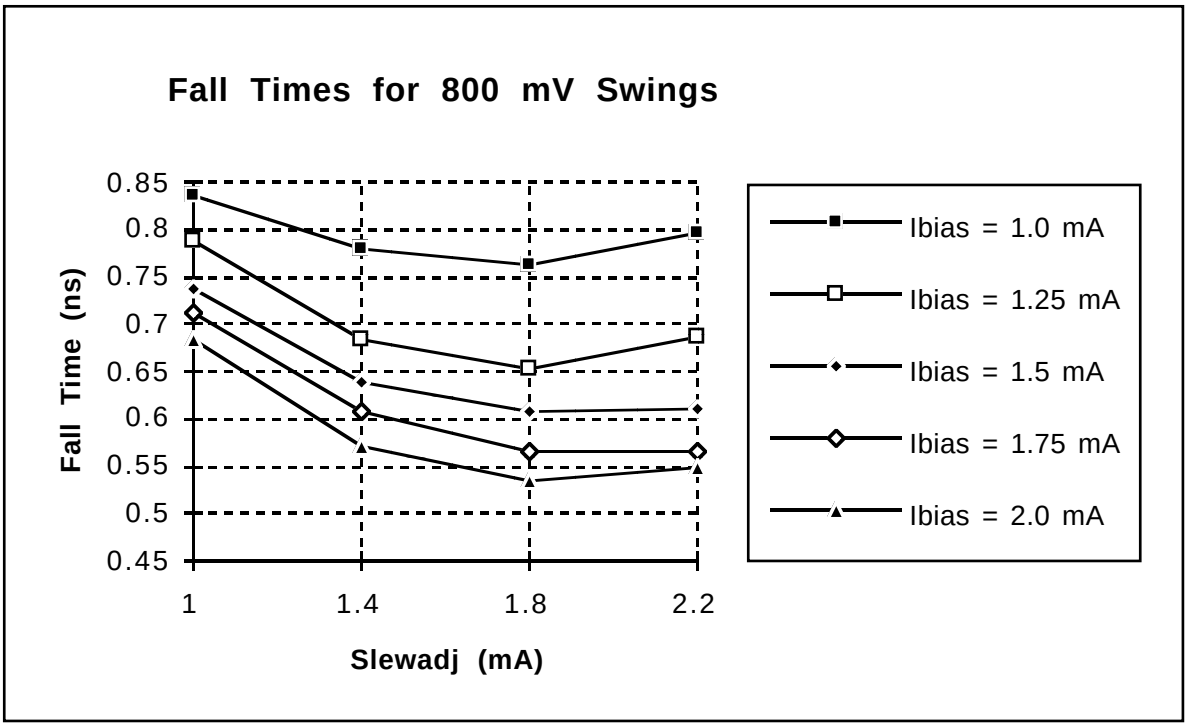


Figure 3. SLEWADJ input circuitry

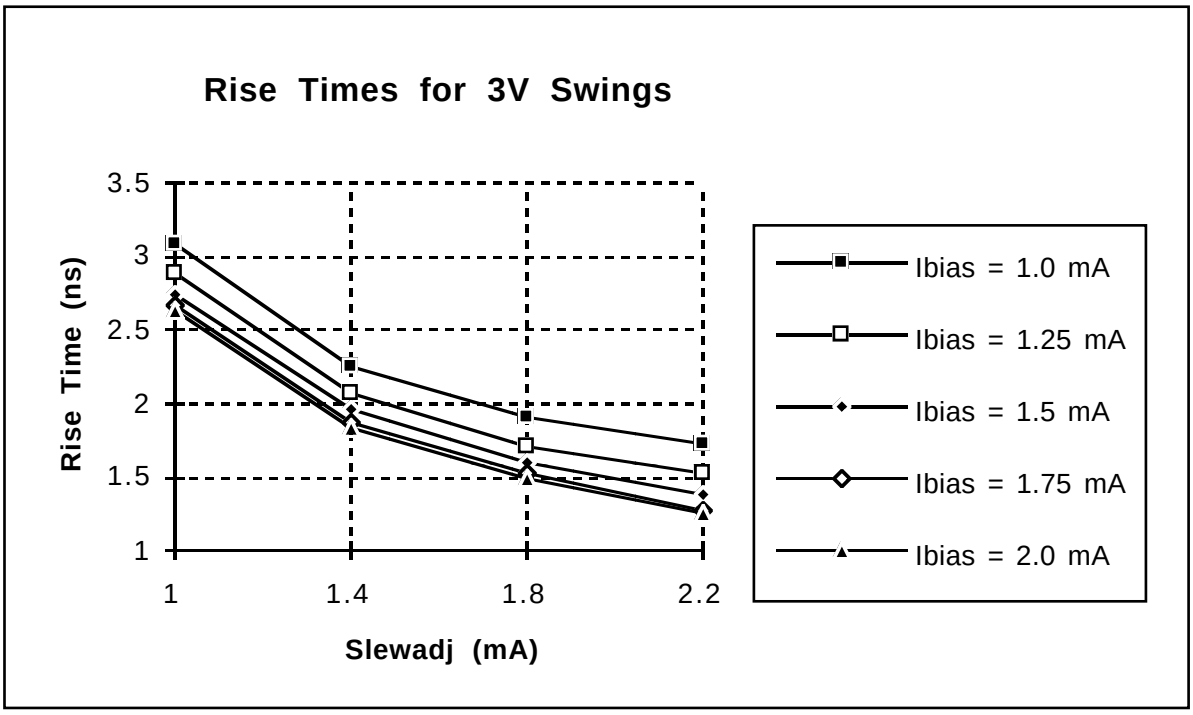
Notice that the driver A slew rate and driver B slew rate are independent. However, the rising and falling edge slew rates on each driver track each other and are not independent.

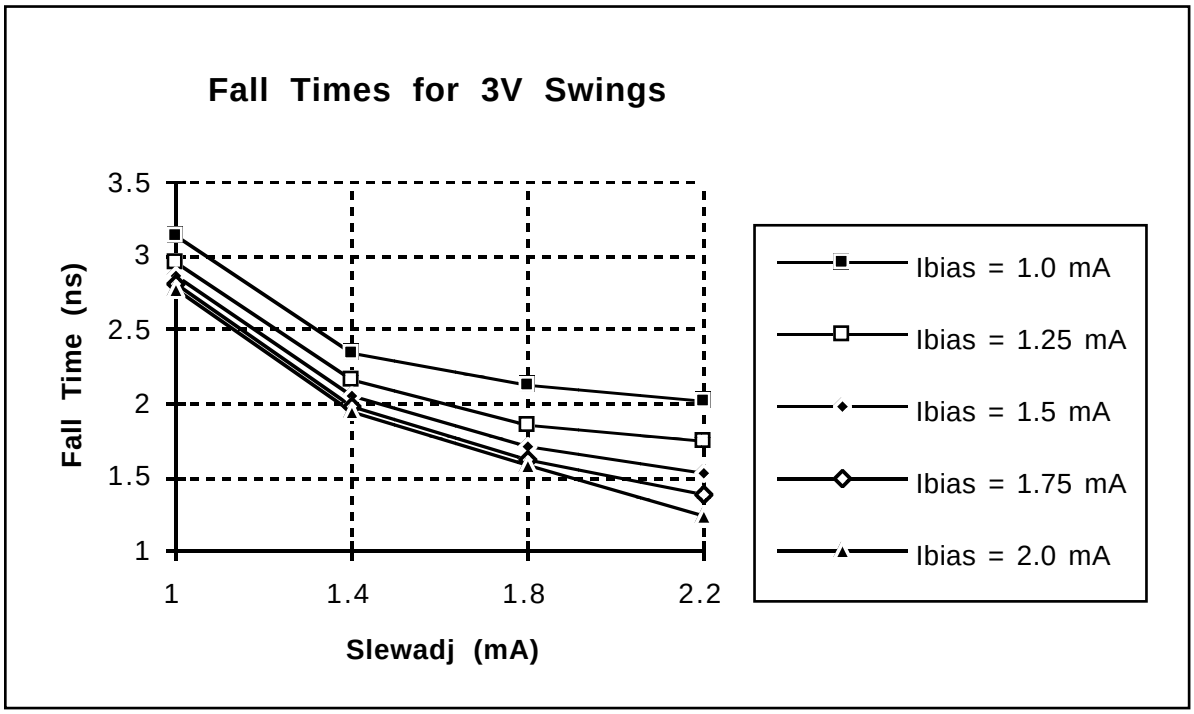
Family of Curves for Rise and Fall Times for 800 mV Swings.



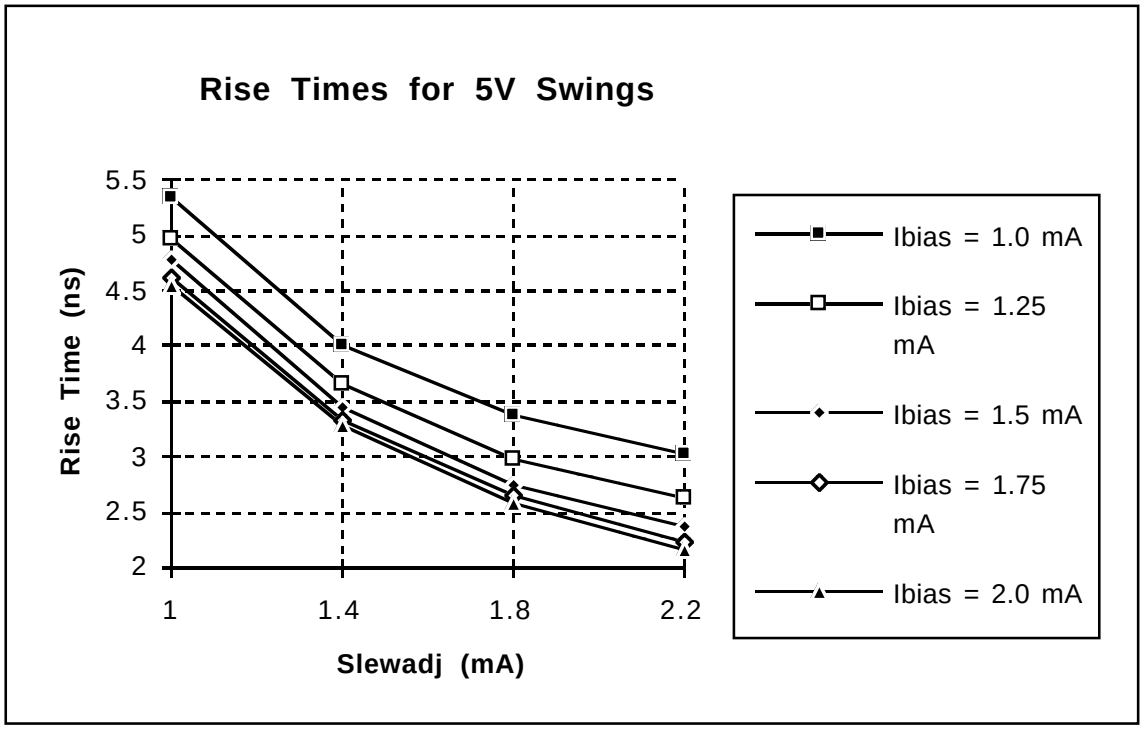


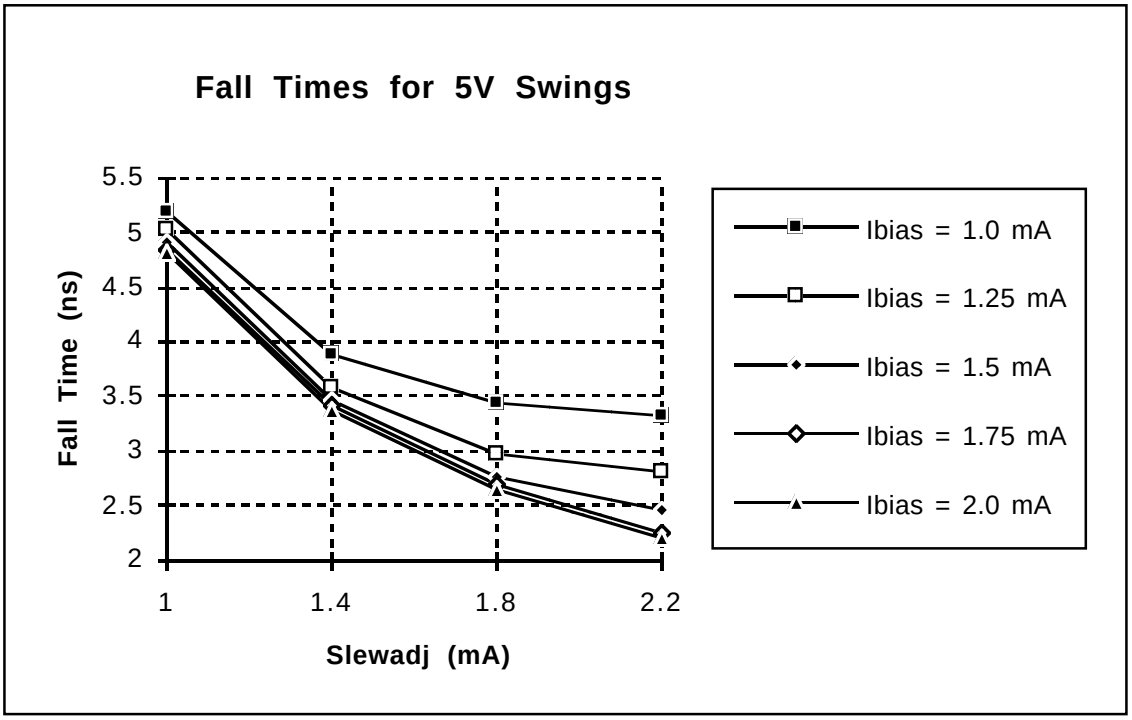
Family of Curves for Rise and Fall Times for 3V Swings.



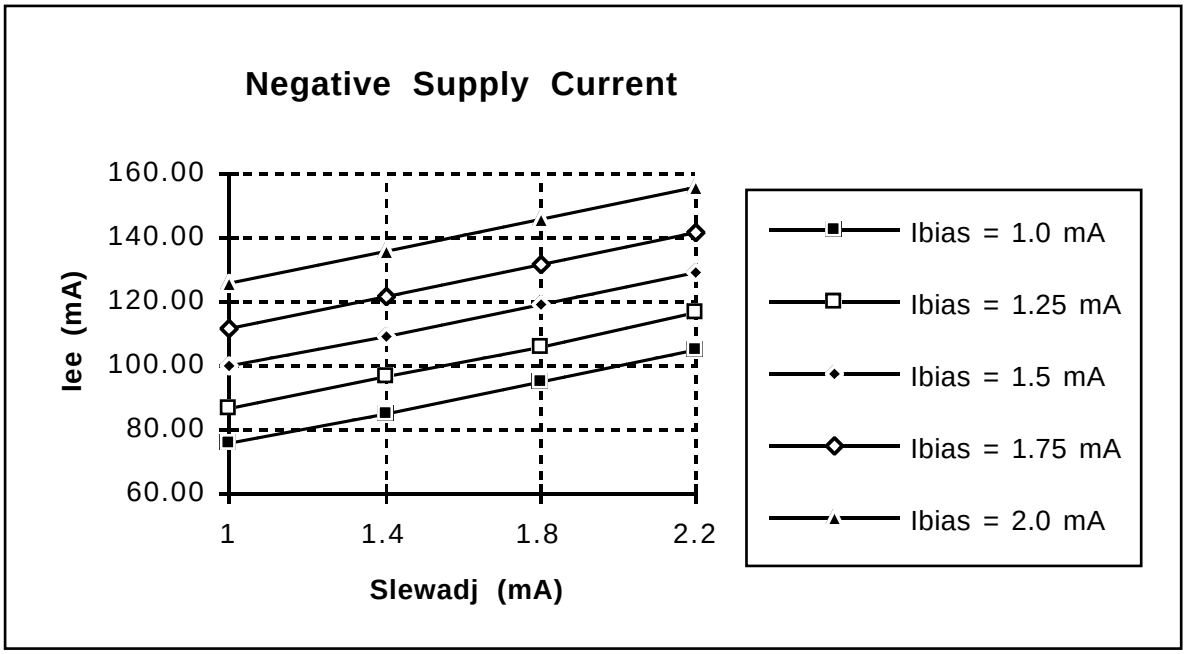


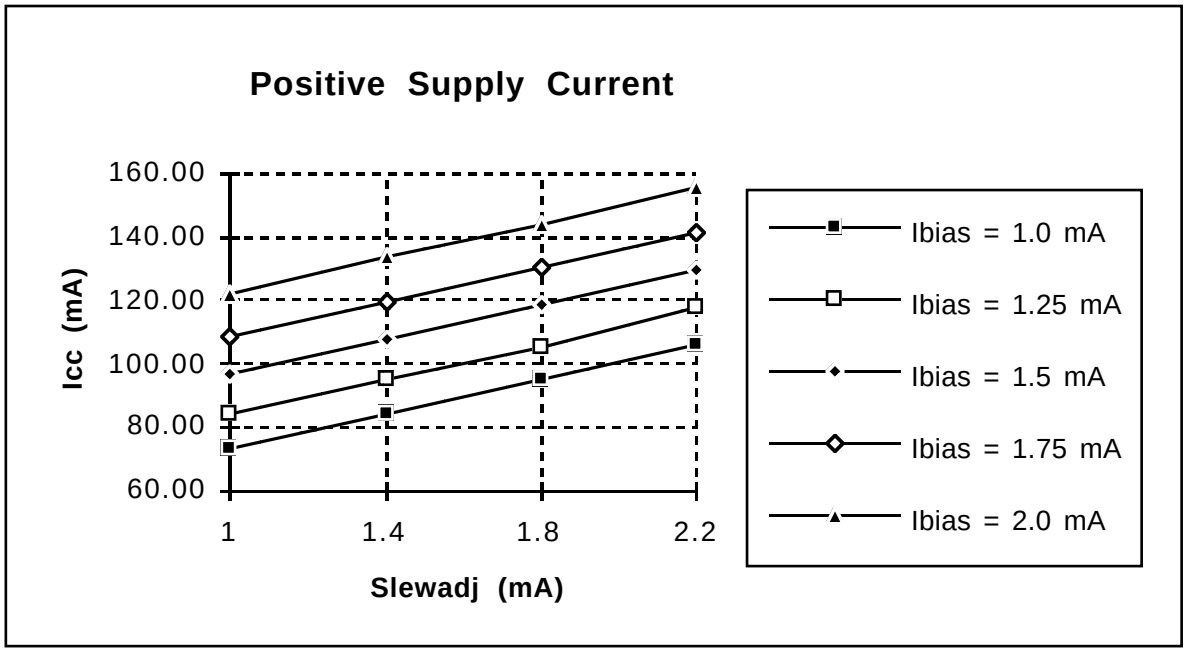
Family of Curves for Rise and Fall Times for 5V Swings.





Supply Current Family of Curves

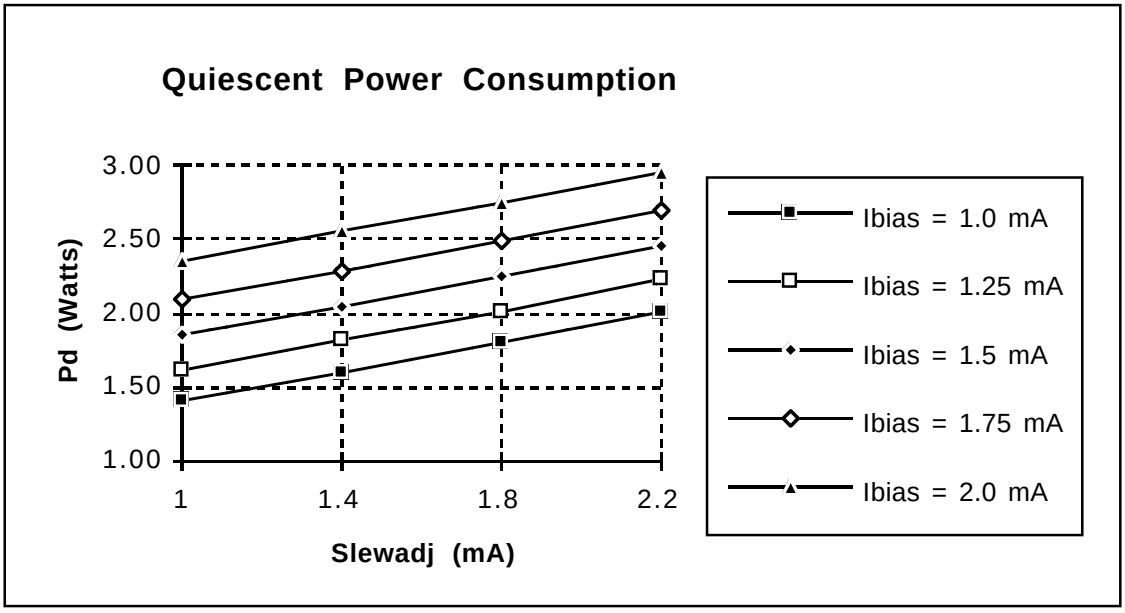


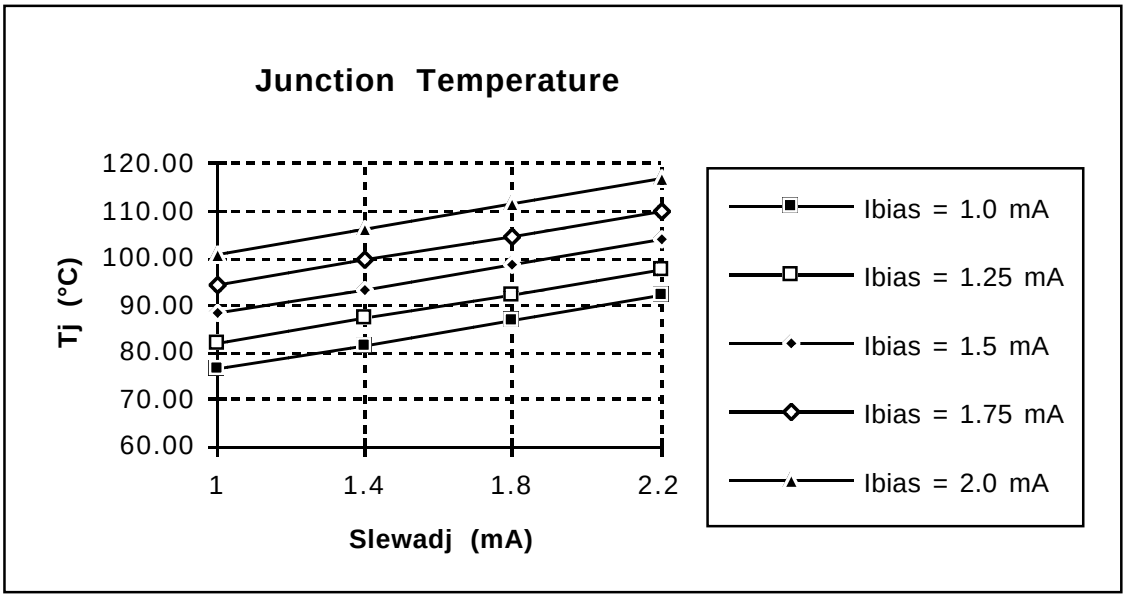


Application Information (continued)

Power Dissipation Family of Curves

Conditions:
VCC = +11.5V
VEE = –7.5V
Ta = 40˚C
θJA = 26˚C





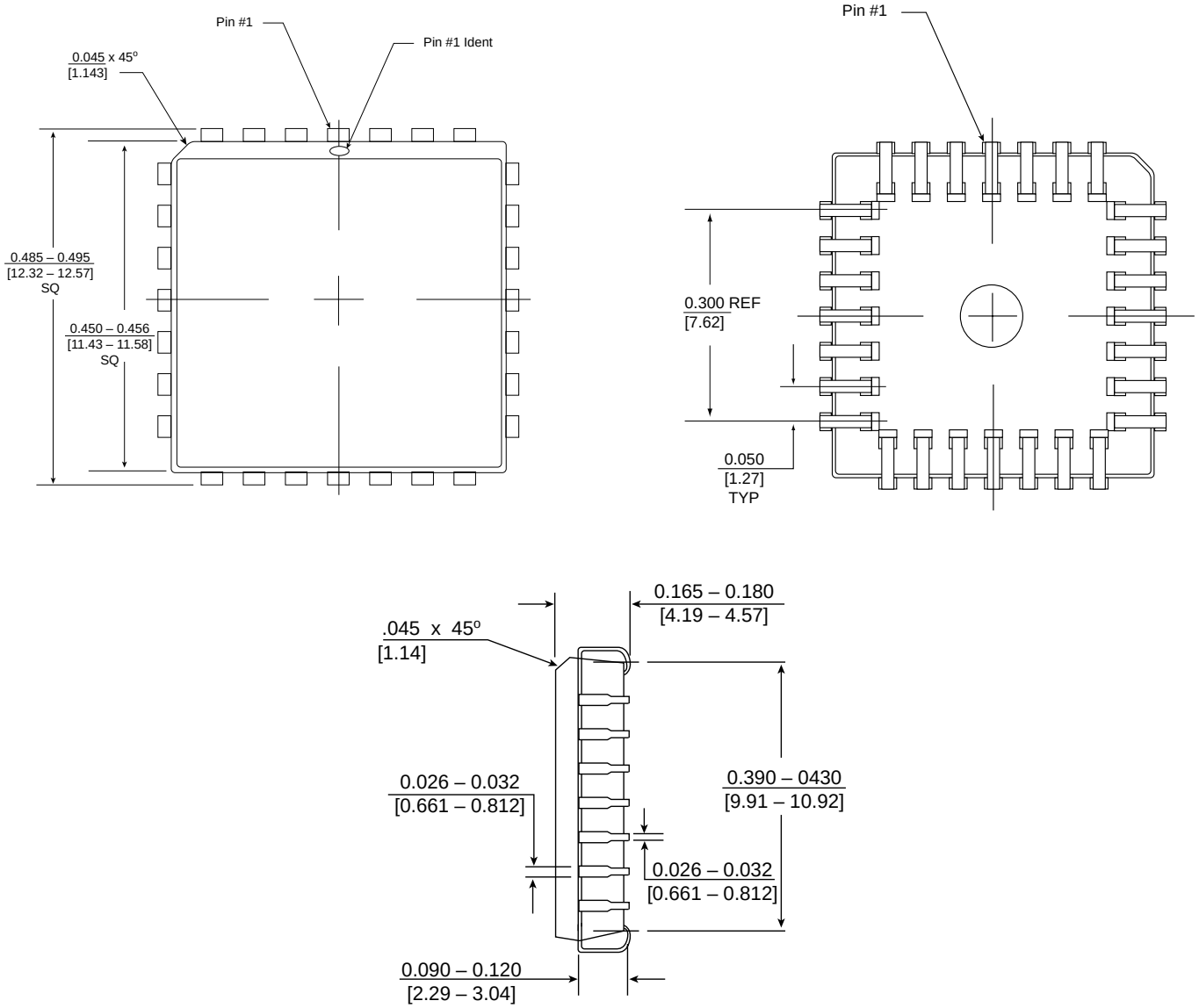
Application Information (continued)

Thermal Information

Parameter	Symbol	Min	Typ	Max	Units
Thermal Resistance					
Junction to Case	θ_{JC}		13		$^oC/W$
Junction to Air					
Still Air	θ_{JA}		49		$^oC/W$
50 LFPM	θ_{JA}		36		$^oC/W$
400 LFPM	θ_{JA}		26		$^oC/W$

Package Information

28 Pin PLCC Package
θJA = 75 to 80˚C / W



Notes: (unless otherwise specified)
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127].
3. PLCC packages are intended for surface mounting on solder lands on 0.050 [1.27] centers.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Positive Power Supply	VCC	8.5	11.5	13.5	V
Negative Power Supply	VEE	-8.5	-7.5	-4.2	V
Total Analog Supply	VCC - VEE	12.7		19.0	V
Analog Inputs					
Driver High Level	DVH	VEE + 3.5		VCC - 2.9	V
Driver Low Level	DVL	VEE + 2.9		VCC - 3.5	V
Driver Bias	BIAS	1.0	1.5	2.0	mA
Driver A Slew Rate Adjust	SLEWADJA	1.0	1.75	2.2	mA
Driver B Slew Rate Adjust	SLEWADJB	1.0	1.75	2.2	mA
Ambient Operating Temperature	TA	+25		+70	^{o}C
Junction Temperature	TJ	+25		+125	^{o}C

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VCC (Relative to GND)	VCC	0		+14.0	V
VEE (Relative to GND	VEE	-10.0		0	V
Total Power Supply	VCC - VEE			+20.0	V
Digital Input Voltages	DRVEN, DRVEN* DHI, DHI*	VEE		+6.0	V
Differential Input Voltages	DRVEN - DRVEN* DHI - DHI*	-5.0		+5.0	V
Analog Voltages	DOUT, DVL, DVH	VEE		VCC	V
Analog Input Currents					
Driver Bias	BIAS	0		2.6	mA
Slew Rate Adjust	SLEWADJA	0		2.8	mA
	SLEWADJB	0		2.8	mA
Ambient Operating Temperature	TA	-55		+125	^{o}C
Storage Temperature	TS	-65		+150	^{o}C
Junction Temperature	TJ			+150	^{o}C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	^{o}C

Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device mounted either in the test socket or on the printed circuit board. Thermal resistance measurements are taken with device soldered to PCB.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Driver Circuit					
Analog Input Current					
DVH, DVL	IIN	-200		+200	µA
Bias Input	BIAS	1.0	1.5	2.0	mA
Adjustment Inputs					
SLEWADJ Current Range		1.0	1.75	2.2	mA
Driver Circuit					
Output Voltage Range	VDOUT	VEE + 3.5		VCC - 3.5	V
Output Voltage Swing	Vswing	0		9.0	V
Max Static Output Current:					
DOUT > -2V	IDOUT	-35		+35	mA
DOUT < -2V	IDOUT	-20		+20	mA
Max Dynamic Output Current		-100		+100	mA
DOUT Leakage Current (Note 1)	ILEAK	-1	<.025	1	µA
DC Accuracy					
Driver High					
Offset (Note 2)	DVH - DOUT	-150		350	mV
Gain (Note 3)	ΔDVH / ΔDOUT	.95	.99	1.0	V/V
Linearity (Note 4)	DVL - DOUT	-20	<10	20	mV
Driver Low					
Offset (Note 2)	DVH - DOUT	-150		350	mV
Gain (Note 3)	ΔDVH / ΔDOUT	.95	.99	1.0	V/V
Linearity (Note 4)	DVL - DOUT	-20	<10	20	mV
Offset Voltage Temperature Coefficient	DOUT TC		±1		mV/°C
Driver Output Impedance	ZOUT	1.0	3.0	4.5	Ω
Driver PSRR	PSRR	30			dB
Digital Inputs					
DRVEN, DRVEN*, DHI, DHI*					
Input Current	IIN	-900		+900	µA
Input Voltage Range	VRNG	-2.0		+5.5	V
Differential Input Swing	VDIFF	0.25		+4.0	V
Power Supply Current					
Positive Supply	ICC		120	150	mA
Negative Supply	IEE	-150	120		mA

Note 1: Device output leakage is specified with DOUT over the entire output voltage range.

Note 2: The offset voltage is defined as the difference between the measured driver output at DOUT under no load conditions versus the programmed voltage (DVH or DVL) when forced to –1.0 V.

Note 3: The driver gain is defined as the change in driver output voltage (DOUT) divided by the change in programmed input voltage (DVH or DVL). Measurements are taken at –1.0 V and +4.0 V programmed inputs with the output under no-load conditions.

Note 4: Linearity error is defined as the maximum deviation between the theoretical driver output voltage (predicted by the straight line determined by the offset and gain) and the actual measured output voltage under no load conditions.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Driver Circuit					
Tpd from DHI to DOUT (Note 1)	Tpd		1.7		ns
Tpd from DRVEN to DOUT HiZ (Note 2)			1.7		ns
Tpd from DRVEN to DOUT Active (Note 2)			1.7		ns
DOUT Rise/Fall Times (Note 3)					
800 mV, 20% - 80%	Tr/Tf	.5	0.6	.75	ns
3V, 10% - 90%	Tr/Tf	1.25	1.6	3.0	ns
5V, 10% - 90%	Tr/Tf	2.25	2.75	5.0	ns
Toggle Rate	Fmax				
800 mV		200			MHz
3V		150			MHz
5V		100			MHz
Output Capacitance in HiZ	Cout		2.0		pF
Minimum Pulse Width (Note 4)					
800 mV		2.5			ns
3V		3.0			ns
5V		5.0			ns

The specified limits shown can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least two minutes while maintaining the normal operating environment.

Note 1: Tpd is measured from crossover point of DHI and DHI* to the 50% point in the output. DVL equals 0 V and DVH equals +3 V.

Note 2: Specification condition: DVL equals -1 V and DVH equals +1 V. Output is terminated to GND by 100 Ω. Tpd is measured from the crossover point of DRVEN and DRVEN* to the point where a 10-percent change in output voltage occurs.

Note 3: The driver load is an 18" 50Ω. transmission line terminated with 1KΩ. in parallel with 2 pF.

Note 4: The output pulse width is measured at the 50-percent points. Output reaches 100% of programmed value.

Ordering Information

Model Number	Package	Ambient Temperature Range
E692AHJ	28-Pin PLCC (with Internal Heat Spreader)	+25°C to +70°C
EVM692AHJ	Edge692 Evaluation Module	

Contact Information

Semtech Corporation
Edge High-Performance Division
10021 Willow Creek Rd., San Diego, CA 92131
Phone: (858)695-1808 FAX (858)695-2633