Edge693
500 MHz Monolithic Dual Pin Electronics Driver

EDGE HIGH-PERFORMANCE PRODUCTS

Description

The Edge693 is a dual pin electronics driver solution manufactured in a high-performance, complementary bipolar process. In Automatic Test Equipment (ATE) applications, the Edge693 offers two pin drivers suitable for drive-only channels in memory testers, as well as for bidirectional channels in memory, VLSI, and mixed- signal test systems.

Each driver is completely isolated from the other. There are separate data, enable, slew rate adjust, high and low levels; as well as power supply inputs for each driver. The driver output slew rate is adjustable from 3 V/ns to 1 V/ns, allowing the matching of edges from channel-to-channel, as well as slowing down edges for noise sensitive applications.

Each driver is capable of driving 9 V signals over a 12 V range, in addition to going into a high impedance state. The Edge693 can generate ECL signals up to 500 MHz and 3V signals in excess of 300 MHz.

Combining two independent drivers into a 28-pin PLCC package offers a highly integrated solution appropriate where speed and density are at a premium.

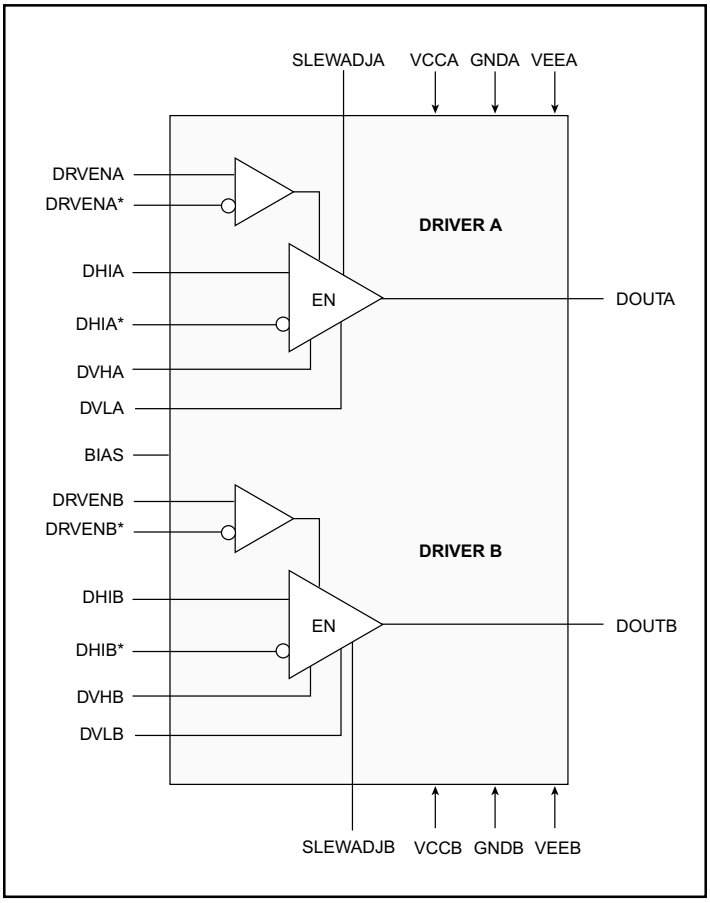
Features

- >2.5 V/ns Driver Slew Rates
- Adjustable Driver Slew Rates
- HiZ Capability
- 12 V Output Range
- 9 V Output Swings
- 28-Pin PLCC with an Internal Heat Spreader

Applications

- Memory Test Equipment
- Instrumentation

Functional Block Diagram

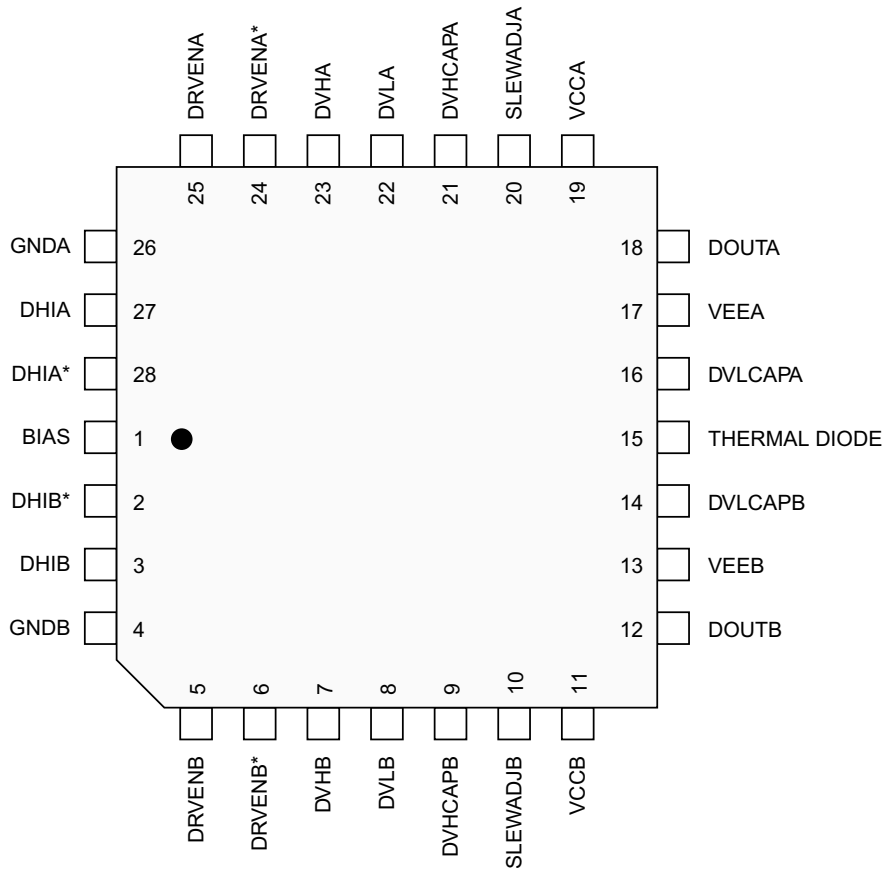


PIN Description

Pin Name	Pin #	Description
Driver		
DRVENA, DRVENA* DRVENB, DRVENB*	25, 24 5, 6	Wide voltage differential input pins that determine whether the driver (A and B respectively) is forcing a voltage or placed in a high impedance state.
DHIA, DHIA* DHIB, DHIB*	27, 28 3, 2	Wide voltage differential input pins that force one of two programmable levels (DVH or DVL) at the driver (A and B respectively) output.
DOUTA DOUTB	18 12	Driver A and driver B outputs.
DVLA, DVHA DVLB, DVHB	22, 23 8, 7	Buffereed analog inputs that program the low and high output levels for driver A and driver B.
DVLCAPA, DVHCAPA DVLCAPB, DVHCAPB	16, 21 14, 9	Analog pins. 0.01 µF capacitor to ground should be connected to each pin.
SLEWADJA SLEWADJB	20 10	Analog current inputs that adjust the rise and fall slew rates of driver A and driver B.
BIAS	1	Analog input. A positive current into this node sets the internal bias level for driver A and driver B.
Power		
VEEA, VEEB	17, 13	Negative power supply for driver A and driver B.
VCCA, VCCB	19, 11	Positive power supply for driver A and driver B.
GNDA, GNDB	26, 4	Device ground for driver A and driver B.
Test Pins		
THERMAL DIODE	15	Thermal monitor output used to track the die junction temperature.

PIN Description *(continued)*

28-Pin PLCC



Circuit Description

Introduction

The driver circuit will force the DOUT output to one of three states:

1. DVH (driver high voltage level)
2. DVL (driver low voltage level)
3. High Impedance (Hi Z).

Both driver digital control inputs (DHI/DHI*, DRVEN/DRVEN*) are wide-voltage differential inputs capable of receiving ECL, TTL, and CMOS signals. Single-ended operation is achievable by generating the proper threshold levels for the inverting inputs.

Drive Enable

The drive enable (DRVEN/DRVEN*) inputs control whether the driver is forcing a voltage or is placed in a high-impedance state. If DRVEN is more positive than DRVEN*, the output will force either DVL or DVH, depending on the driver data inputs. When DRVEN is more negative than DRVEN*, the output is set to high-impedance, independent of the driver data inputs.

Driver Data

The driver data inputs (DHI/DHI*) determine whether the driver output is high or low. If DHI is more positive than DHI*, the output will force DVH when the driver is enabled. If DHI is more negative than DHI*, the output will force DVL when the driver is enabled.

Table 1 summarizes the functionality of the driver enable and driver data pins.

DRVEN, DRVEN*	DHI, DHI*	DOUT
DRVEN > DRVEN*	DHI > DHI*	DVH
DRVEN > DRVEN*	DHI < DHI*	DVL
DRVEN < DRVEN*	X	HiZ

Table 1. DRVEN and DHI Pin Functionality

Driver Levels

DVH and DVL are high-input impedance voltage controlled inputs that establish the driver logical high and low levels respectively.

Slew Rate Adjustment

The driver rising and falling slew rates are adjustable from 3.0 V/ns to 1 V/ns. The SLEWADJ signals are current controlled inputs that vary the rising and falling edge slew rates. An input current of 2.0 mA translates to a slew rate of 3.0 V/ns. An input current of 0.8 mA forces a 1 V/ns edge (see Figure 1).

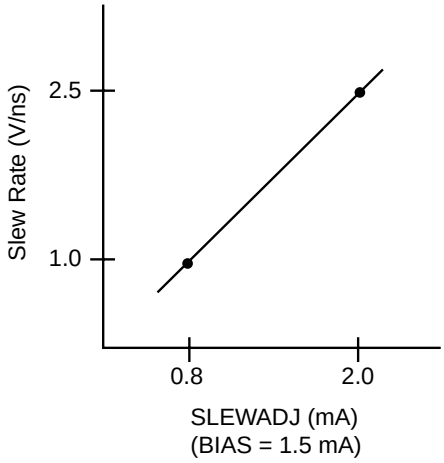
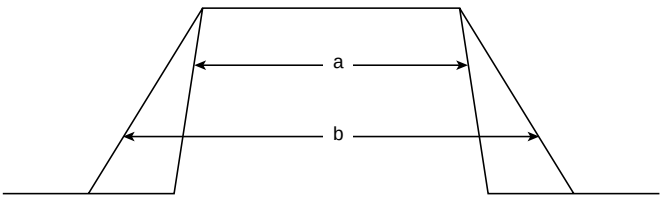


Figure 1. Slew Rate Control

Notice that the driver A slew rate and driver B slew rate are independent. However, the rising and falling edge slew rates on each driver track each other and are not independent (see Figure 2).



a. SLEWADJ = 2.0 mA, Rising SR = Falling SR = 2.5V/ns.
b. SLEWADJ = 0.8 mA, Rising SR = Falling SR = 1.0V/ns.

Figure 2. Output Slew Rate Adjustability

Circuit Description *(continued)*

For system level flexibility, the SLEWADJ input is designed to allow a voltage DAC, a current DAC, or a resistor to a fixed voltage as possible slew rate control mechanisms (see Figure 3).

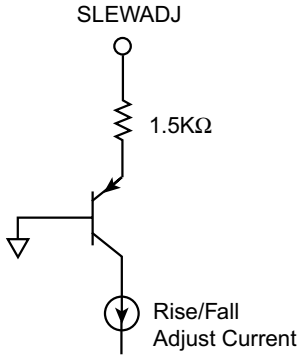


Figure 3. SLEWADJ Inputs

Driver Bias

The BIAS pin is an analog current input that requires a 1.2 mA fixed reference current for the driver. Several circuit configurations are usable to satisfy this requirement, the most simple being a fixed resistor to a fixed power supply, typically VCC (see Figure 4). Looking into the BIAS node shows a .7 V voltage source with a 1.5 KW impedance, so the equation to select the fixed resistor is:

$$(VCC - .7) / (R + 1.5) = 1.2\ mA$$

Alternatively, a current DAC could be used to either program the BIAS current or to perform subtle adjustments in the fixed value.

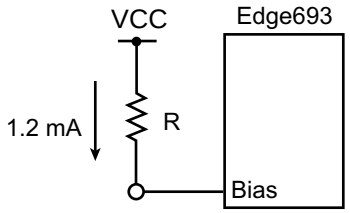


Figure 4. Bias Current Generation

DVLCAP / DVHCAP

These two analog nodes are brought out to better stabilize the high and low driver levels. Much like placing decoupling capacitors on the DVL and DVH input pins, the DVLCAP and DVHCAP pins require a fixed .01 µF chip capacitor (with good high frequency characteristics) to ground (see Figure 5). A tight layout with minimum etch is recommended.

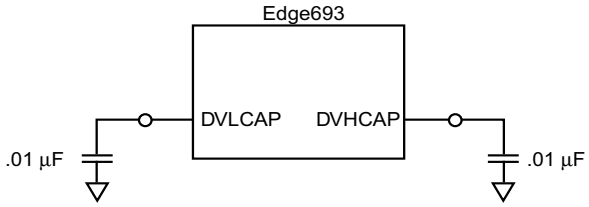


Figure 5. DVLCAP and DVHCAP

Thermal Monitor

The Edge693 includes an on-chip thermal monitor accessible through the THERMAL DIODE pin. This node connects to 5 diodes in series to VEE (see Figure 6) and may be used to accurately measure the junction temperature at any time.

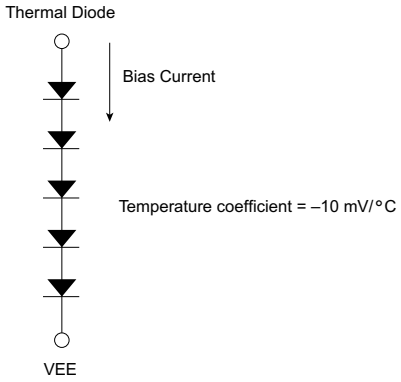


Figure 6. Thermal Diode String

A bias current of 100 µA is injected into this node, and the measured voltage corresponds to a specific junction temperature with the following equation:

$$T_{J(°C)} = \{(V_{THERMAL\ DIODE} - VEE) / 5 - .7\} / (-.00208).$$

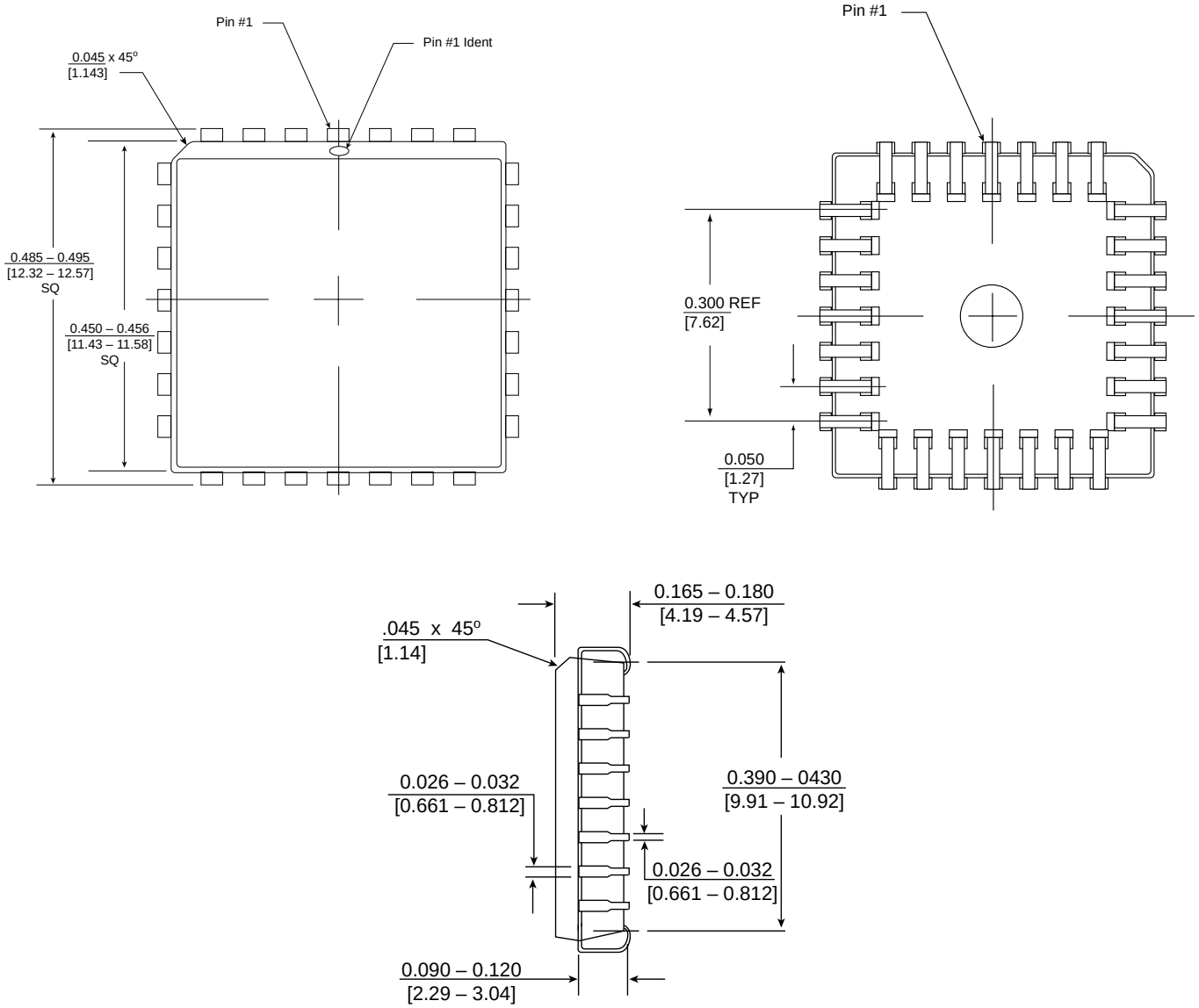
Thermal Information

Parameter	Symbol	Min	Typ	Max	Units
Thermal Resistance					
Junction to Case	θJC		13		°C/W
Junction to Air					
Still Air	θJA		49		°C/W
50 LFPM	θJA		36		°C/W
400 LFPM	θJA		26		°C/W

Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device mounted either in the test socket or on the printed circuit board. Thermal resistance measurements are taken with device soldered to PCB.

Package Information

28 Pin PLCC Package
θJA = 75 to 80˚C / W



Notes: (unless otherwise specified)
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127].
3. PLCC packages are intended for surface mounting on solder lands on 0.050 [1.27] centers.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Positive Power Supply	VCC	10.5		12.5	V
Negative Power Supply	VEE	-8.0		-4.2	V
Total Analog Supply	VCC - VEE	14.7		19.0	V
Analog Inputs					
Driver High Level	DVH	VEE + 3.5		VCC - 2.9	V
Driver Low Level	DVL	VEE + 2.9		VCC - 3.5	V
Driver Bias	BIAS		1.5		mA
Driver A Slew Rate Adjust	SLEWADJA	0.8		2.5	mA
Driver B Slew Rate Adjust	SLEWADJB	0.8		2.5	mA
Ambient Operating Temperature	TA	0		+70	^{o}C
Junction Temperature	TJ	+25		+125	^{o}C

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VCC (Relative to GND)	VCC	0		+14.0	V
VEE (Relative to GND	VEE	-10.0		0	V
Total Power Supply	VCC - VEE			+19.0	V
Digital Input Voltages	DRVEN, DRVEN* DHI, DHI*	VEE		+7.0	V
Differential Digital Input Voltages	DRVEN - DRVEN* DHI - DHI*	-5.5		+5.5	V
Analog Voltages	DOUT, DVL, DVH	VEE		VCC	V
Analog Input Currents					
Driver Bias	BIAS	0		2.5	mA
Slew Rate Adjust	SLEWADJA	0		3.0	mA
	SLEWADJB	0		3.0	mA
Driver Output Current (Static)	DOUT	-50		+50	mA
Ambient Operating Temperature	TA	-55		+125	^{o}C
Storage Temperature	TS	-65		+150	^{o}C
Junction Temperature	TJ			+150	^{o}C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	^{o}C

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Analog Input Current					
DVH, DVL	IIN	-50		+50	µA
Bias Input	BIAS		1.5		mA
Adjustment Inputs					
SLEWADJ Input Resistance			1.5		KΩ
SLEWADJ Current Range		0.9		2.0	mA
Driver Circuit					
Output Voltage Range	VDOUT	VEE + 3.5		VCC - 3.5	V
Output Voltage Swing	Vswing	0.25		9.0	V
Max Static Output Current:					
DOUT >= -2V	IDOUT	-35		+35	mA
DOUT < -2V	IDOUT	-20		+35	mA
Max Dynamic Output Current		-100		+100	mA
DOUT Leakage Current (Note 1)					
DOUT >= -2V	ILEAK	-1		1	µA
DOUT < -2V	ILEAK	-3		3	µA
Driver High Accuracy					
Offset (Note 1)	DVH - DOUT	-90	-65	-40	mV
Gain (Note 2)	ΔDVH / ΔDOUT	-95	.99	1.0	V/V
Linearity (Note 3)	DVL - DOUT	-15	1	+15	mV
Driver Low Accuracy					
Offset (Note 1)	DVH - DOUT	-75	-50	-25	mV
Gain (Note 2)	ΔDVH / ΔDOUT	-95	.99	1.0	V/V
Linearity (Note 3)	DVL - DOUT	-15	1	+15	mV
Offset Voltage Temperature Coefficient	DOUT TC		±1		mV/°C
Driver Output Impedance	ZOUT	1.0	3.0	4.5	Ω
Driver PSRR	PSRR	20			dB
Digital Inputs					
DRVEN, DRVEN*, DHI, DHI*					
Input Current	IIN	-900		+900	µA
Input Voltage Range	VRNG	-2.0		+5.5	V
Differential Input Swing	VDIFF	0.25		+4.0	V
Power Supply Current				160	
Positive Supply	ICC		140		mA
Negative Supply	IEE	-160	-140		mA

Note 1: The offset voltage is defined as the difference between the measured driver output at DOUT under no load conditions versus the programmed voltage (DVH or DVL) when forced to –1.0 V.

Note 2: The driver gain is defined as the change in driver output voltage (DOUT) divided by the change in programmed input voltage (DVH or DVL). Measurements are taken at –1.0 V and +4.0 V programmed inputs with the output under no-load conditions.

Note 3: Linearity error is defined as the maximum deviation between the theoretical driver output voltage (predicted by the straight line determined by the offset and gain) and the actual measured output voltage under no load conditions.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Driver Circuit					
Tpd from DHI to DOUT (Note 1)	Tpd		1.5		ns
Tpd from DRVEN to DOUT HiZ (Note 2)			1.5		ns
Tpd from DRVEN to DOUT Active (Note 2)			1.5		ns
DOUT Rise/Fall Times (Note 3)					
ECL, 20% - 80%	Tr/Tf		0.6		ns
3V, 10% - 90%	Tr/Tf		1.2		ns
5V, 10% - 90%	Tr/Tf		1.8		ns
8V, 10% - 90%	Tr/Tf		2.75		ns
Slew Rate Sensitivity to RADJ or FADJ	SR/IADJ		.938		V/ns/mA
Toggle Rate (Note 4)	Fmax		500		MHz
Output Capacitance in HiZ	Cout		2.0		pF
Minimum Pulse Width (Note 5)					
ECL			1.0		ns
3V			2.0		ns
5V			2.7		ns
7V			3.5		ns

The specified limits shown can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least two minutes while maintaining the normal operating environment. (IBIAS = 1.2 mA, SLEWADJ = 2.5 mA)

Note 1: Tpd is measured from crossover point of DHI and DHI* to the 50% point in the output. DVL equals 0 V and DVH equals +3 V.

Note 2: Specification condition: DVL equals -1 V and DVH equals +1 V. Output is terminated to GND by 100 Ω. Tpd is measured from the crossover point of DRVEN and DRVEN* to the point where a 10-percent change in output voltage occurs.

Note 3: The driver load is an 18 cm 50Ω transmission line terminated with 1KΩ in parallel with 3 pF.

Note 4: ECL output conditions. Signal reaches 100% of programmed value.

Note 5: The output pulse width is measured at the 50-percent points. Output reaches 100% of programmed value.

Ordering Information

Model Number	Package
E693AHJ	28-Pin PLCC (with Internal Heat Spreader)
EVM693AHJ	Edge693 Evaluation Module

Contact Information

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