Edge710
500 MHz Pin Electronics Driver, Window Comparator, and Load

EDGE HIGH-PERFORMANCE PRODUCTS

Description

The Edge710 is a totally monolithic ATE pin electronics solution manufactured in a high-performance complementary bipolar process. In Automatic Test Equipment (ATE) applications, the Edge710 incorporates a driver, a load, and a window comparator suitable for very fast bidirectional channels in VLSI, Mixed-Signal, and Memory test systems.

The three-statable driver is capable of generating 9V swings over a 12V range. In addition, 13V super voltage may be obtained under certain operating conditions. Separate rise and fall edge adjustments support both high speed and low speed applications, and allow for superior rise and fall time matching. An input power down mode allows extremely low leakage current in HiZ.

The load supports programmable source and sink currents of ± 35 mA over a 12V range, or it can be completely disabled. The source current, sink current, and commutating voltage are all independently set. In addition, the load is configurable and may be used as a programmable voltage clamp.

The window comparator spans a 12V common mode range, tracks input signals with edge rates greater than 6 V/ns, and passes sub-ns pulses. An input power down mode allows for extremely low leakage measurements.

The inclusion of all pin electronics building blocks into a 52 lead MQFP (10 mm body w/ internal heat spreader) offers a highly integrated solution that is traditionally implemented with multiple integrated circuits or discretes.

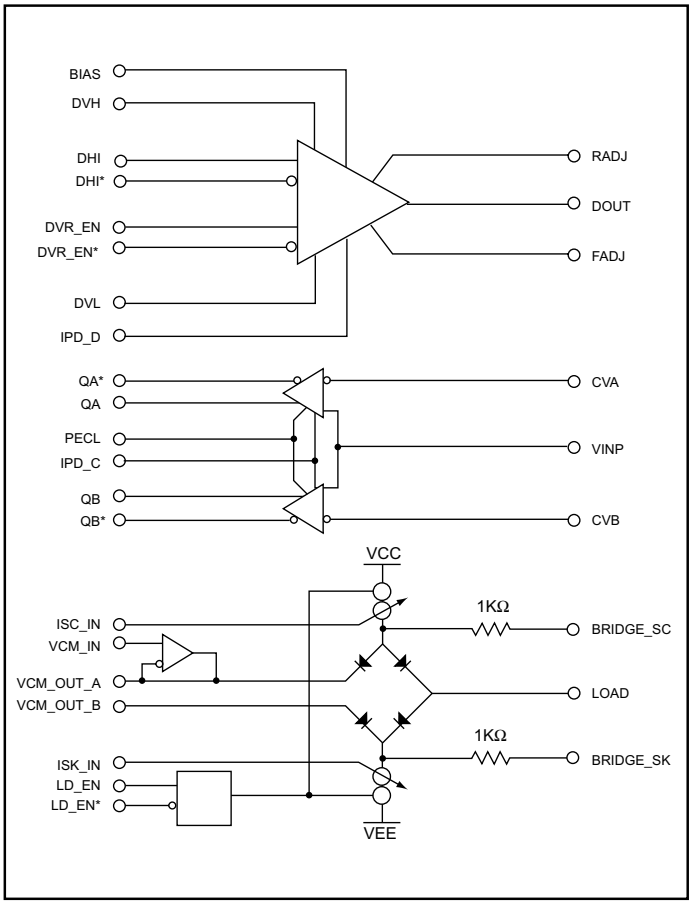
Applications

- VLSI Test Equipment
- Mixed-Signal Test Equipment
- Memory Testers (Bidirectional Channels)
- ASIC Verifiers

Features

- Fully Integrated Three-Statable Driver, Window Comparator, and Dynamic Active Load
- 12V Driver, Load, Compare Range
- 13V Super Voltage Capable
- ± 35 mA Programmable Load
- Comparator Input Tracking >6V/ns
- Leakage (L+D+C) < 1 µA (normal mode)
- Leakage (L+D+C) < 25 nA (IPD mode)
- Small footprint (52 pin MQFP)

Functional Block Diagram

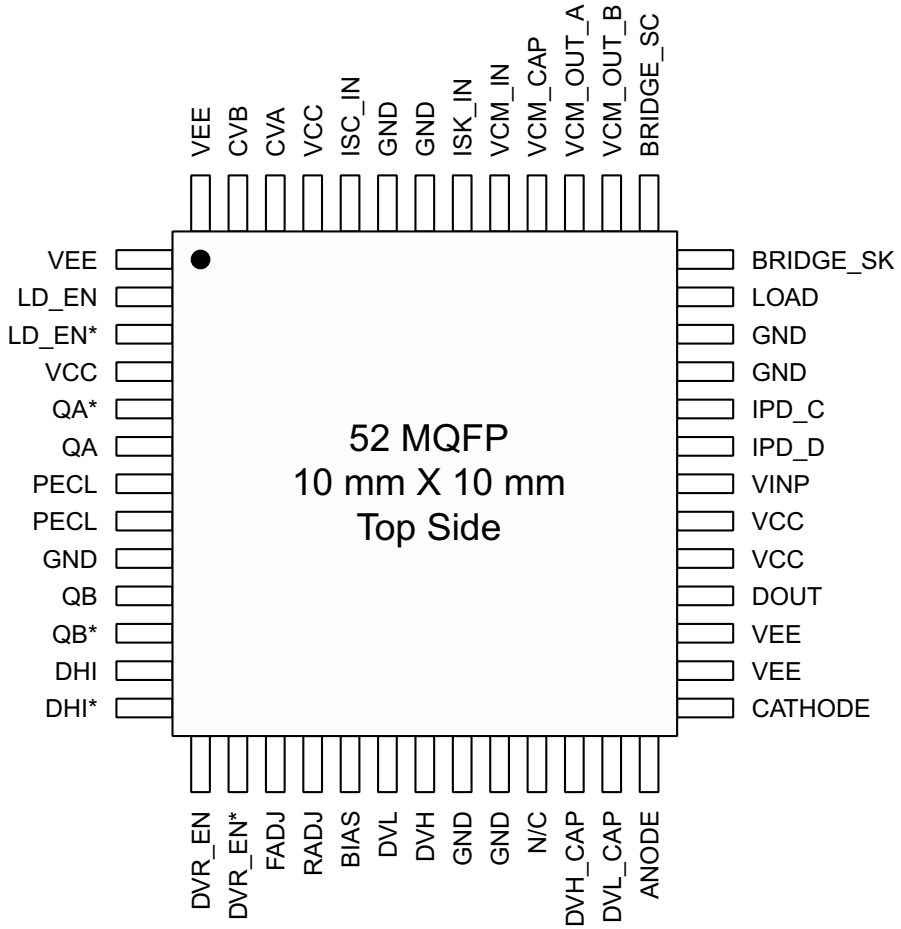


PIN Description

Pin Name	Pin #	Description
Driver		
DOUT	30	Driver Output.
DHI/DHI*	12, 13	Wide voltage differential input digital pins which determine the driver high or low level.
DVR_EN/DVR_EN*	14, 15	Wide voltage differential input digital pins which control the driver being active or in a high impedance state.
DVH, DVL	20, 19	High impedance analog voltage inputs which determine the driver high and low level.
DVH_CAP	24	Op amp compensation pin. A 100 pF capacitor should be connected to DVH.
DVL_CAP	25	Op amp compensation pin. A 100 pF capacitor should be connected to DVL.
RADJ, FADJ	17, 16	Input currents which determine the driver transition times.
BIAS	18	Analog current input which sets an internal bias current.
IPD_D	34	TTL driver input power down control which slows the driver down and reduces the driver HiZ leakage current.
Comparator		
VINP	33	Analog voltage input to the positive input of comparators.
CVA, CVB	50, 51	Analog inputs which set the comparator thresholds.
QA/QA* QB/QB*	6, 5 10, 11	Differential ECL (or PECL) digital outputs of comparators A and B.
IPD_C	35	TTL input power down input which slows the comparator down, but significantly reduces the VINP bias current.
PECL	7, 8	Unbuffered power supply level for the comparator output stages which establishes either ECL or PECL digital levels.
Load		
LOAD	38	Load Output.
LD_EN/LD_EN*	2, 3	Wide voltage differential inputs which activate and disable the load.
VCM_IN	44	High impedance analog voltage input that programs the commutating voltage.
ISC_IN, ISK_IN	48, 45	Analog current inputs which program the load source and sink currents. Should be connected to external voltage or current source through minimum 500 Ω series resistors.
VCM_CAP	43	Commutating buffer op amp compensation pin.
VCM_OUT_A VCM_OUT_B	42 41	Commutating voltage pins.
BRIDGE_SC BRIDGE_SK	40 39	Diode bridge connections to the output bridge that bypass the internal current sources.

PIN Description *(continued)*

Pin Name	Pin #	Description
Power Supplies, Miscellaneous		
CATHODE ANODE	27 26	Terminals of the on-chip thermal diode string.
VCC	4, 31, 32, 49	Positive power supply level.
VEE	1, 28, 29, 52	Negative power supply level.
GND	9, 21, 22, 36, 37, 46, 47	Device Ground.
N/C	23	No connect.



Driver

Introduction

The driver will force DOUT to one of three states:

1. DVH (Drive High)
2. DVL (Drive Low)
3. HiZ (High Impedance).

Both driver digital control inputs (DHI / DHI*, DRV_EN / DRV_EN*) are "Flex Inputs" - wide voltage differential inputs capable of receiving ECL, TTL, CMOS, or custom level signals. Single-ended operation is supported by connecting the inverting input to the appropriate DC threshold level.

Drive Enable

The drive enable (DRV_EN / DRV_EN*) inputs control whether the driver is forcing a voltage, or is placed in a high-impedance state. If DRV_EN is more positive than DRV_EN*, the output will force either DVH or DVL, depending on the driver data input. If DRV_EN is more negative that DRV_EN*, the output goes into a high impedance state.

Do NOT leave DRV_EN / DRV_EN* floating.

Driver Data

The driver data inputs (DHI / DHI*) determine whether the driver output is forcing a high or a low. If DHI is more positive than DHI*, the driver will force DVH when the driver is active. If DHI is more negative than DHI*, the driver will force DVL when active.

Do NOT leave DHI / DHI* floating.

Driver Enable	Driver Data	DOUT
DRV_EN > DRV_EN*	DHI > DHI*	DVH
DRV_EN > DRV_EN*	DHI < DHI*	DVL
DRV_EN < DRV_EN*	X	HiZ

Table 1. Driver Control Truth Table

Driver Levels

DVH and DVL are high input impedance voltage controlled inputs which establish the driver levels of a logical "1" and "0" respectively.

Driver Level Buffer Compensation

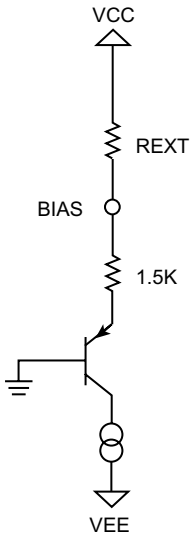
DVH_CAP and DVL_CAP are op amp compensation pins for the high and low level on-chip buffers. Each pin requires a 0.01 µF chip capacitor (with good high frequency characteristics) connected to ground. A tight layout with minimal distance between the pin and the capacitor is recommended.

Driver Bias

The BIAS pin is an analog current input which establishes an on-chip bias current, from which other currents are generated. This current, to some degree, also establishes the overall power consumption and performance of the chip. Ideally, an external current source would be used to minimize any part-to-part performance variation within a test system. However, a precision external resistor tied to a large positive voltage is acceptable. (See figure below.) The optimal BIAS current is a function of the RADJ and FADJ settings, and cannot be set independently.

The established bias current follows the equation:

$$BIAS = (VCC - 0.7) / (Rext + 1.5).$$



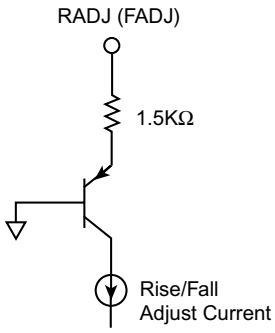
Circuit Description *(continued)*

Driver Slew Rate Adjustment

The driver rising and falling transition times are independently adjustable. The RADJ and FADJ pins are analog current inputs which establish the driver rise and fall times.

Ideally, an external current source would be used for RADJ and FADJ. However, for most applications (where the rise and fall times are fixed), precision external resistors to a positive voltage are acceptable. The currents into RADJ and FADJ follow the equation:

RADJ, FADJ = (VCC - 0.7) / (Rext + 1.5).



Input Power Down

IPD_D is a TTL compatible input which affects both the driver speed as well as high impedance leakage. With IPD_D = 0, the driver functions normally. With IPD_D = 1, the driver is in IPD mode, where it still functions, although with slower rise and fall times, but with an extremely low HiZ leakage current.

Do not leave IPD_D floating !! If IPD_D is not used, connect it to ground.

Load

The load is capable of sourcing and sinking at least 35 mA dynamically, or being placed into a high impedance state. The load may also be configured with separate commutating voltage to act as a programmable voltage clamp. In addition, the load may act as a 50Ω transmission line termination.

Load Enable

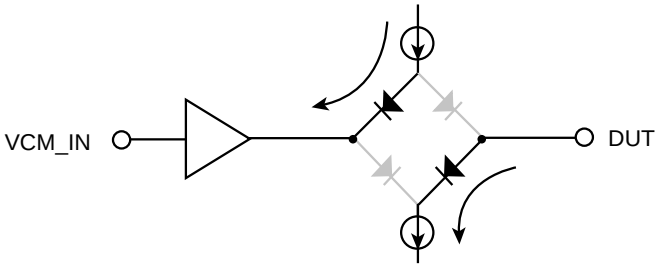
The load enable input determines whether the load is active or in high impedance. If LD_EN is more positive than LD_EN*, the load is active and is capable of sourcing and sinking currents. If LD_EN is more negative than LD_EN*, the load is placed into a high impedance state.

LD_EN / LD_EN* are "Flex In" - wide voltage differential inputs capable of receiving ECL, TTL, CMOS, or custom levels. Single-ended operation is supported by connecting the inverting input to the appropriate DC threshold level.

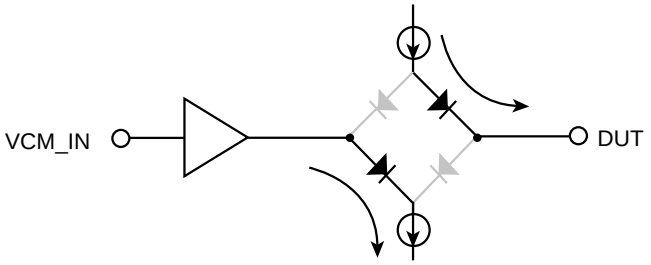
Do NOT leave LD_EN / LD_EN* floating.

Commutating Voltage

VCM_IN is a high input impedance analog voltage input which sets the commutating voltage of the load. If LOAD is more positive than VCM_IN, the bridge will sink current from the DUT into the load. If LOAD is more negative than VCM_IN, the load will source current from the load into the DUT.



LOAD > VCM_IN



LOAD < VCM_IN

Circuit Description *(continued)*

Source and Sink Current Levels

The amount of current that the diode bridge can source and sink is adjustable from 0 mA to 35 mA. The source and sink levels are separate and independent.

ISC_IN and ISK_IN are current controlled inputs whose voltage level is held very close to ground (<100 mV variation) over the entire legal current input range.

There is a nominal gain of 20 between the ISC_IN current and the bridge source current.

$$ISOURCE = 20 * ISC\_IN$$

There is a nominal gain of –20 between the ISK_IN current and the bridge sink current.

$$ISINK = -20 * ISK\_IN$$

Because the inversion creates a 180˚ phase shift between ISK_IN and ISINK, there is a tendency toward instability. A minimum of 500 W of external series resistance should be used between an external voltage or current source and the ISC_IN and ISK_IN pins to ensure stability. Stray capacitance at the ISK_IN pin should be kept to a minimum. PCB layout should minimize coupling between ISK_IN and LOAD.

Caution: The ISKIN and ISCIN inputs are designed for positive current between 0 mA and 1.75 mA flowing into the part. Care should be taken to insure that current is never required to flow out of the part on these two nodes.

Commutating Voltage Compensation

The VCM_CAP pin is an op amp compensation node that requires a fixed .01 µF chip capacitor (with good high frequency characteristics) to ground. This capacitor is used to compensate an internal node on the on-chip buffer for the commutating voltage input.

Split Load

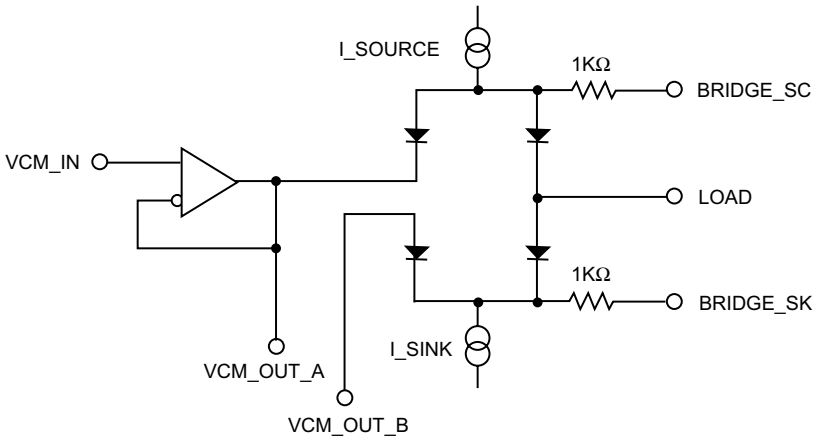
The VCM_OUT_A is the actual commutating voltage generated by the on-chip buffer. VCM_OUT_A is also connected to the upper half of the diode bridge, and is responsible for sinking the programmed source current when the load is sinking current from the DUT.

VCM_OUT_B is connected to the lower half of the diode bridge, and is responsible for providing the sink current when the load is sourcing current to the DUT.

VCM_OUT_B does NOT have an on-chip buffer. To configure the load as a standard active diode bridge, connect VCM_OUT_A and VCM_OUT_B together off-chip. Or, to configure the load as a split load, an external buffer must be used for VCM_OUT_B.

External Bridge Connections

Access to the top and bottom of the diode bridge is granted through a 1 KW resistor. Pins BRIDGE_SC and BRIDGE_SK allow external current sources to be used instead of the internal I_SOURCE and I_SINK sources. These external pins are useful when extremely accurate source and sink currents are required for low current operation.

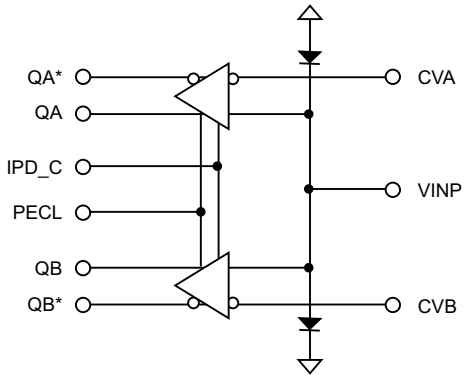


Window Comparator

Two comparators are connected on-chip to form a window comparator to determine whether the DUT is high, low, or in an indeterminant state. VINP is tied to the positive inputs of both comparators.

The selection of either comparator A or B for the DUT high versus the DUT low is arbitrary. However, because the positive input is used on both comparators, the comparator used to detect DUT low will have an inversion at it digital outputs.

The figure below shows the correct polarity for the comparator connections.



Thresholds

CVA and CVB are the two comparator threshold levels. These inputs are high impedance voltage controlled inputs that determine at which VINP voltage the comparators will change output states.

PECL Level Capability

PECL is the power supply level for the output stage of the comparators. When connected to ground, the comparator outputs will be standard ECL outputs. However, by making PECL more positive, QA / QA* and QB / QB* will track PECL and also become more positive.

By raising these voltage levels, the comparators may connect directly with CMOS ICs.

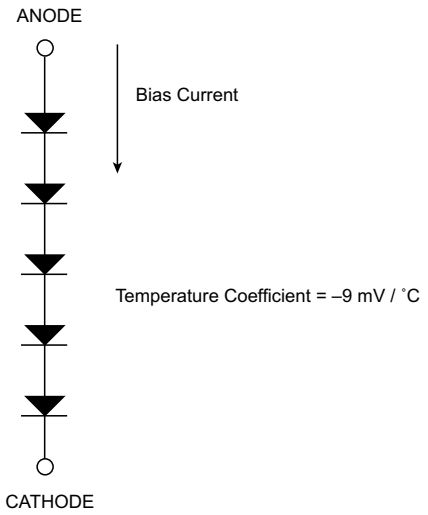
The power supply driving the PECL pin must be capable of sourcing all the current flowing out of the QA/QA* and QB/QB* open emitter outputs.

Comparator Input Protection

VINP connect to over-voltage diodes connected to the positive and negative power supplies. These diodes are sized to handle up to 100 mA current.

Thermal Monitor

An on-chip thermal diode string of five diodes in series exists (see figure below). This string allows accurate die temperature measurements.



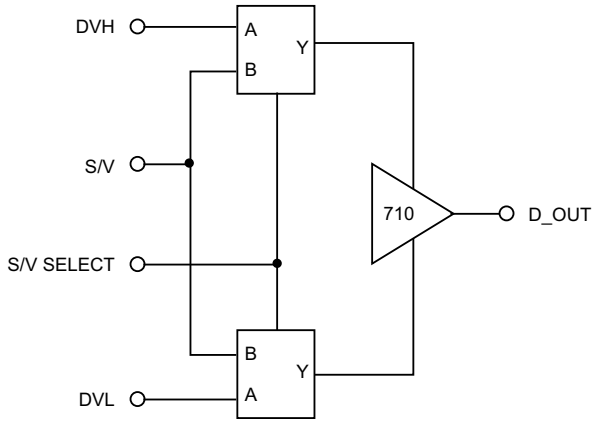
An external bias current of 100 µA is injected through the string, and the measured voltage corresponds to a specific junction temperature with the following equation:

$$Tj[^{\circ}C] = \{(ANODE - CATHODE)/5 - .7752\} / (-.0018).$$

Application Information

Super Voltage Operation

The Edge710 may be used to generate a super voltage level up to 13V at the driver output. To generate this high voltage, an analog input mux may be used to switch between the normal high and low drive levels, and a super voltage level.



Certain Power Supply conditions must be met to support this functionality.

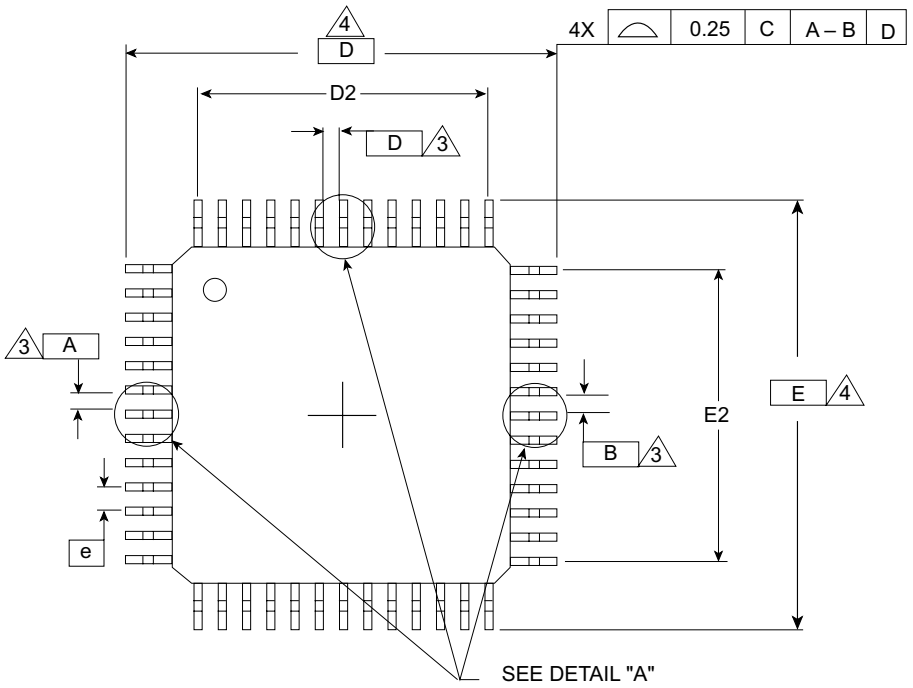
Extremely Low Leakage Usage

The Edge710 is capable of supporting total load + drive + comparator leakage ≤ ~15 nA. This low leakage mode may be very useful during PMU operation if the pin electronics are not isolated by a relay, thus eliminating the need for 1 relay per pin.

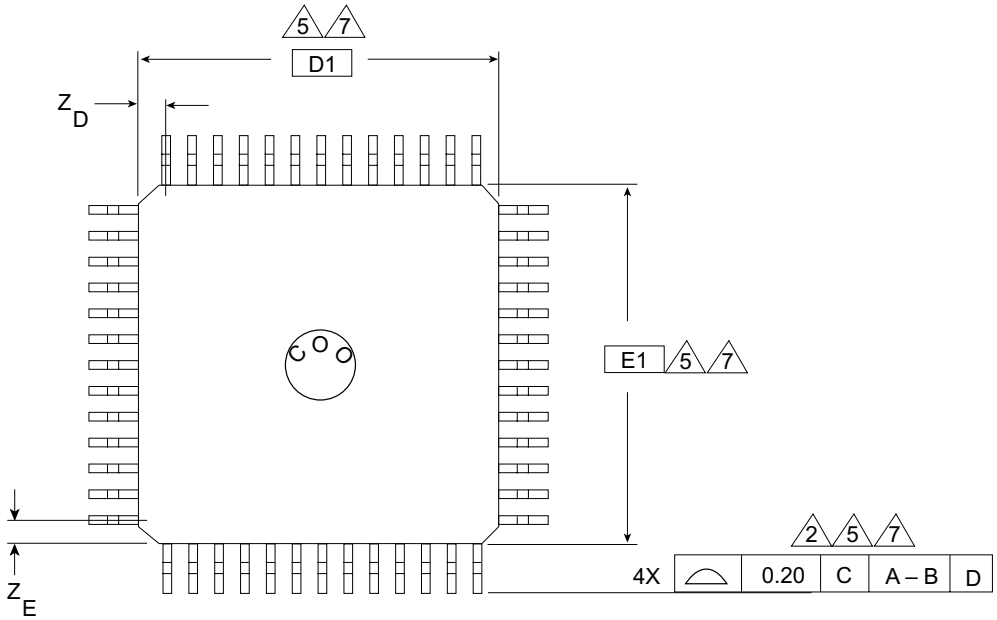
To realize this low leakage, the following conditions must be met:

1. IPD_D = 1 (place the driver in "power down" mode)
2. IPD_C = 1 (place the comparator in "power down" mode)
3. CVA, CVB ≥ VINP (program the comparator thresholds ≥ any expected voltage at the comparator inputs.)

Package Information

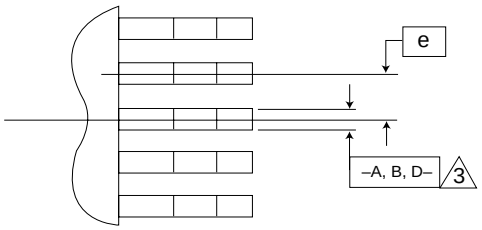


TOP VIEW

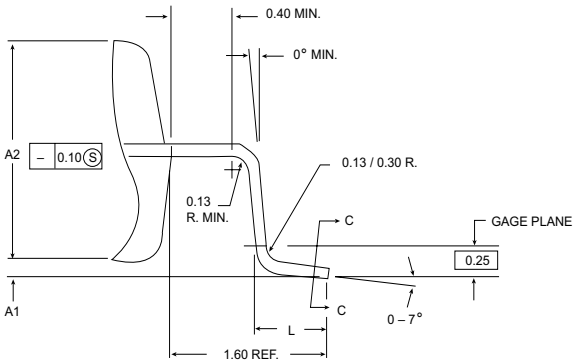


BOTTOM VIEW

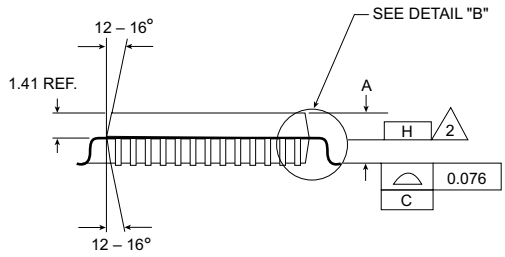
Package Information *(continued)*

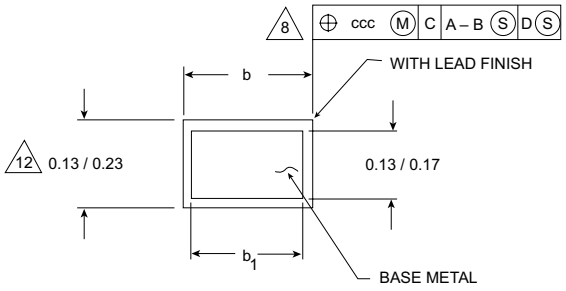


DETAIL "A"



DETAIL "B"





SECTION C-C

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5-1982.
2. Datum plane -H- located at mold parting line and coincident with lead, where lead exits plastic body at bottom of parting line.
3. Datums A-B and -D- to be determined where centerline between leads exits plastic body at datum plane -H-.
4. To be determined at seating plane -C-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable mold protrusion is 0.254 mm per side. Dimensions D1 and E1 do include mold mismatch and are determined at datum plan -H-.
6. "N" is the total # of terminals.
7. Package top dimensions are smaller than bottom dimensions by 0.20 mm, and top of package will not overhang bottom of package.
8. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot.
9. All dimensions are in millimeters.
10. Maximum allowable die thickness to be assembled in this package family is 0.635 millimeters.
11. This drawing conforms to JEDEC registered outline MS-108.
12. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.

JEDEC Variation
(all dimensions in millimeters)

Symbol	Min	Nom	Max	Note	Comments
A		2.15	2.35		Height above PCB
A1	0.10	0.15	0.25		PCB Clearance
A2	1.95	2.00	2.10		Body Thickness
D		13.20 BSC		4	
D1		10.00 BSC		5	Body Length
D2		7.80 REF			
ZD		1.10 REF			
E		13.20 BSC		4	
E1		10.00 BSC		5	Body Width
E2		7.80 REF			
ZE		1.10 REF			
L	0.73	0.88	1.03		
N		52		6	Pin Count
e		0.65			Lead Pitch
b	0.22		0.38	8	
b1	0.22	0.30	0.33		
aaa		0.12			

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Units
Positive Power Supply	VCC	9.0	15.5	V
Negative Power Supply	VEE	-8.0	-4.2	V
Total Analog Supply	VCC - VEE	13.2	20.5	V
Comparator Output Supply	PECL	0	5.0	V
Analog Inputs				
Driver High Level	DVH	VEE + 3.5	VCC - 2.9	V
Driver Low Level	DVL	VEE + 2.9	VCC - 3.5	V
Super Voltage Levels	DVH, DVL	VEE + 3.5	VCC - 2.0	V
Slew Rate Adjustments	RADJ, FADJ	.4	1.3	mA
Chip Bias	BIAS	.6	1.25	mA
Source, Sink Currents	ISC_IN, ISK_IN	0	1.65	mA
Comparator Thresholds	CVA, CVB	VEE + 3.5	VCC - 3.5	V
Ambient Operating Temperature	TA		+70	°C
Junction Temperature	TJ	25	+125	°C

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
VCC (relative to GND)	VCC	0	16.5	V
VEE (relative to GND)	VEE	-10	0	V
Total Power Supply	VCC - VEE		21.0	V
Digital Input Voltages	DHI(*), DVR_EN(*), LD_EN(*)	VEE	+7.0	V
Analog Input Voltages	CVA, CVB, DVH, DVL, VCM_IN	VEE	VCC	V
Analog Input Currents	ISC_IN, ISK_IN	0	3.0	mA
Digital Output Currents	QA/QA*, QB/QB*	0	50	mA
Driver Output Current	Iout	-40	+40	mA
Driver Swing	DVH - DVL	0	13	V
Comparator Input Voltage	CVA(B) - VINP	-13	+13	V
Ambient Operating Temperature	TA	-50	+125	°C
Storage Temperature	TS	-65	+150	°C
Junction Temperature	TJ		+150	°C
Soldering Temperature (5 seconds, .25" from the pin)	TSOL		+260	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these, or any other conditions beyond those listed, is not implied. Exposure to absolute maximum conditions for extended periods may affect device reliability.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
LOAD Circuit					
Commutating Voltage					
Programmable Range	VCM_IN	VEE + 3.5		VCC - 3.5	V
Offset Voltage	VCM_OUT_A - VCM_IN	-100		+100	mV
VCM_IN_A Current In	Iin	-100	5	+100	µA
Diff Voltage Range	LOAD - VCM_OUT_A	-10		+10	V
Load Output					
Output Voltage Range	V - LOAD	VEE + 3.5		VCC - 3.5	V
Output Current Range	I - LOAD	-35		+35	mA
Load Enable					
Input Voltage Range	LD_EN, LD_EN*	-2.0		+5.0	V
Differential Input Swing	LD_EN - LD_EN*	±0.25		±4.0	V
Input Current	Iin	-100		+100	µA
Source Current					
Input Current	ISC_IN	0		2.0	mA
ISC_IN Voltage	V_ISC_IN	-100	0	+100	mV
Current Gain	I_SOURCE/ ISC_IN	18.2	20	21.8	
Sink Current					
Input Current	ISK_IN	0		2.0	mA
ISK_IN Voltage	V_ISK_IN	-100	0	+100	mV
Current Gain	I_SINK/ ISK_IN	18.2	20	21.8	
Load Linearity					
0 mA <= Output < 5 mA	Actual - Programmed	-1µA - 1%		+1µA + 1%	µA
5 mA <= Output < 35 mA	Actual - Programmed	-50		+50	µA
HiZ Leakage Current	Ibias	-100	0	+100	nA
HiZ Compliance		VEE + .5		VCC	V
Source/Sink Bridge Resistance (measured @ I = 500 µA)		.5	1.0	2.0	KΩ
Source/Sink Error					
Cal Points / *Test Point*					
20 µA / 30 µA — 25 µA		-(1% + 1)		1% + 1	µA
30 µA / 130 µA — 80 µA		-(1% + 1)		1% + 1	µA
130 µA / 500 µA — 315 µA		-50		+50	µA
500 µA / 750 µA — 625 µA		-50		+50	µA
750 µA / 1 mA — 875 µA		-50		+50	µA
1 mA / 1.2 mA — 1.1 mA		-50		+50	µA
1.2 mA / 1.4 mA — 1.3 mA		-50		+50	µA
1.4 mA / 1.6 mA — 1.5 mA		-50		+50	µA
1.6 mA / 1.8 mA — 1.7 mA		-50		+50	µA

DC test conditions (unless otherwise specified): "Recommended Operating Conditions". RADJ = FADJ = 1.1 mA. BIAS = .6 mA.

DC Characteristics *(continued)*

Parameter	Symbol	Min	Typ	Max	Units
COMPARATOR Circuit					
V_INP Leakage (IPD = 0)					
@ +8V	I_BIAS	-2	±1 <	+2	µA
@ +5V	I_BIAS	-1		+1	µA
@ -2V	I_BIAS	-1		+1	µA
@ -4V	I_BIAS	-1		+1	µA
V_INP Leakage (IPD = 1)					
@ VEE + 3.5V	I_BIAS	-250	±100 <	+250	nA
@ VCC - 3.5V	I_BIAS	-250	±100 <	+250	nA
Offset Voltage (Note 1)					
IPD_C = 0	Vos	-10		+10	mV
IPD_C = 1	Vos	-10		+10	mV
Threshold Voltage	CVA, CVB	VEE + 2.9		VCC - 2.9	V
Threshold Input Current	I_BIAS CVA(B)	-50		+50	µA
Input Voltage Range	V_INP	VEE + 3.5		VCC - 3.5	V
Input Diffierential Range	V_INP - CVA(B)	-12		+8	V
Differential Output Swing	|QA - QA*|, |QB - QB*|	400			mV
Common Mode Output (Note 2)					
Logical 1	QA, QA*, QB, QB*	PECL - 1.3	PECL - 1.13	PECL - 0.9	V
Logical 0	QA, QA*, QB, QB*	PECL - 1.8	PECL - 1.64	PECL - 1.4	V
POWER SUPPLIES					
Power Supply Consumption (Note 3)					
Positive Supply	ICC	120		180	mA
Negative Supply	IEE	-200		-160	mA

DC test conditions (unless otherwise specified): "Recommended Operating Conditions". RADJ = FADJ = 1.1 mA. BIAS = .6 mA.

Note 1: This parameter is guaranteed by characterization. It is tested in production against ± 100 mV limits.
Note 2: Tested at PECL = 0V, PECL = +4V.
Note 3: No Load Conditions.

DC Characteristics *(continued)*

Parameter	Symbol	Min	Typ	Max	Units
DRIVER Circuit					
Analog Inputs					
High Level	DVH	VEE + 3.5		VCC - 2.9	V
Low Level	DVL	VEE + 2.9		VCC - 3.5	V
Super Voltage Levels	DVH, DVL	VEE + 3.5		VCC - 2.0	V
Driver Swing	DVH - DVL	0		9.0	V
Input Current	I_in	–50		+50	µA
Slew Rate Adjustments	RADJ, FADJ	0.4	0.6	1.3	mA
Chip Bias Current	BIAS	.6		1.25	mA
Driver Output					
DC Output Current	Imax	-35		+35	mA
Output Impedance (@ ±25 mA)	Rout	0.5		3.0	Ω
HiZ Leakage (IPD_D = 0)	Ibias	–250		+250	nA
HiZ Leakage (IPD_D = 1) (Note 1)	Ibias	–5		+5	nA
DC "High" Accuracy					
Offset Voltage	DVH - DOUT	–100		+100	mV
Gain (Note 2)	ΔDVH/ΔDOUT	.985		1.0	V/V
Linearity (-2V to +7V)	DVH - DOUT	-10		+10	mV
Linearity (@ -3V, @ +8V)	DVH - DOUT	-15		+15	mV
DC "Low" Accuracy					
Offset Voltage	DVL - DOUT	–100		+100	mV
Gain (Note 3)	ΔDVL/ΔDOUT	.985		1.0	V/V
Linearity (-3V to +6V)	DVL - DOUT	–10		+10	mV
Linearity (@ -4V, @ +7V)	DVL - DOUT	–15		+15	mV
Digital Inputs					
Input Voltage Range	DHI(*), DVR_EN(*)	–2.0		+5.0	V
Differential Input Swing	Input - Input*	±0.25		±4.0	V
Input Current	Iin	–350		+350	µA

Note 1: This parameter is guaranteed by characterization. It is tested in production against ± 200 nA limits.
Note 2: Gain is computed from 2 points: DVH = –1V, +4V.
Note 3: Gain is computed from 2 points: DVL = –1V, +4V.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
LOAD Circuit					
Propagation Delay					
Inhibit to Iout	Tpd_on		3		ns
Iout to Inhibit	Tpd_off		<.8		ns
Output Capacitance					
Load Active	Cout			3.5	pF
Load Off	Cout			2.0	pF
COMPARATOR Circuit					
Propagation Delay	Tpd		1.5		ns
Input Slew Rate Tracking					
IPD_C = 0		6.0			V/ns
IPD_C = 1		25			mV/ns
Input Capacitance	Cin		2.0		pF
Digital Output Rise and Fall Times (20% - 80%)	Tr, Tr		250		ps
Minimum Pulse Width				1.0	ns
DRIVER Circuit					
Propagation Delay					
Data to Output	Tpd		1.5		ns
Enable to HiZ	Tpd		1.5		ns
Enable to Output Active	Tpd		1.5		ns
Rise/Fall Times					
800 mV (20% - 80%)	Tr/Tf		500		ps
3V (10% - 90%)	Tr/Tf		800		ps
5V (10% - 90%)	Tr/Tf		1.0		ns
Fmax					
800 mV	Fmax		600		MHz
3V	Fmax		400		MHz
5V	Fmax		200		MHz
Minimum Pulse Width					
800 mV			800		ps
3V			1.2		ns
5V			2.4		ns
Output Capacitance	Cout		2.0		pF

DC test conditions (unless otherwise specified): "Recommended Operating Conditions".
RADJ = FADJ = 1.1 mA. BIAS = .6 mA.

Ordering Information

Model Number	Package
E710AHF	52 Lead MQFP (10 mm x 10 mm Body) with Internal Heat Spreader
D710	Die Form
EVM710AHF	Edge710 Evaluation Board

Contact Information

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