400mA SmartLDO™ with Internal Pass MOSFET

SC1532

January 3, 2000

TEL:805-498-2111 FAX:805-498-3804 WEB:http://www.semtech.com

DESCRIPTION

Intended for applications such as Power Managed PCI, the SC1532 is designed to maintain a glitch-free 3.3V output when at least one of two inputs, 5V (VIN1) and 3.3V (VIN2), is present.

The SC1532 combines a 5V to 3.3V linear regulator with an integral 3.3V bypass switch, along with logic and detection circuitry to control which supply provides the power for the output.

Whenever VIN1 exceeds a predetermined threshold value, the internal 3.3V PMOS linear regulator is enabled, and the internal pass NMOS is turned off. When VIN1 falls below a lower threshold value, the NMOS pass device is turned on and the PMOS linear regulator is turned off. This ensures an uninterrupted 3.3V output even if VIN1 falls out of specification.

When both supplies are simultaneously available, the PMOS linear regulator will be turned on, and the NMOS pass will be turned off, thus preferentially supplying the output from the 5V supply.

The internal 5V detector has its upper threshold (for VIN1 rising) set to 4.18V (typical) while the lower threshold (for VIN falling) is at 4.1V (typical) giving a hysteresis of approximately 80mV.

The SC1532 is available in the popular SO-8 surface mount package.

FEATURES

- Glitch-free transition between input sources
- Internal logic selects input source
- 5V detector with hysteresis
- 1% regulated output voltage accuracy
- 400mA load current capability

APPLICATIONS

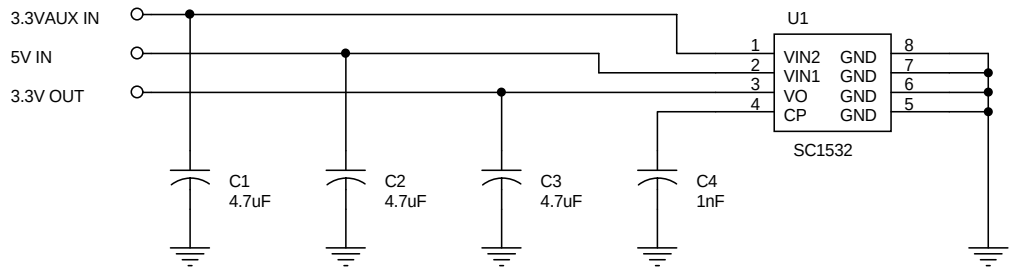
- Desktop Computers
- Network Interface Cards (NICs)
- PCMCIA/PCI Interface Cards
- Peripheral Cards

ORDERING INFORMATION

Part Number(1)	Package
SC1532CS	SO-8

Note:
(1) Add suffix 'TR' for tape and reel packaging.

TYPICAL APPLICATION CIRCUIT



NOTES:
(1) Ceramic capacitors are recommended - see Applications Information for further details.
(2) Output capacitor C3 needs to be 1.0uF or greater for stability. Additional capacitance (tantalum or ceramic) will improve overall performance.

652 MITCHELL ROAD NEWBURY PARK CA 91320

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Maximum	Units
Input Supply Voltages	VIN1, VIN2	-0.5 to +7	V
Charge Pump Capacitor Pin Voltage	CP	-0.5 to +16	V
Output Current	I_O	400	mA
Operating Ambient Temperature Range	T_A	-5 to +70	°C
Operating Junction Temperature Range	T_J	-5 to +125	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature (Soldering) 10 Sec	T_{LEAD}	300	°C
Thermal Impedance Junction to Ambient(1)	θ_{JA}	65	°C/W
ESD Rating (Human Body Model)	ESD	4	kV

NOTE:
(1) 1 inch square of 1/16" FR-4, double sided, 1 oz. minimum copper weight.

ELECTRICAL CHARACTERISTICS

Unless specified, T_A = 25°C, VIN1 = 5V, VIN2 = 3.3V, I_O = 400mA, CIN1 = 4.7uF, CIN2 = 4.7uF, C_O = 4.7uF, Cp=1nF.
Values in **bold** apply over full operating temperature range.

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
VIN1						
Supply Voltage	VIN1	VIN2 = 0V	4.3	5.0	5.5	V
Quiescent Current	I_{Q1}	VIN1 = 5V, 0V ≤ VIN2 ≤ 3.6V, I_O = 0mA		2.0	3.0	mA
					4.0	
Reverse Leakage From VIN2(1)	I_{VIN1}	VIN1 = 0V, VIN2 = 3.6V, I_O = 0mA		0	**1**	µA
VIN2						
Supply Voltage	VIN2		3.0	3.3	3.6	V
Quiescent Current	I_{Q2}	VIN2 = 3.3V, 0V ≤ VIN1 ≤ 5.5V, I_O = 0mA		650	1300	µA
					2000	
Reverse Leakage From VIN1(1)	I_{VIN2}	VIN1 = 5.5V, VIN2 = 0V, I_O = 0mA		0	**1**	µA
5V Detect(1)(2)						
Low Threshold Voltage	$V_{TH(LO)}$	VIN1 Falling, I_O = 20mA	**3.90**	4.10		V
Hysteresis	V_{HYST}	I_O = 20mA	60	80	150	mV
High Threshold Voltage	$V_{TH(HI)}$	VIN1 Rising, I_O = 20mA		4.18	**4.30**	V

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ELECTRICAL CHARACTERISTICS (Cont.)

Unless specified, T_A = 25°C, VIN1 = 5V, VIN2 = 3.3V, I_O = 400mA, CIN1 = 4.7uF, CIN2 = 4.7uF, C_O = 4.7uF, Cp=1nF.
Values in **bold** apply over full operating temperature range.

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
VO						
LDO Voltage Accuracy	VO	I_O = 20mA	-1		+1	%
		4.3V ≤ VIN1 ≤ 5.5V, 0mA ≤ I_O ≤ 400mA(1)	**-2**		**+2**	
		3.90V ≤ VIN1 ≤ 4.3V, VIN2 = 3.3V, 0mA ≤ I_O ≤ 400mA(1)	**3.000**			V
VIN2 Pass Device On Resistance (Aux. NMOS)(1)(3)	$R_{DS(ON)}$	VIN1 < 3.9V, 0mA ≤ I_O ≤ 400mA		360	**500**	mΩ
Line Regulation	$REG_{(LINE)}$	VIN1 = 4.3V to 5.5V		0.3	0.6	%
					0.7	
Load Regulation	$REG_{(LOAD)}$	I_O = 20mA to 400mA		0.3	0.6	%
					0.7	
Current Limit (LDO)						
Output Current	I_{LIM}	VIN1 = 5V, VIN2 = 0V, VO = 0V	600	975	1200	mA
					1400	
Over Temperature Protection						
High Trip Level	T_{HI}	VIN1=5V		175		ºC
Hysteresis	T_{HYS}	VIN1=5V		10		ºC

NOTES:
(1) Guaranteed by design.
(2) Recommended source impedance for 5V supply: ≤ 0.125Ω. This will ensure clean transitions between supplies with no "chattering" (see Applications Information).
(3) Refer to block diagram.

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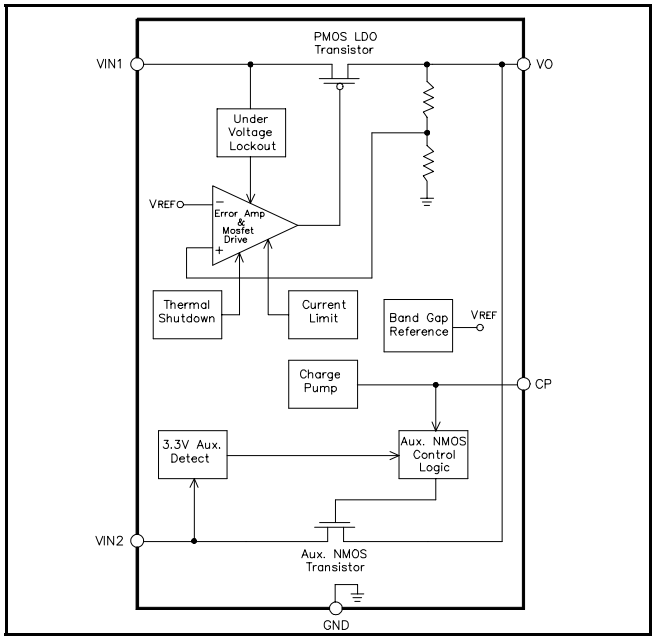
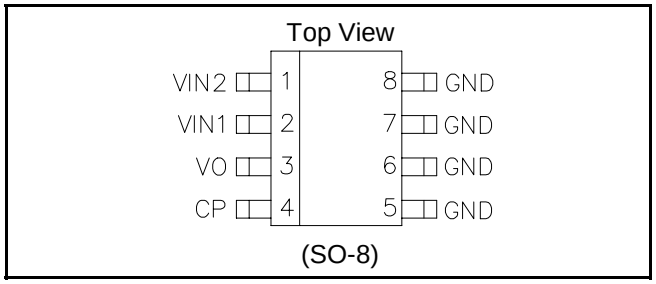
BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTIONS

Pin	Pin Name	Pin Function
1	VIN2	Secondary input supply, nominally 3.3V.
2	VIN1	Main input supply for the IC, nominally 5V.
3	VO	3.3V out.
4	CP	Charge pump capacitor connection.
5	GND	Ground pin.
6	GND	Ground pin.
7	GND	Ground pin.
8	GND	Ground pin.

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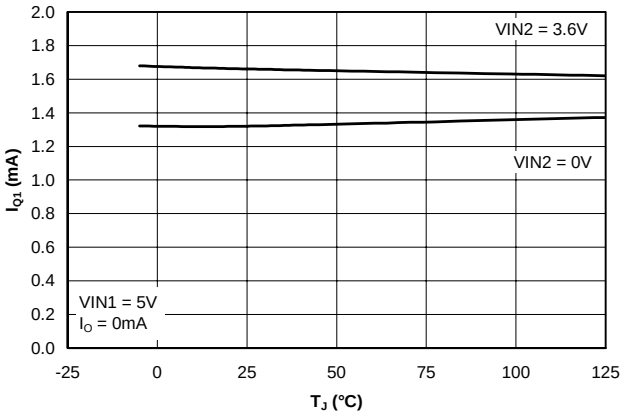
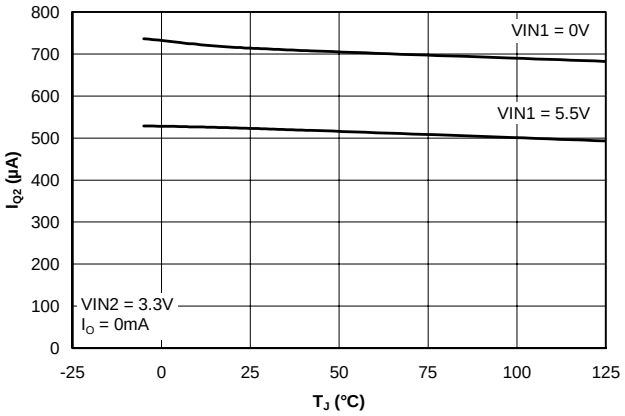
TYPICAL CHARACTERISTICS

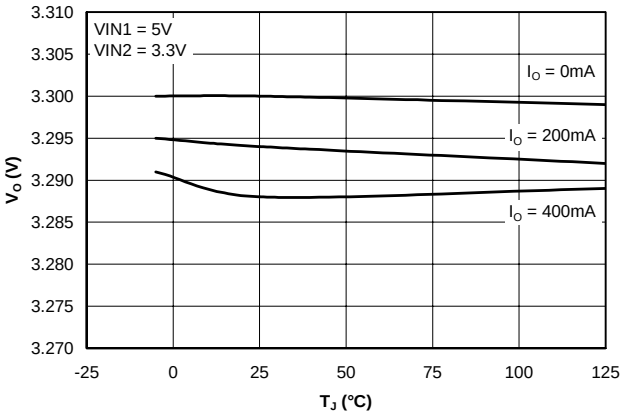
Quiescent Current (I_{Q1}) vs. Junction Temperature vs. VIN2



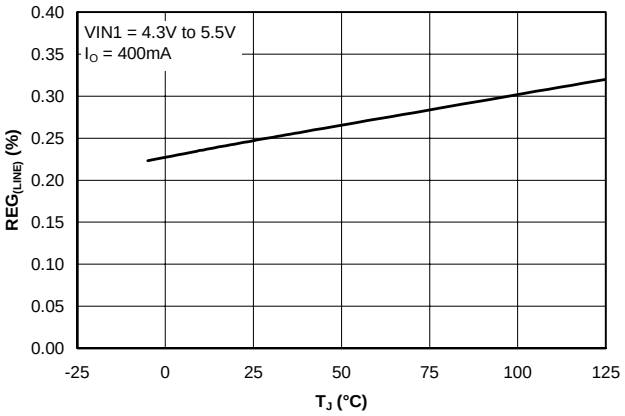
Quiescent Current (I_{Q2}) vs. Junction Temperature vs. VIN1



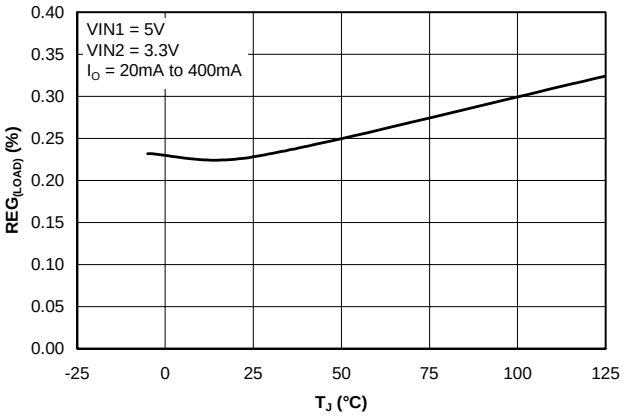
LDO Output Voltage vs. Junction Temperature vs. Output Current



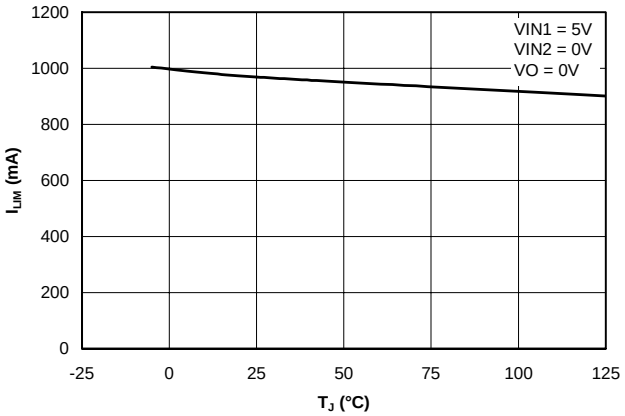
LDO Line Regulation vs. Junction Temperature



LDO Load Regulation vs. Junction Temperature



LDO Current Limit vs. Junction Temperature



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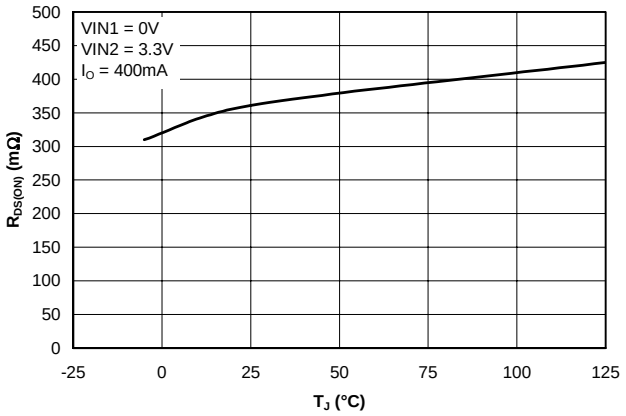
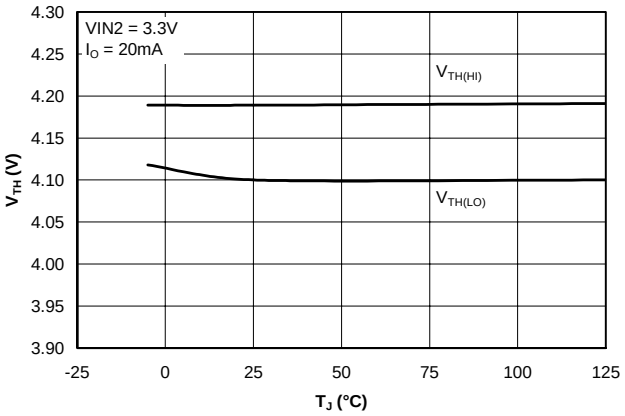
TYPICAL CHARACTERISTICS (Cont.)

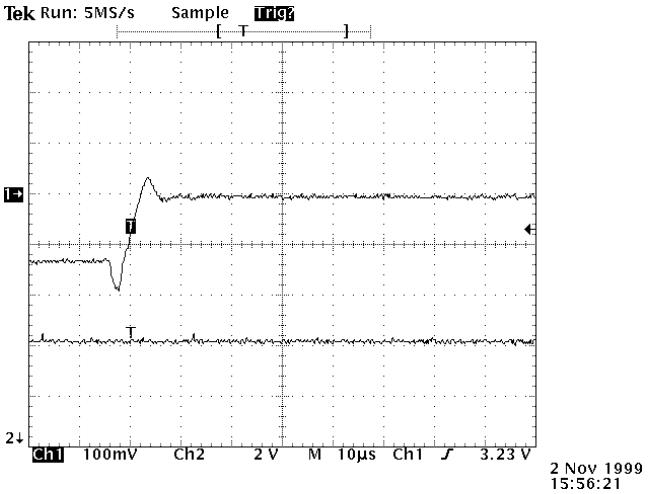
VIN2 Pass Device On Resistance vs. Junction Temperature



5V Detect Threshold Voltage vs. Junction Temperature

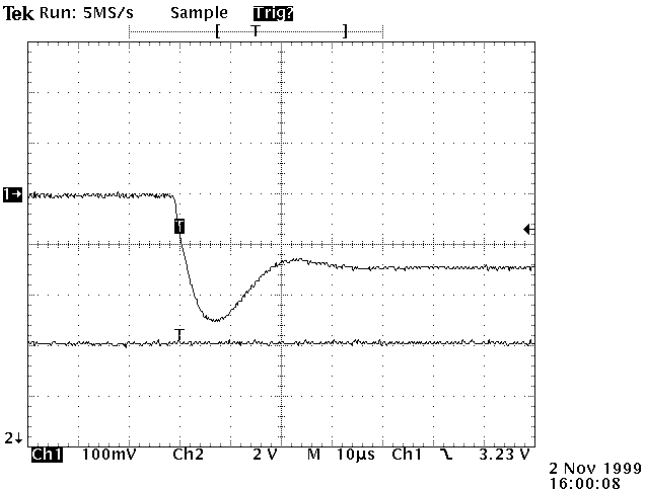


$VO_{(MIN)}$ With VIN1 Rising[1][2]



Trace 1: VO, offset 3.3V, 100mV/div.
Trace 2: VIN1 rising through $V_{TH(HI)}$, 2V/div.
$VO_{(MIN)}$ = 3.11V

$VO_{(MIN)}$ With VIN1 Falling[1][2]



Trace 1: VO, offset 3.3V, 100mV/div.
Trace 2: VIN1 falling through $V_{TH(LO)}$, 2V/div.
$VO_{(MIN)}$ = 3.05V

NOTES:
(1) In Application Circuit on page 1.
(2) R_L = 8.2Ω.

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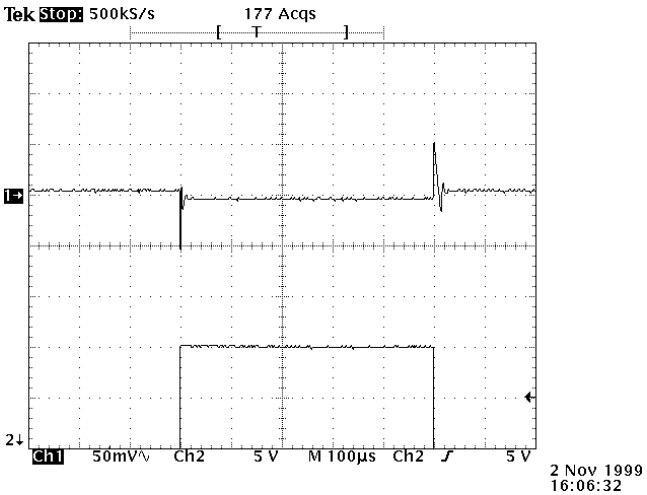
TYPICAL CHARACTERISTICS (Cont.)

Transient Load Response(1)



Trace 1: VO, offset 3.3V, 50mV/div.
Trace 2: I_O stepping from 0mA to 400mA

NOTES:
(1) In Application Circuit on page 2.

APPLICATIONS INFORMATION

Introduction

The SC1532 is intended for applications such as power managed PCI and network interface cards (NICs), where operation from a 3.3V VAUX supply may be required when the 5V supply has been shut down. It provides a simple, low cost solution that uses very little pcb real estate. During regular operation, 3.3V power for the PCI card is provided by the SC1532's on-board low dropout regulator, generated from the 5V supply. When the 5V supply is removed and 3.3V VAUX is available, the SC1532 connects this supply directly to its output using an internal NMOS pass device.

Component Selection

Output capacitors - Semtech recommends a 4.7µF or greater ceramic capacitor at the output for the best combination of performance and cost effectiveness. Increasing the capacitance value improves transient response and glitch performance. The SC1532 is very tolerant of output capacitor value and ESR variations, in fact any combination of capacitors with C ≥ 1µF and ESR < 1Ω is sufficient for stability. This target is easily met using surface mount ceramic or tantalum capacitors.

Input capacitors - Semtech recommends the use of a 4.7µF ceramic capacitor at both inputs. This allows for the device being some distance from any bulk capacitance on the rail. Additionally, input droop due to load transients is reduced, improving load transient response and aiding smooth supply transitions. Tantalum capacitors should not be used.

Charge pump capacitor - Semtech recommends the use of a 1nF ceramic capacitor between CP and GND.

Thermal Considerations

When operating from the 5V supply, the power dissipation in the SC1532 is approximately equal to the product of the output current and the input to output voltage differential:

$$P_D \approx (VIN1 - VO) \bullet I_O$$

The absolute worst-case dissipation is given by:

$$P_{D(MAX)} = (VIN1_{(MAX)} - VO_{(MIN)}) \bullet I_{O(MAX)} + VIN1_{(MAX)} \bullet I_{Q1(MAX)} + VIN2_{(MAX)} \bullet I_{Q2(MAX)}$$

Note that the $VIN2_{(MAX)}$ x $I_{Q2(MAX)}$ term does not apply if VIN2 is not supplied.

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APPLICATIONS INFORMATION (Cont.)

Inserting VIN1 = 5.5V, VO = 3.234V, I_O = 400mA, VIN2 = 3.6V, I_{Q1} = 4mA and I_{Q2} = 2mA yields:

$$P_{D(MAX)} = 0.936\ W$$

Using this figure, we can calculate the maximum thermal impedance allowable to maintain $T_J \leq 125°C$ at an ambient temperature of 55°C:

$$R_{TH(J-A)(MAX)} = \frac{(T_{J(MAX)} - T_{A(MAX)})}{P_{D(MAX)}} = \frac{(125 - 55)}{0.936} = 75°C/W$$

This is readily achievable using pcb copper area to aid in conducting the heat away from the device (see Figure 1 below).

VIN1 Source Impedance

In order to ensure seamless transitions between supplies with VIN1 rising and falling, it is recommended that the source impedance of VIN1 is less than 0.125Ω. This is because as the output current switches from VIN1 to VIN2 and visa-versa, the supplies can "chatter" if:

$$I_O \bullet R_{SOURCE} > V_{HYST}$$

In general, this can be avoided by minimizing supply trace lengths and resistances. In circumstances where the source impedance is causing supply "chattering", increasing the value of the VIN1 input capacitor should solve the problem by reducing the instantaneous drop or jump in VIN1 as the supplies are switched.

Layout Considerations

While layout for linear devices is generally not as critical as for a switching application, careful attention to detail will ensure reliable operation. See Figure 1 below for a sample layout.

1) Attaching the part (pins 5 to 8) to a larger copper footprint will enable better heat transfer from the device, especially on PCBs where there are internal ground and power planes.

2) Place the input and output capacitors close to the device for optimal transient response.

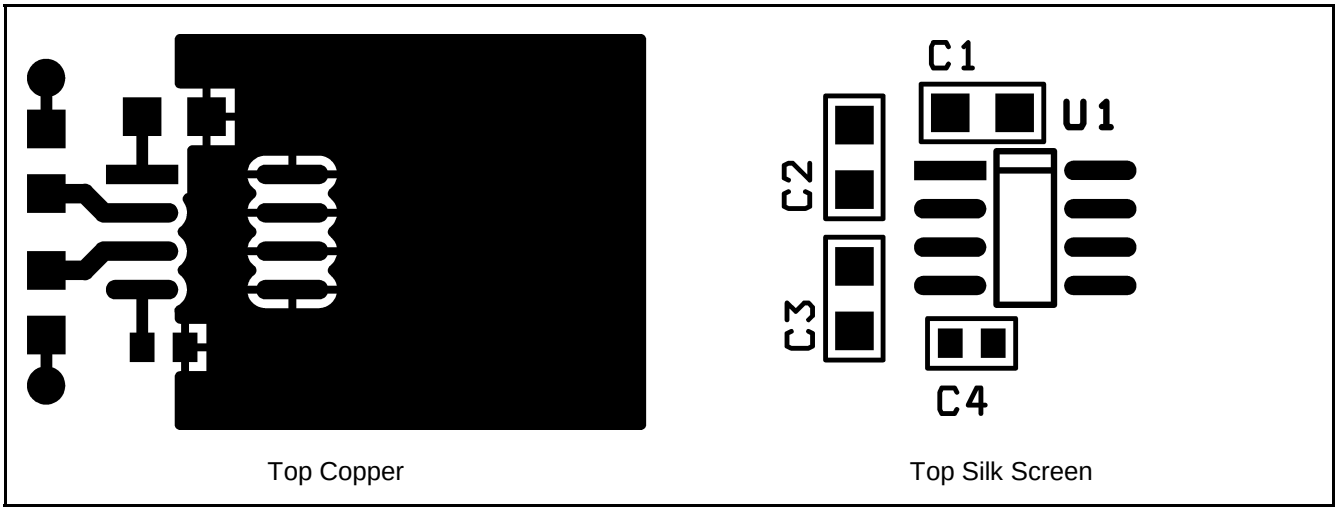

Fig. 1: Suggested pcb layout based upon Application Circuit on Page 1.

NOTES:

(1) All vias go to ground plane.

(2) Copper area on pins 5 thru 8 is recommended, 0.5" x 0.5" area only is shown. Connect to the ground plane with a via or vias.

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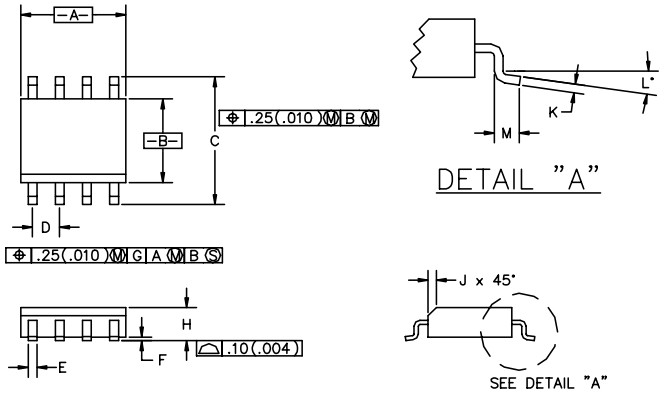
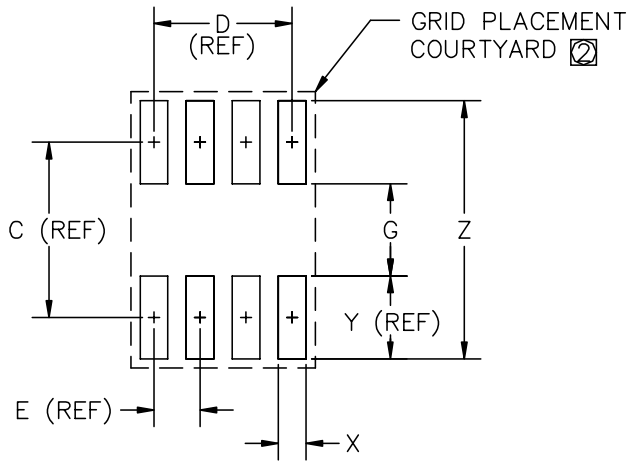
OUTLINE DRAWING - SO-8



JEDEC
REF: MS-012AA

DIMENSIONS					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.188	.197	4.80	5.00	
B	.149	.158	3.80	4.00	
C	.228	.244	5.80	6.20	
D	.050	BSC	1.27	BSC	
E	.013	.020	0.33	0.51	
F	.004	.010	0.10	0.25	
H	.053	.069	1.35	1.75	
J	.011	.019	0.28	0.48	
K	.007	.010	.19	.25	
L	0°	8°	0°	8°	
M	.016	.050	0.40	1.27	

MINIMUM LAND PATTERN - SO-8



DIMENSIONS (1)					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
C	–	.19	–	5.00	–
D	–	.15	–	3.81	–
E	–	.05	–	1.27	–
G	.10	.11	2.60	2.80	–
X	.02	.03	.60	.80	–
Y	–	.09	–	2.40	–
Z	–	.29	7.20	7.40	–

(2) GRID PLACEMENT COURTYARD IS 12x16 ELEMENTS (6 mm X 8mm) IN ACCORDANCE WITH THE INTERNATIONAL GRID DETAILED IN IEC PUBLICATION 97.

(1) CONTROLLING DIMENSION: MILLIMETERS

ECN99-789